Integrated Power Management for Wearable applications: Opportunities & Challenges

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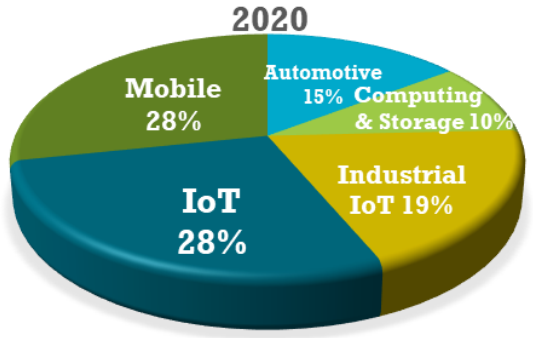
PwrSoc2020

Agenda

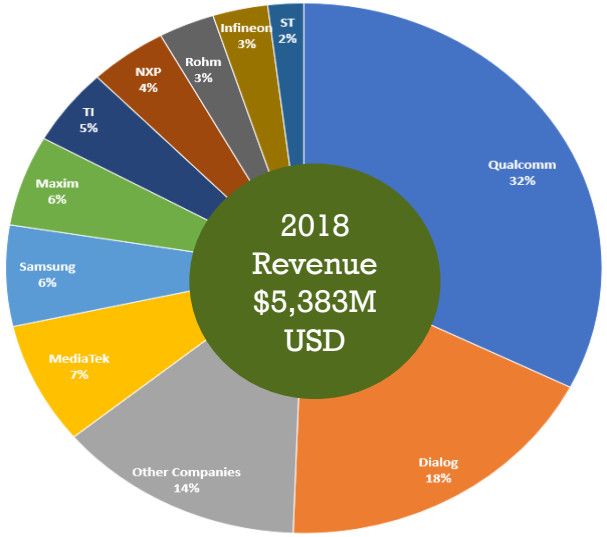
- Dialog Semiconductor
- Integrated Power Management for wearable applications: opportunity, markets, complexity, requirements
- Dialog‘s solutions for novel Integrated Power Management: performance, voltage, size, cost
- Open challenges for the future

Dialog Semiconductor (DLG) at a Glance

- Dialog Semiconductor is a leading provider of standard and custom integrated circuits (ICs) including **Power and Battery Management, Bluetooth® low energy, Wi-Fi and Configurable Mixed-signal ICs** .
- **“Powering the Smart Connected Future”**
- 2300 employees, fabless model

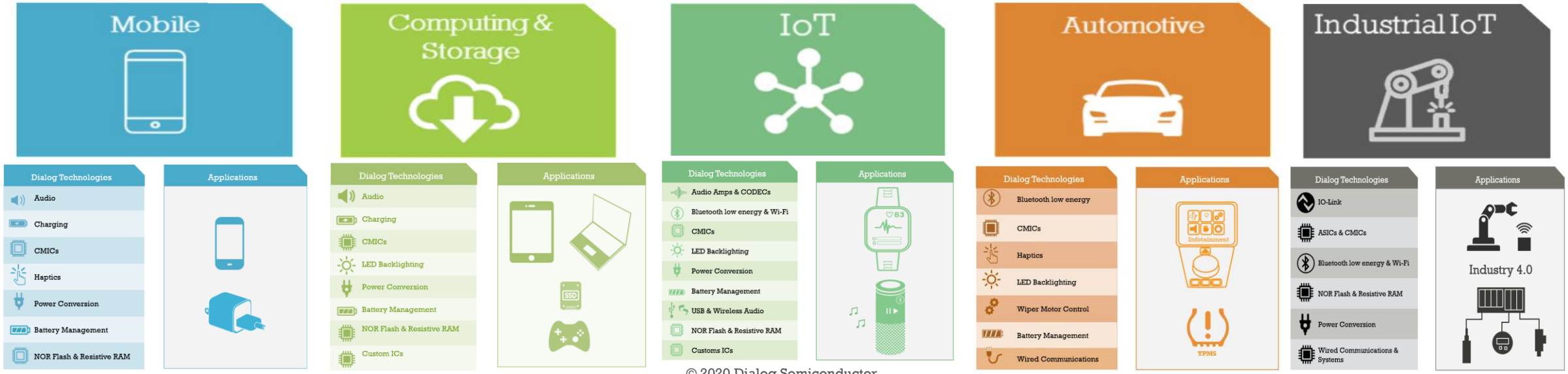


Percentage split by Dialog Markets



#1 Pure Play PMIC Supplier
Multi-Channel PMIC

Source: IHS Q2 2019

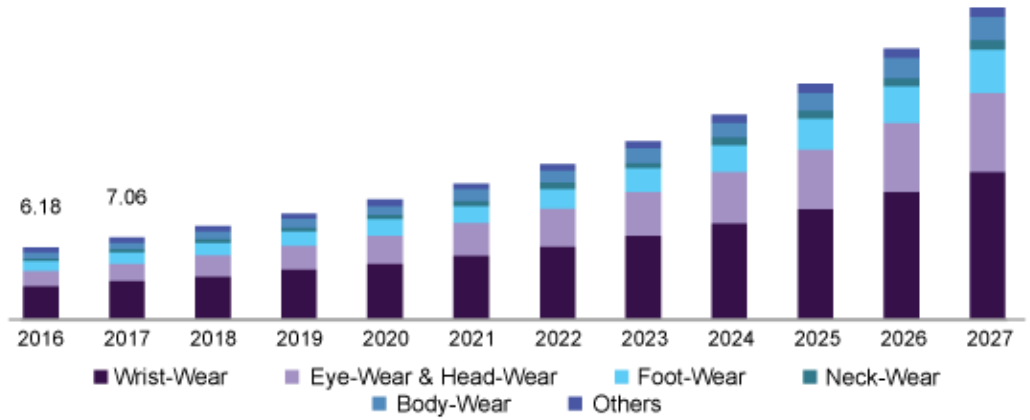


What is wearable?

Wearable devices driving stronger need for integration of technologies including power management for battery chargers, displays, SoC, sensors, audio.

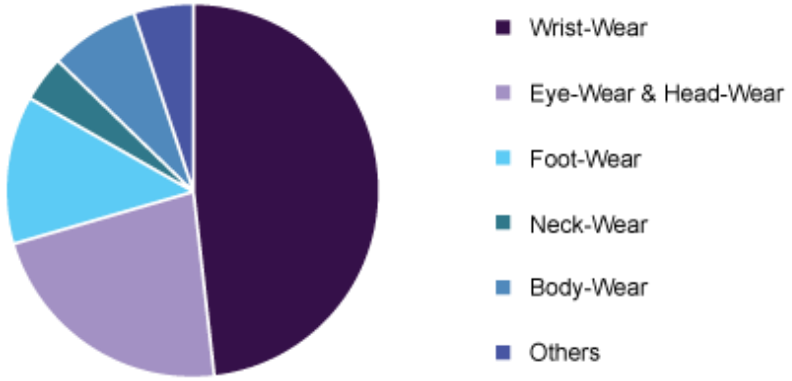
Opportunity: growth of wearable market

U.S. wearable technology market size, by product, 2016 - 2027 (USD Billion)



Source: www.grandviewresearch.com

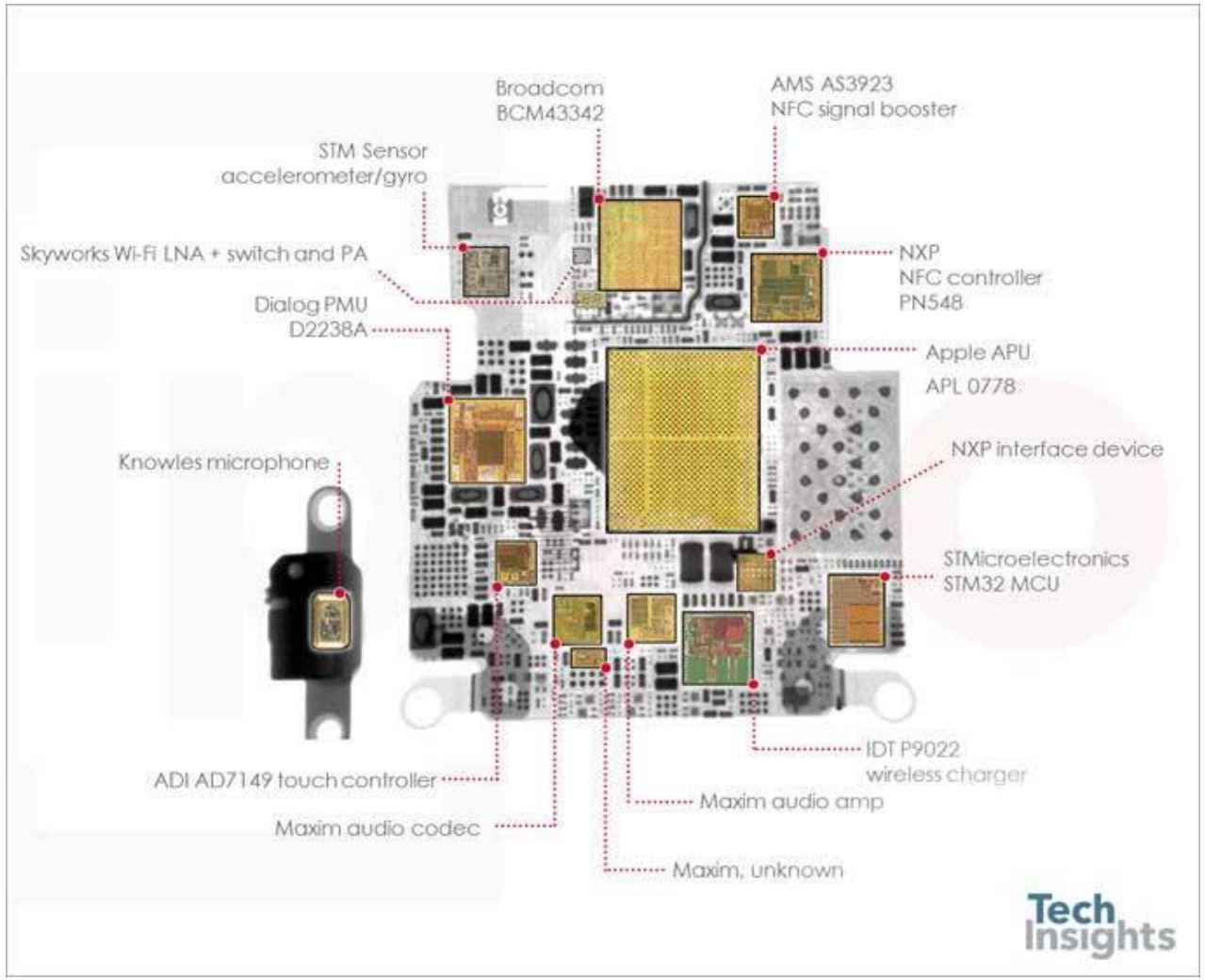
Global wearable technology market share, by application, 2019 (%)

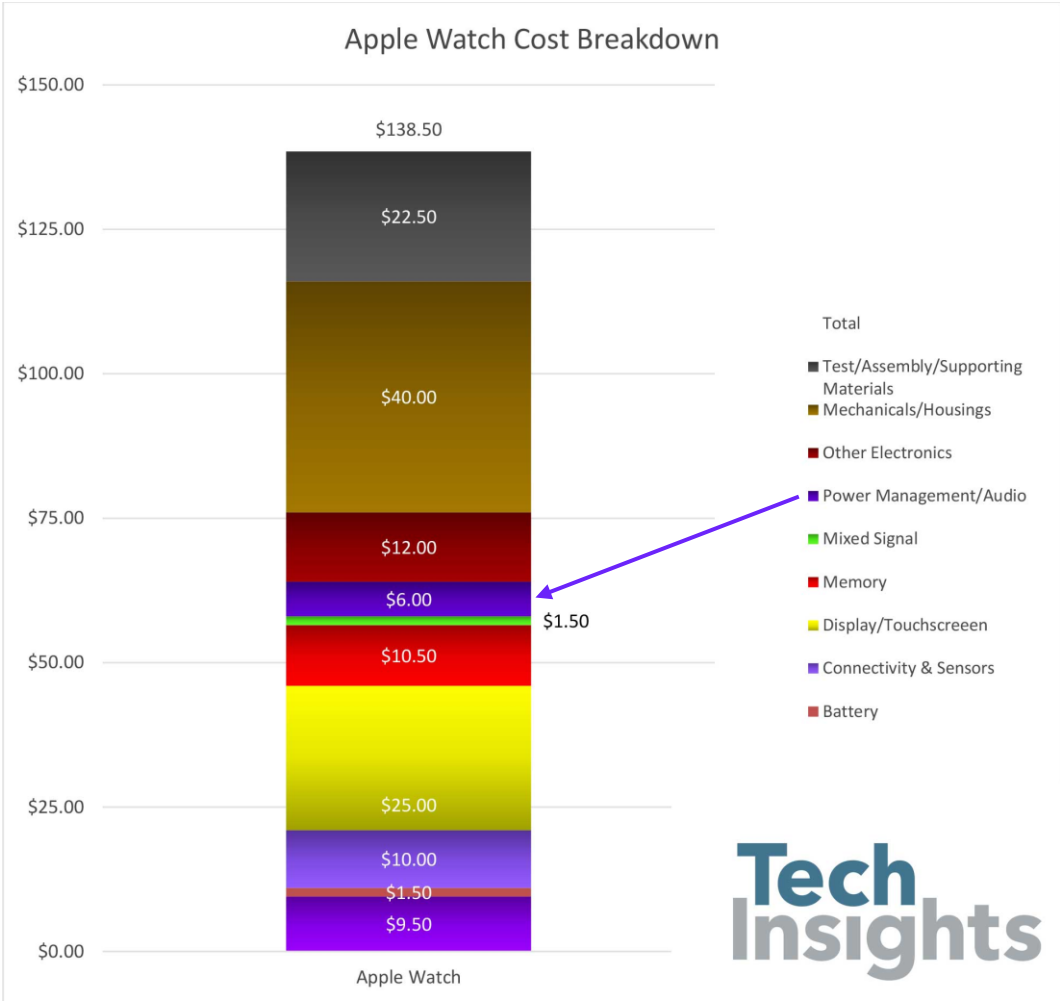


Source: www.grandviewresearch.com

- **Hearables/TWS**
  - Key Trends: Rapidly growing market segregating into
  - High-end (Tier-1 OEM): high integration, power, complexity
  - Mid-end (Tier-2 OEM): more features fuel gauge, communication protocols (PLC)
- **AR/VR**
  - Advancements in display technology (µLED) are key to AR success
  - VR systems are increasing in capability. Popularity and shipments are growing
- **Smartwatch**
  - Key Trends: transition to AMOLED for broader market
  - Increased functionality with simultaneous increase in battery life
- SAM growing annually at double-digit %.

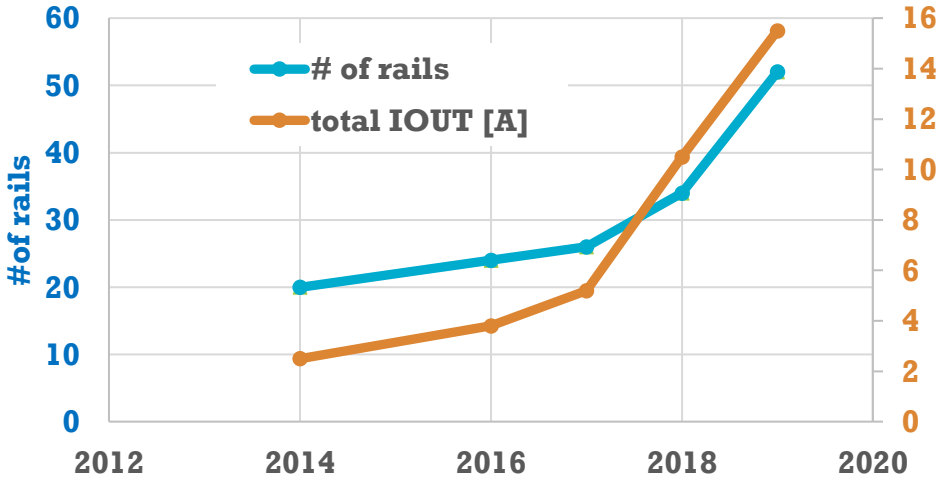
Opportunity: Integrated Power Management for Wearables

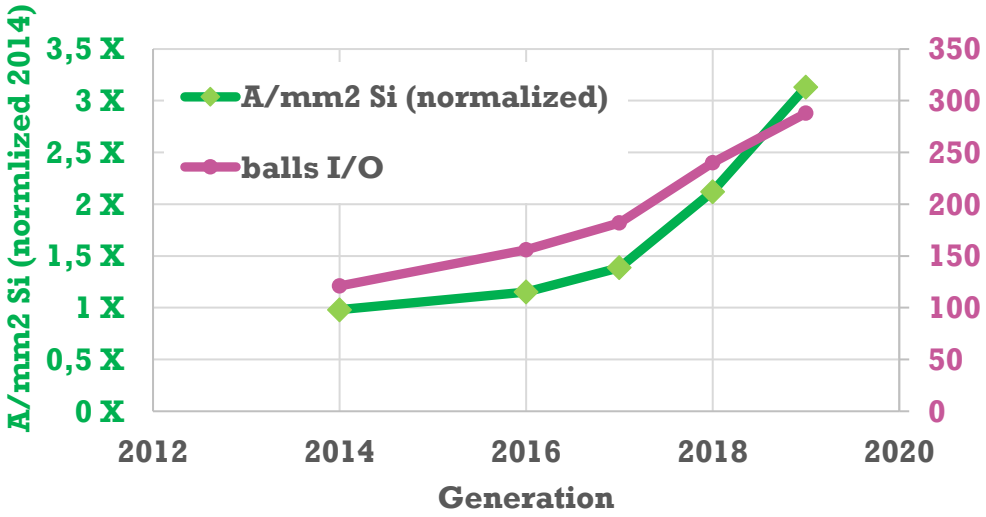




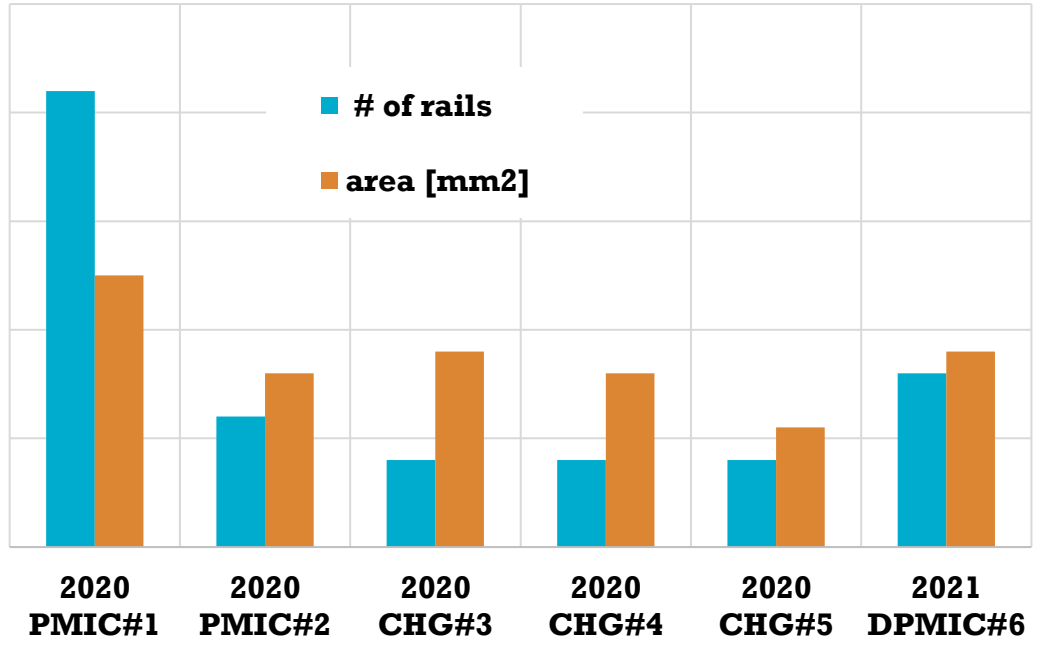
PMIC for Wearables: trends

Ultra-high-end wearable PMIC





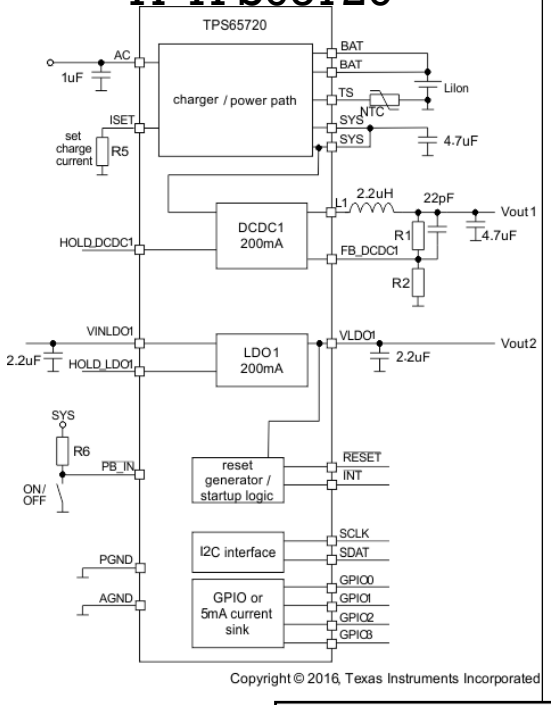
Medium-end wearable PMIC



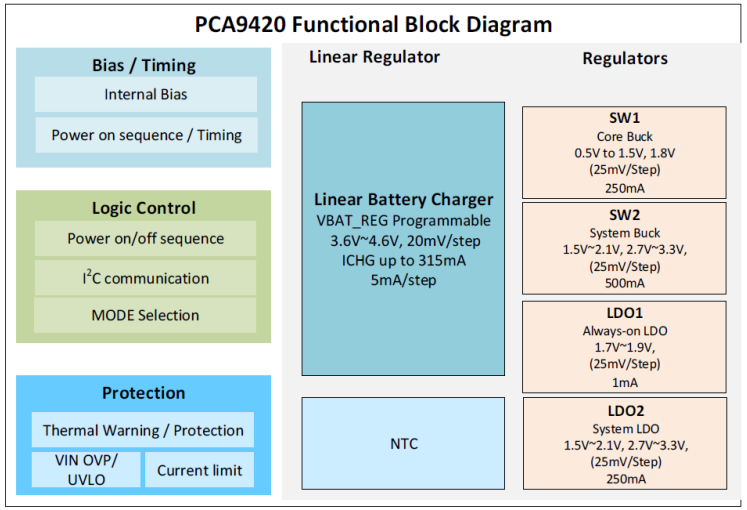
Typical PMIC products for Wearables

PMIC includes- Battery charger, DC-DC, LDOs, I2C interface

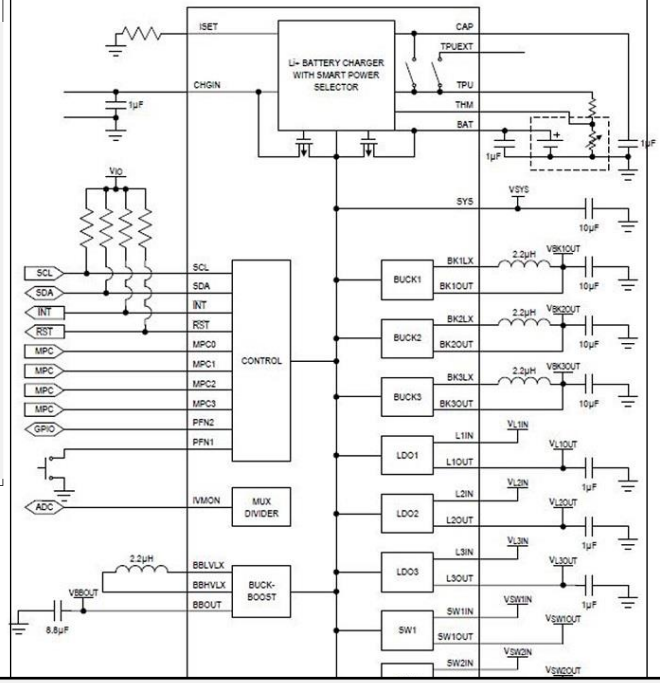
TI-TPS65720



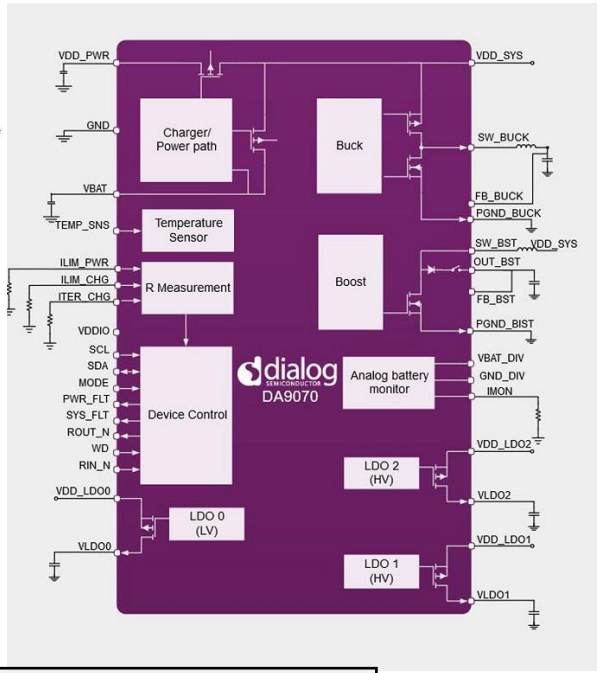
NXP-PCA9420



Maxim-Max20345



Dialog-DA9070



Competition about

- ✓ *Compact size*
- ✓ *Low Quiescent Current*
- ✓ *Noise performance / EMI mitigations*
- ✓ *Increased functionality and integration*

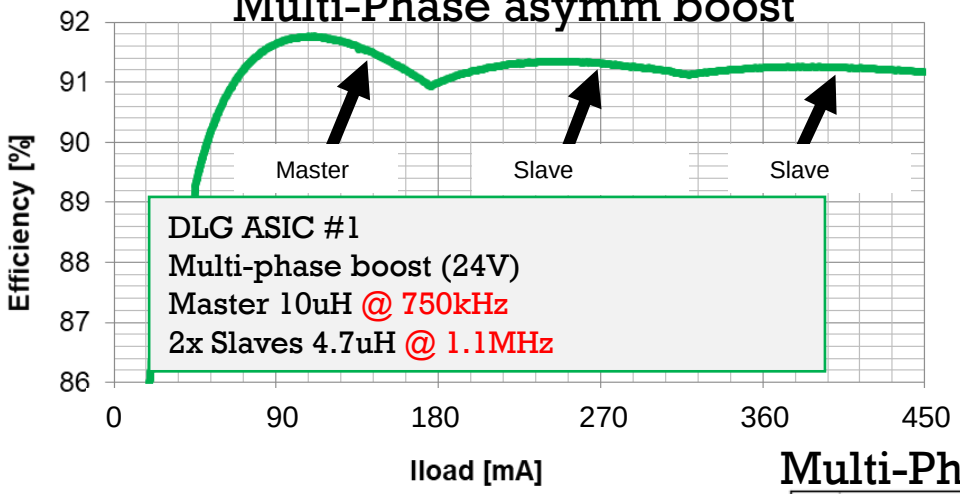
Challenge: Requirements of Integrated Power Management for Wearables

- Performance requirements (Iq, transient, efficiency)
  - Ship mode: wake-up circuits <100nA. Significant challenge on power FETs.
  - Sleep mode(s): <500nA with regulators on
- Voltage requirements
  - Li-Ion batteries dominate
  - 2.2-5V are must-have. Strong demand for supporting 2V minimum (transient of some ms = DC…)
  - USB interface 20V support (up to 30V for customer-specific reliability tests)
  - Integrated PMIC to generate power **negative** supplies (display): i.e. 5-10W @ -10V
  - Integrated PMIC to support +30V and -10V simulateneously, i.e. 40V BCD Process Tech
- Size requirements
  - Tier-1: extremely high integration, ~20-40 mm2 PMIC (30+ rails)
  - Tier-2: simpler power tree but growing ~8-15 mm2 PMIC (5-15 rails)
- Cost requirements:
  - Competing with stand-alone regulators
    - LDO ~0.01-0.02 USD optimized for low cost
    - DC/DC ~0.05 USD optimized for low cost

DLG Solutions: Architectures for **performance** requirements

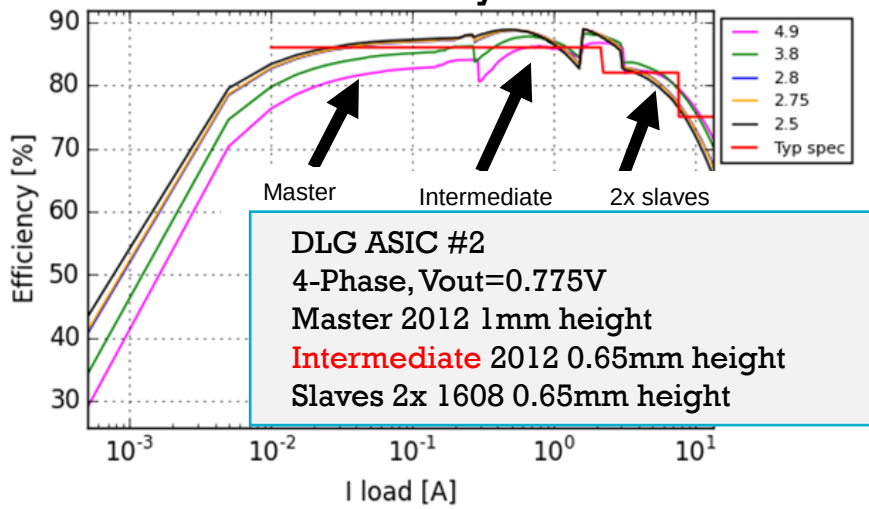
Efficiency: asymmetric multi-phase (**Patents US9768688, US9837906**)

Multi-Phase asymm boost



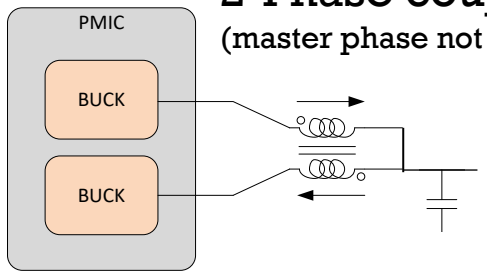
DLG ASIC #1
Multi-phase boost (24V)
Master 10uH @ 750kHz
2x Slaves 4.7uH @ 1.1MHz

Multi-Phase asymm buck

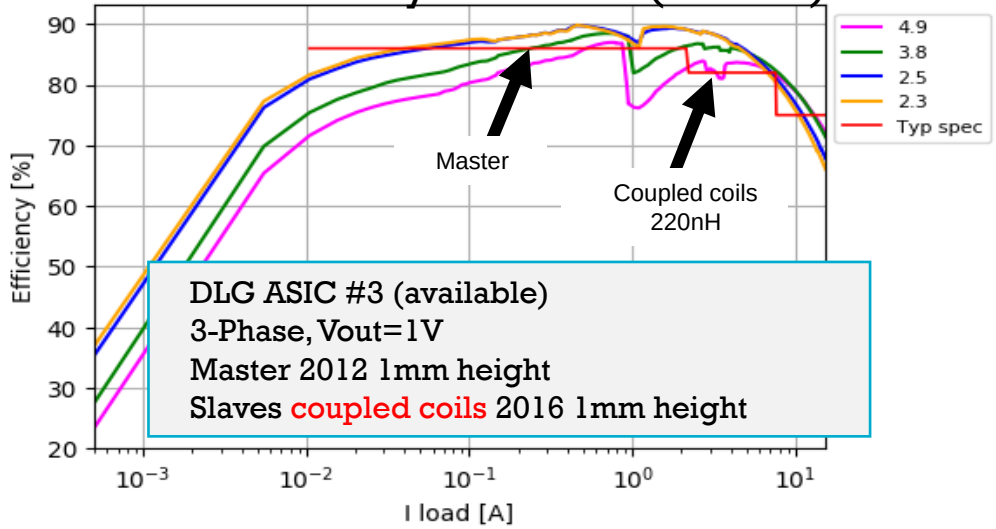


DLG ASIC #2
4-Phase, Vout=0.775V
Master 2012 1mm height
Intermediate 2012 0.65mm height
Slaves 2x 1608 0.65mm height

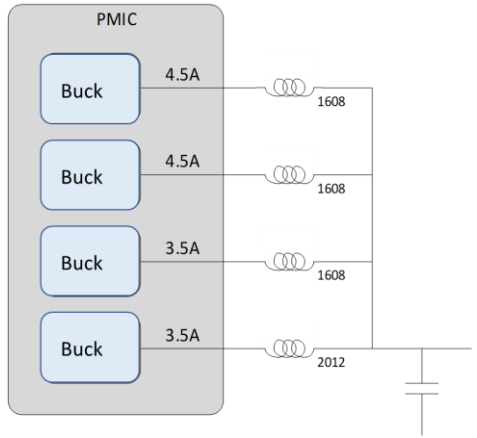
2-Phase coupled
(master phase not shown)



Multi-Phase asymm buck (c-coils)



DLG ASIC #3 (available)
3-Phase, Vout=1V
Master 2012 1mm height
Slaves coupled coils 2016 1mm height



DLG Solutions: Architectures for **performance** requirements

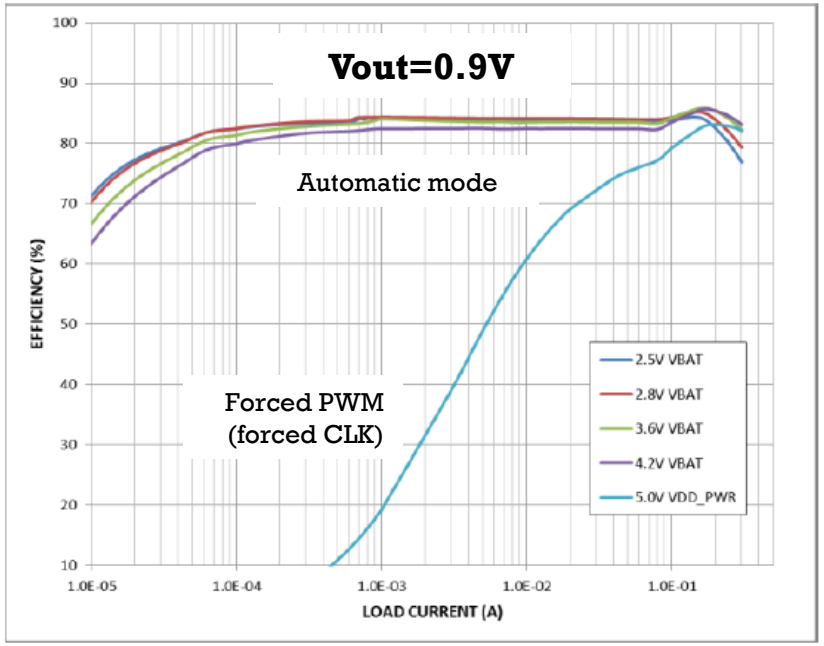
Ultra-low-IQ PMIC

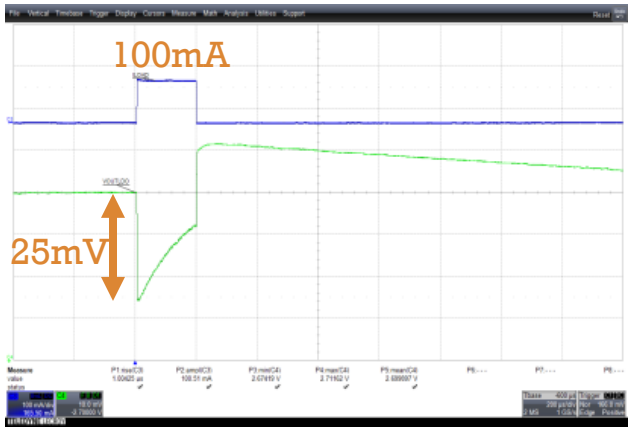
- Bucks:
  - **600nA**
  - **>80% efficient at 10uA load, 1.8V, 3.3uH, 10uF**
  - Programmable VOUT 0.6V to 1.9V, IOUT 300mA
  - ±2.5% Output Voltage Accuracy
  - Dynamic Voltage Scaling (DVS)
  - 20mV Load transient response 0-50mA t_R=1us

- LDOs:
  - **300nA**
  - **25mV load tran (0-100mA, trise = 1us)**
  - Programmable VOUT 1.8V to 3.3V, IOUT 100mA

- **Design techniques:**
  - Dynamic bias
  - Feedforward paths (transient)

- **Process technology**
  - Leakage control
  - IQ vs size: compact device



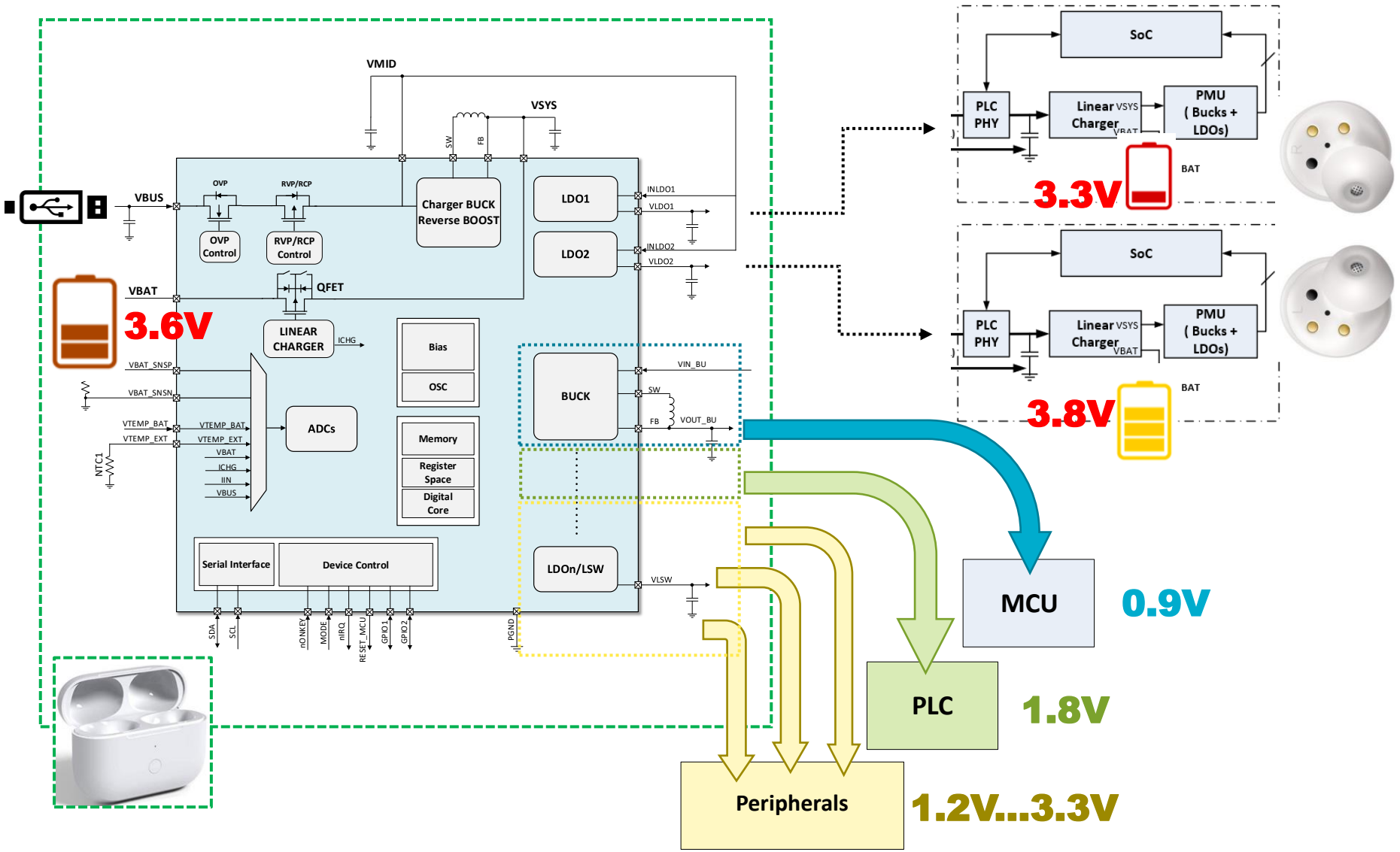


COUT=1uF, PW=200us, VIN=3.8V, VOUT=2.7V, room temp

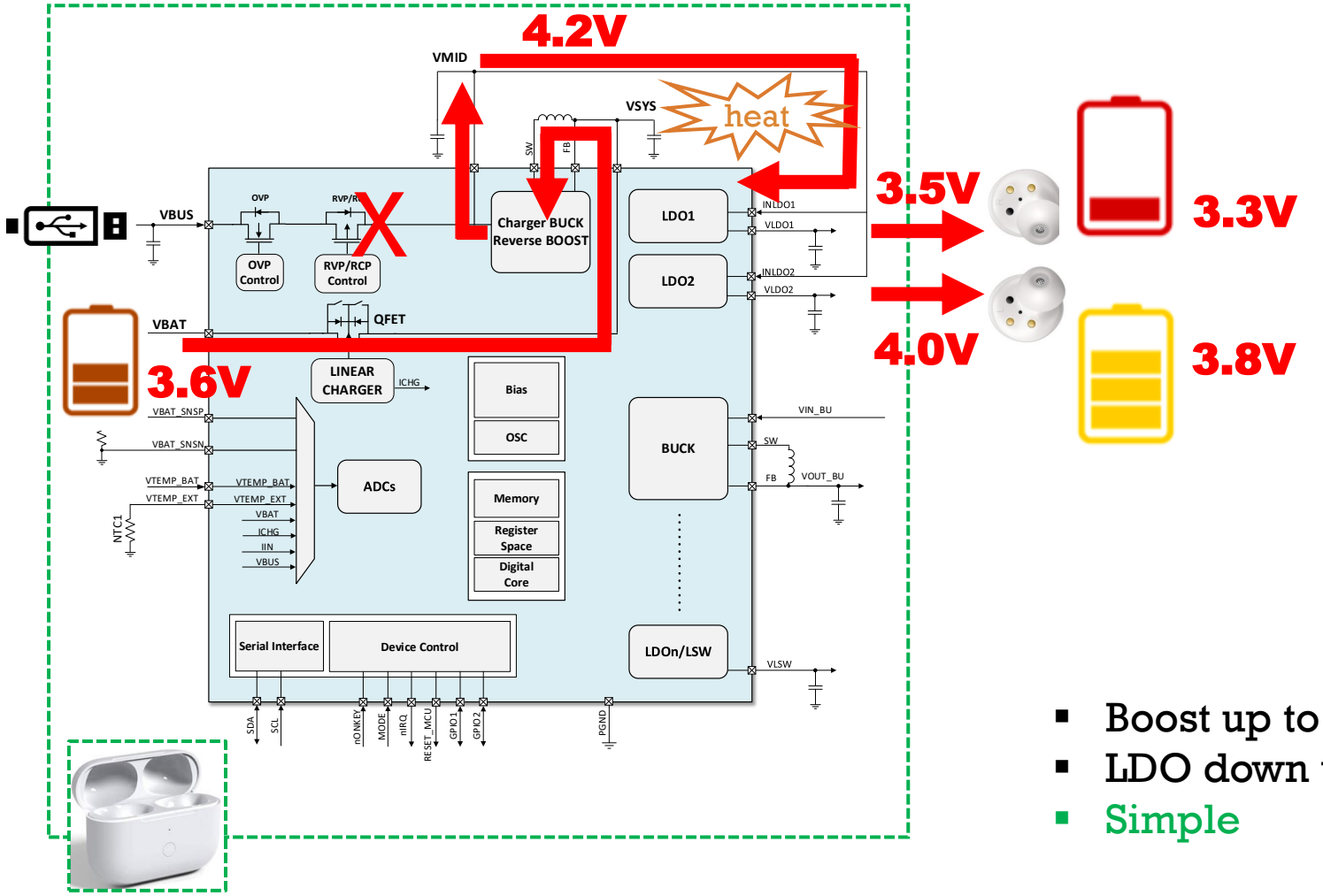
DLG Solutions: Architectures for **voltage** requirements

- Trend: power-tree tend to move from pure Buck to Buck-Boost
- Mostly driven by system with multiple batteries, example wearable TWS (charging case + earbuds)
- Driven by Li-Ion batteries min transient voltages (i.e. 2.0V) while analog sensors voltage don‘t scale (i.e. CMOS camera Vpixel 2.85V)
- Stable voltage (no OV/UV/glitches) during mode transitions.
- Challenges to optimize area/Iq of loop control for Buck-mode, Boost-mode and Buck-Boost-mode.
- Challenges of die-size (+50% switches, additional control loop circuitry)
  - Push on technology to optimize FETs FoM (mOhm*mm2)

DLG Solutions: Architectures for **voltage** requirements. Example TWS

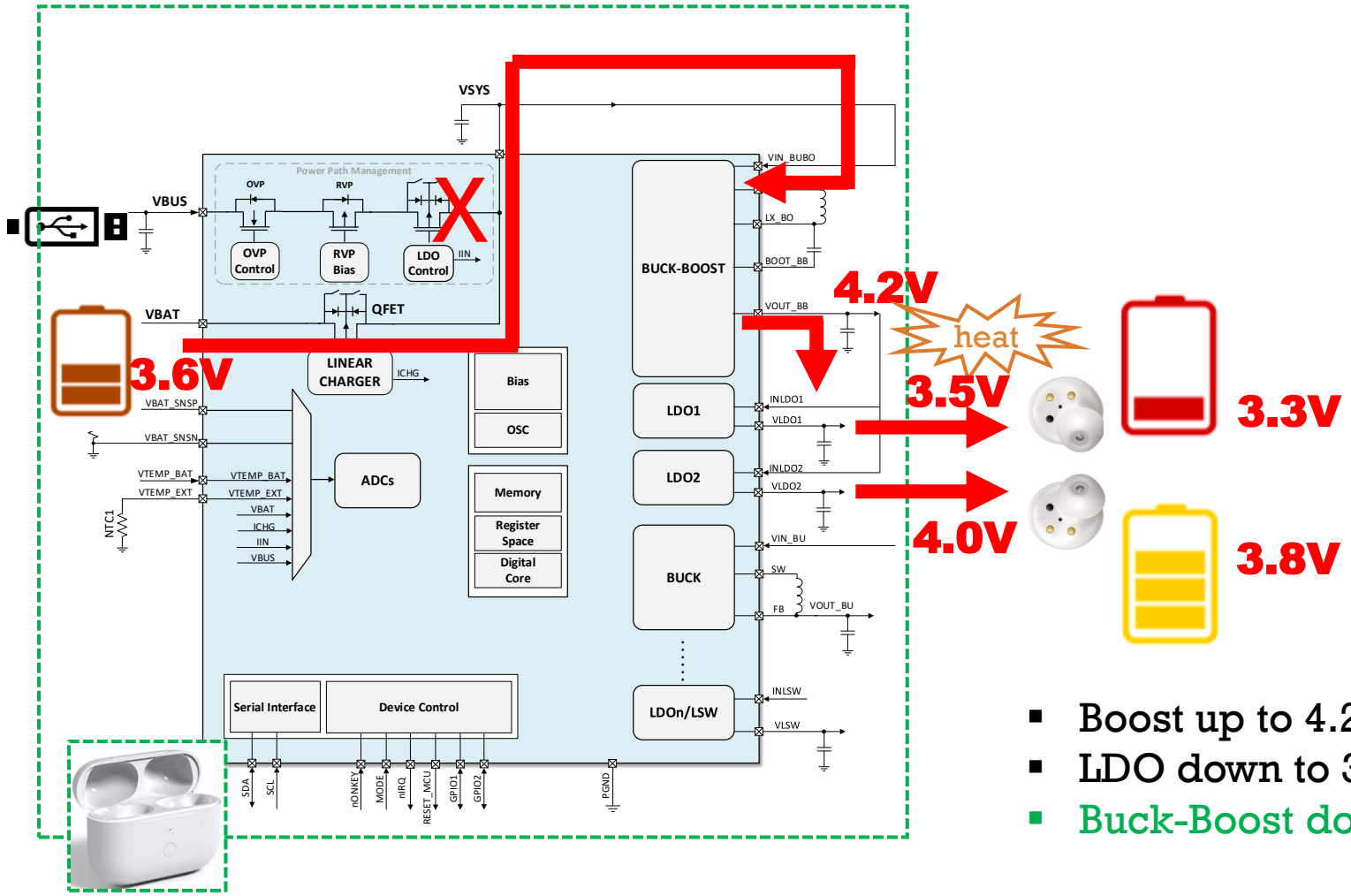


Charging TWS batteries (charging case and earbuds) - I



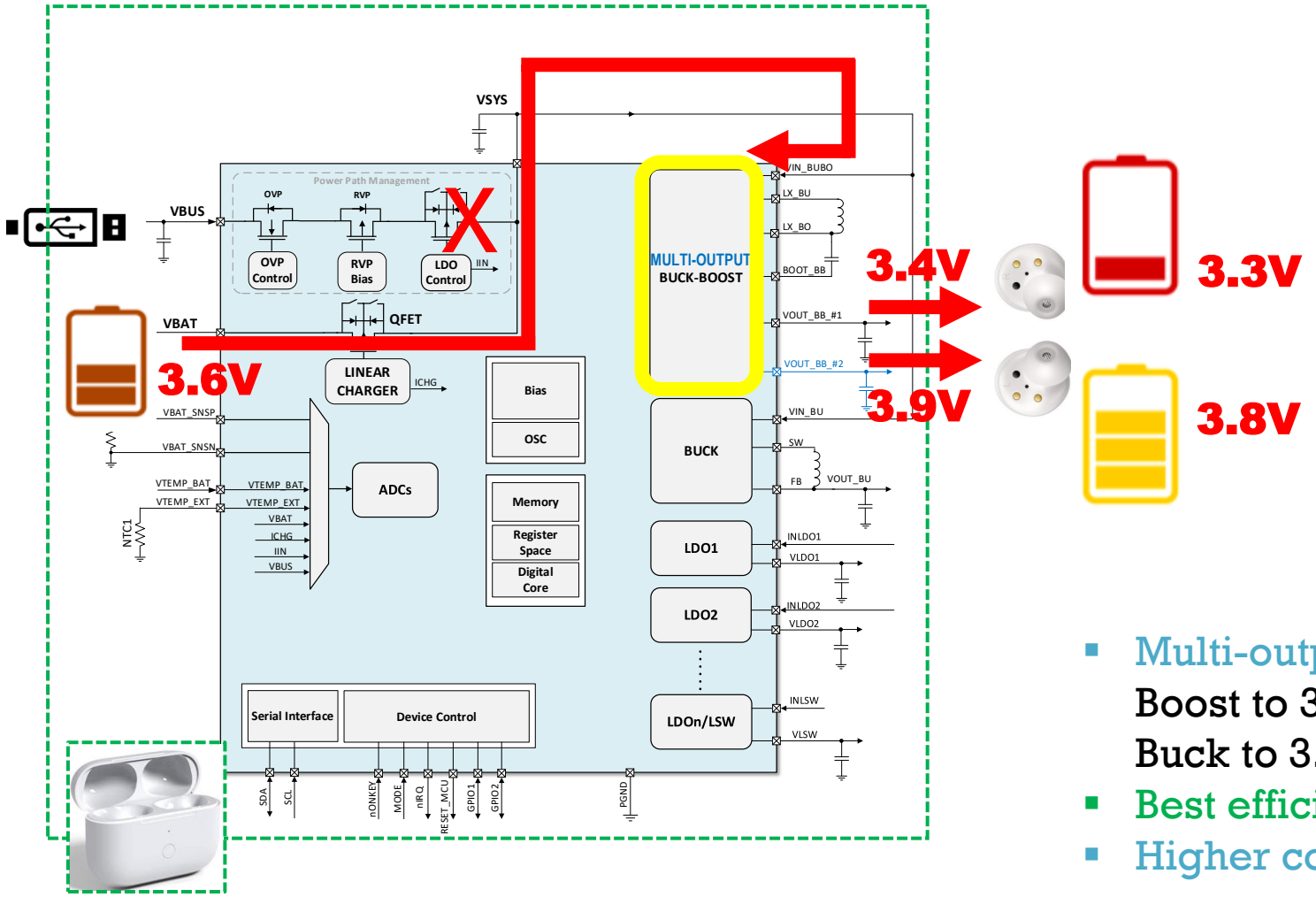
- Boost up to 4.2V
- LDO down to 3.5-4.0V (efficiency, heat)
- Simple

Charging TWS batteries (charging case and earbuds) - II



- Boost up to 4.2V (via Buck-Boost)
- LDO down to 3.5-4.0V (efficiency, heat)
- Buck-Boost down if VBAT=4.3V or USB

Charging TWS batteries (charging case and earbuds) - III

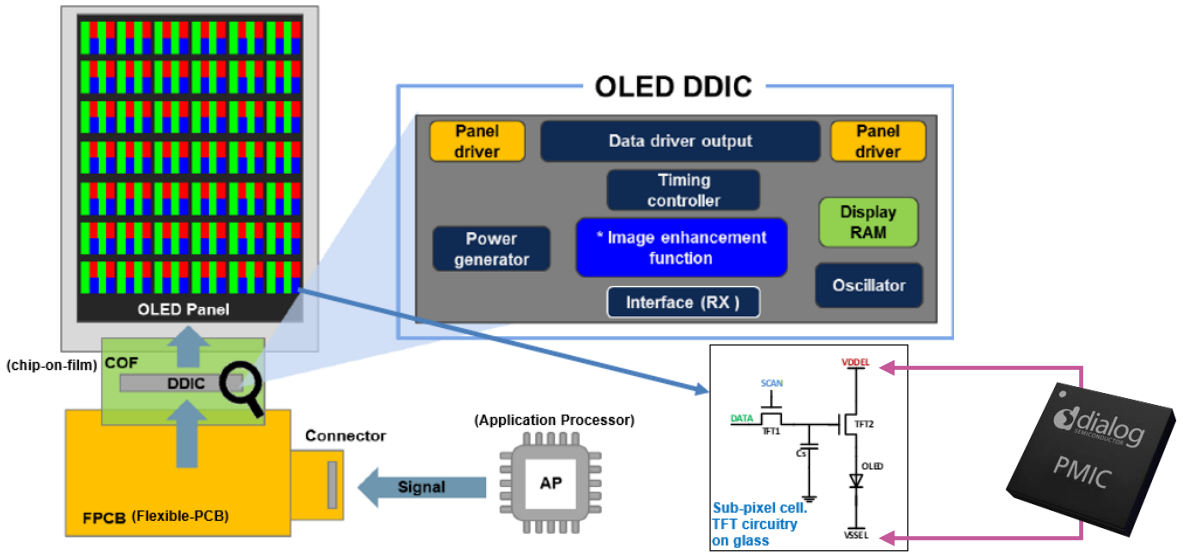


- Multi-output BuckBoost:
  Boost to 3.9V (via Buck-Boost)
  Buck to 3.4V (via Buck-Boost)
- Best efficiency
- Higher complexity

DLG Solutions: Architectures for **voltage** requirements

Negative voltages for OLED Displays

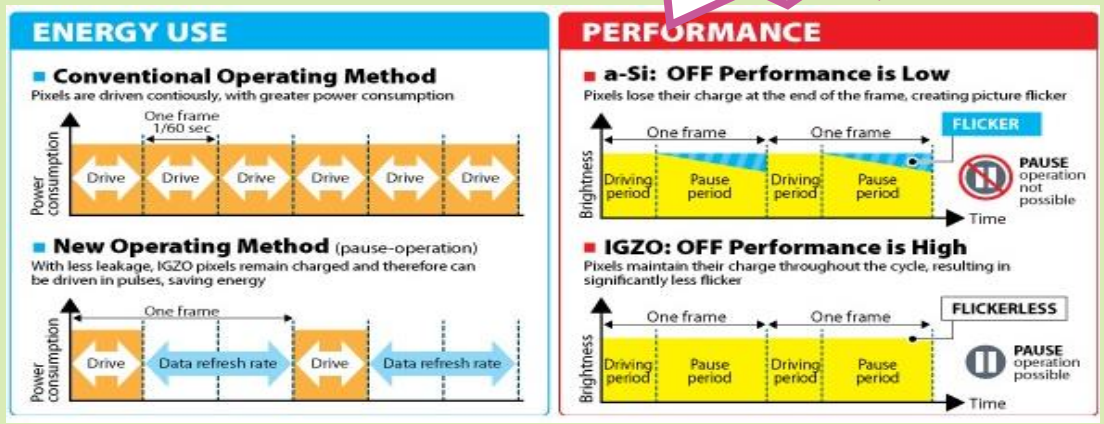
Vout [V]	Iout [A]	Pout [W]	Note
-1...-15	0.2...1	5...10 (from neg rail)	Eff >90% @3.8 Vin, -5 Vout Single phase and multi-phase



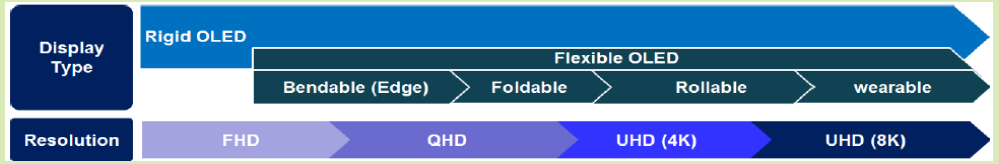
Display PMIC is often a Chip-On-Film:
PDN + pulsed loads is a challenge
(over/under-shoots, stability, etc.)

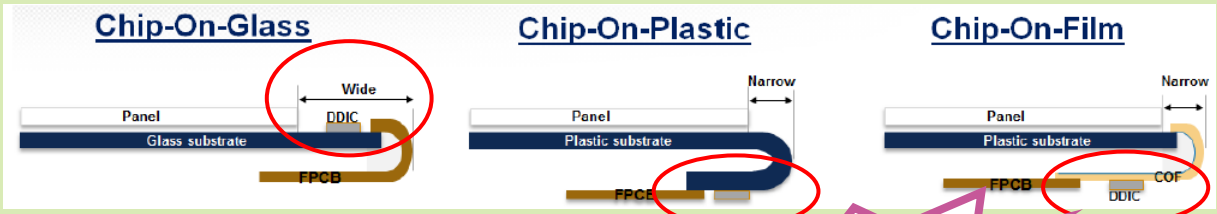
Low-leakage
IGZO TFT: pulsed
load 0-100%

#1 Pixel technology



#2 Panel substrate technology

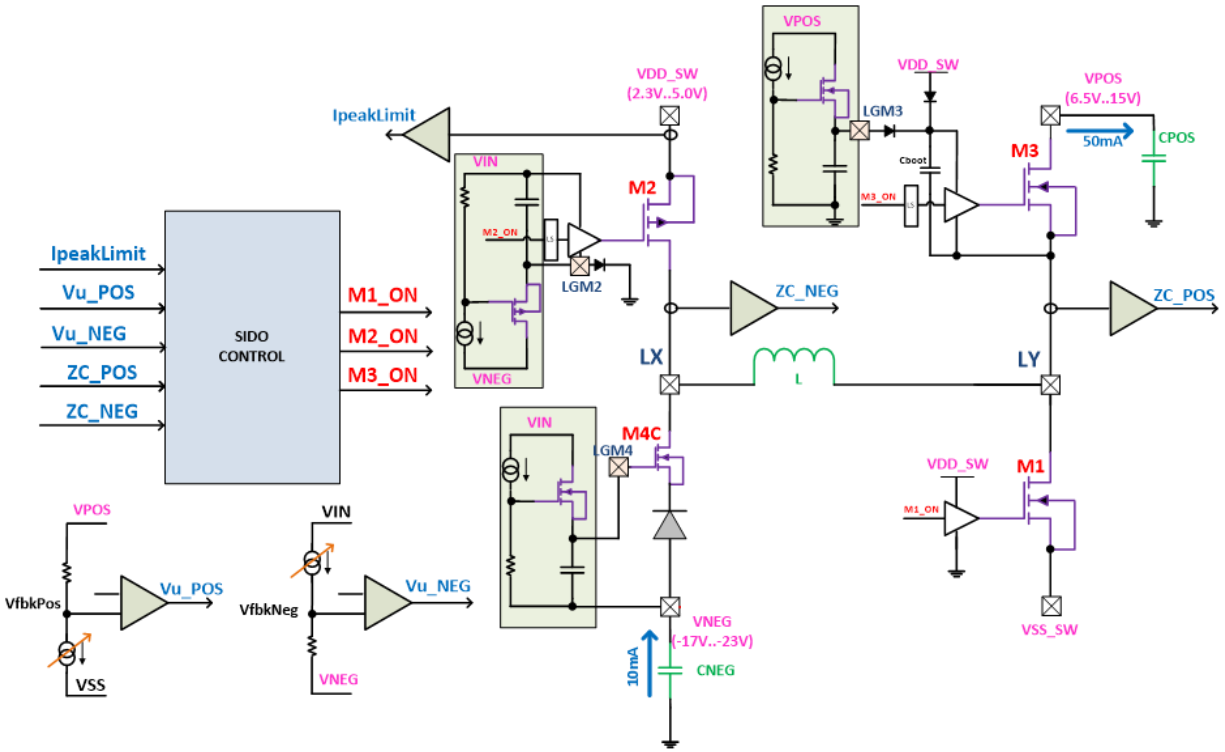




CoF: Input &
output PDN

DLG Solutions: Architectures for **solution** size requirements

Single-Inductor-Multiple-Output Architectures (i.e. positive/negative boosted rails)



Key Features

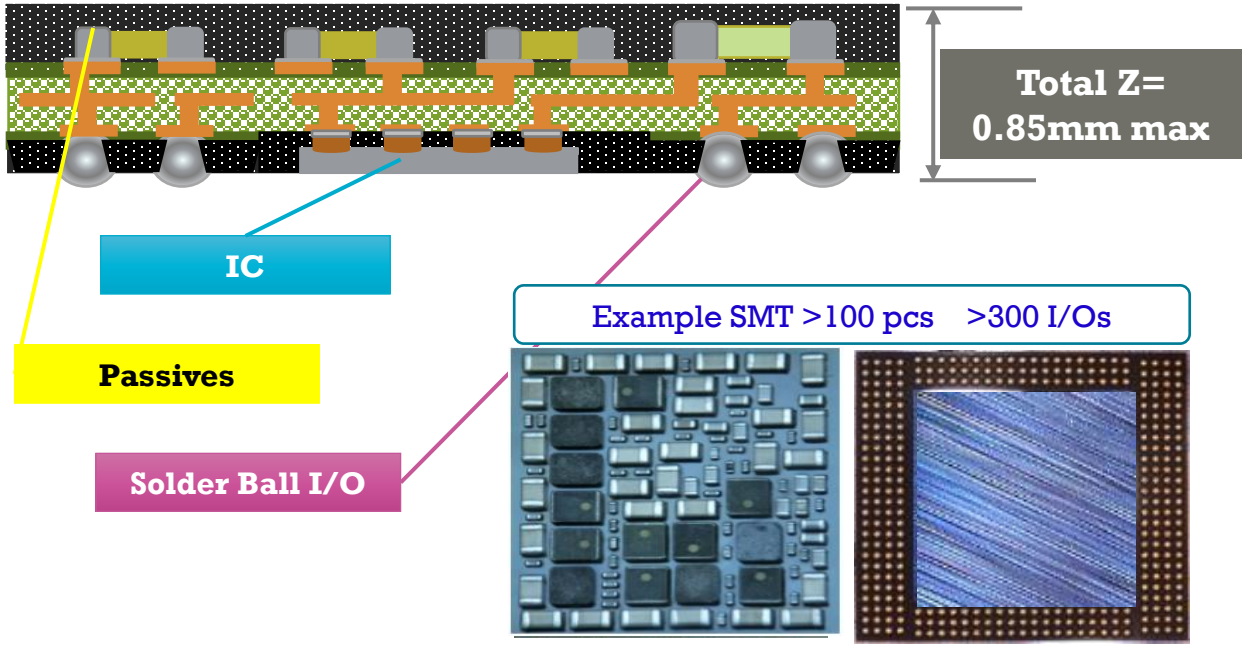
- DLG SIMO BOOST IP generates one positive boosted rail and one negative boosted rail using a single coil.
- Minimum BOM and independent programmable outputs range. Example IP:
  - **VPOS = 6.5V to 15V @50mA**
  - **VNEG = -10 to -15V @10mA**
- Full H-bridge.
- Current limit adaptive with conditions for ripple optimisation.
- SIMO BOOST IP portfolio expands to 2X VPOS boost and 2X NEG boost, 4X SIMO

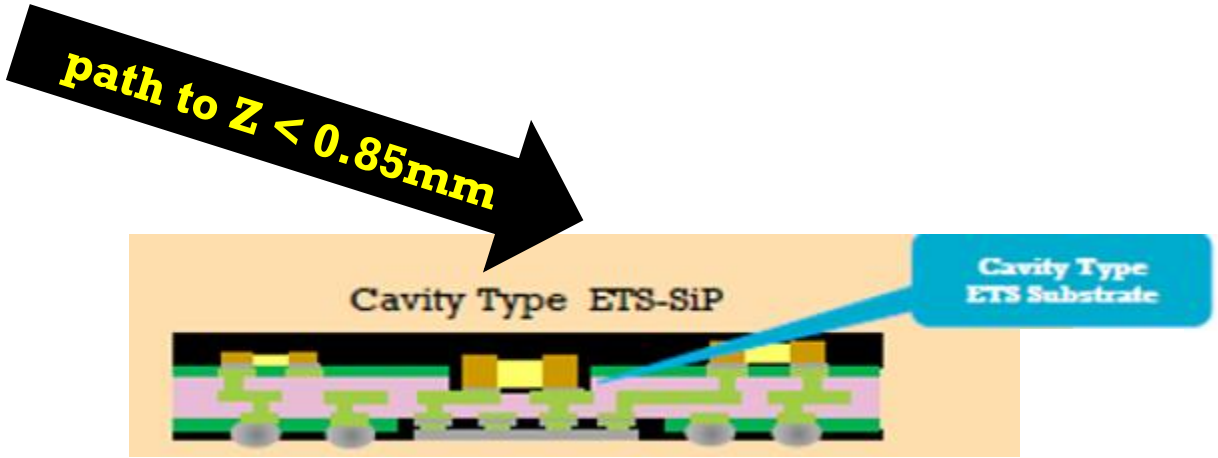
Solution size requirements: **integrated PMICs in package**

- Opportunity for integrating passives as packaged solution rather than monolithic solution
- Total height to be <0.85mm or <0.65mm

Package Passives

- Require low AC losses: to minimize AC losses, higher inductance in smaller volume is required
- DLG offer ETS 2.5D & eWLP SiP solutions
- **Cross-section of DLG ETS 2.5D SiP** (US Patent Appl. 15718080, DE Patent Appl. 102018207060.1)





DLG Solutions: Architectures for **cost** requirements

Cost targets

- Competing with stand-alone regulators
- LDO ~0.01-0.02 USD optimized for low cost
- DC/DC ~0.05 USD optimized for low cost
- Power sequencing moves from MCU to PMIC → not always accounted for when calculating solution cost (SW footprint, MCU wake-up energy)

- Strong push on Process Technology with high-performance FETS (Rdson, FoM, BV)

- **Add value: integration of more features into single ASIC (power, charging, sensing, fuel-gauging)**

DLG technology portfolio: DC/DC **bucks**

Best suited for Wearable

Best suited for other applications

Nano Iq
Ultra-low quiescent current
Good efficiency and load transient performance at low loads

Multi-phase Coupled Coils
Very good transient response
Superb current-density

Peak-Valley
Flexible buck supporting reduced BOM with good load-transient

Voltage Mode
Very good current-density
Very high per-phase currents reduce BOM and cost

Multi-phase Integrated Regulators
Allows superb regulator bandwidth enabling DVS load tracking
Supports SIP power solutions

Reduced Area
Reduced area buck with support for reduced BOM

Voltage Mode
Very good current-density
Allows very high per-phase currents to reduce BOM area and cost

Current-Mode
Dialog standard buck
Highly customisable
Up-to 3A per-phase at up-to 3MHz

Current-Mode Multi-phase
Better balance of low-load efficiency with load-transient performance. Excellent current-density

PFM-only
Small footprint for wearables
Asynchronous PFM

Current-Mode Multi-phase Asymmetric-coils
Dialog's most flexible architecture

Low Cost | Reduced BOM | Efficiency

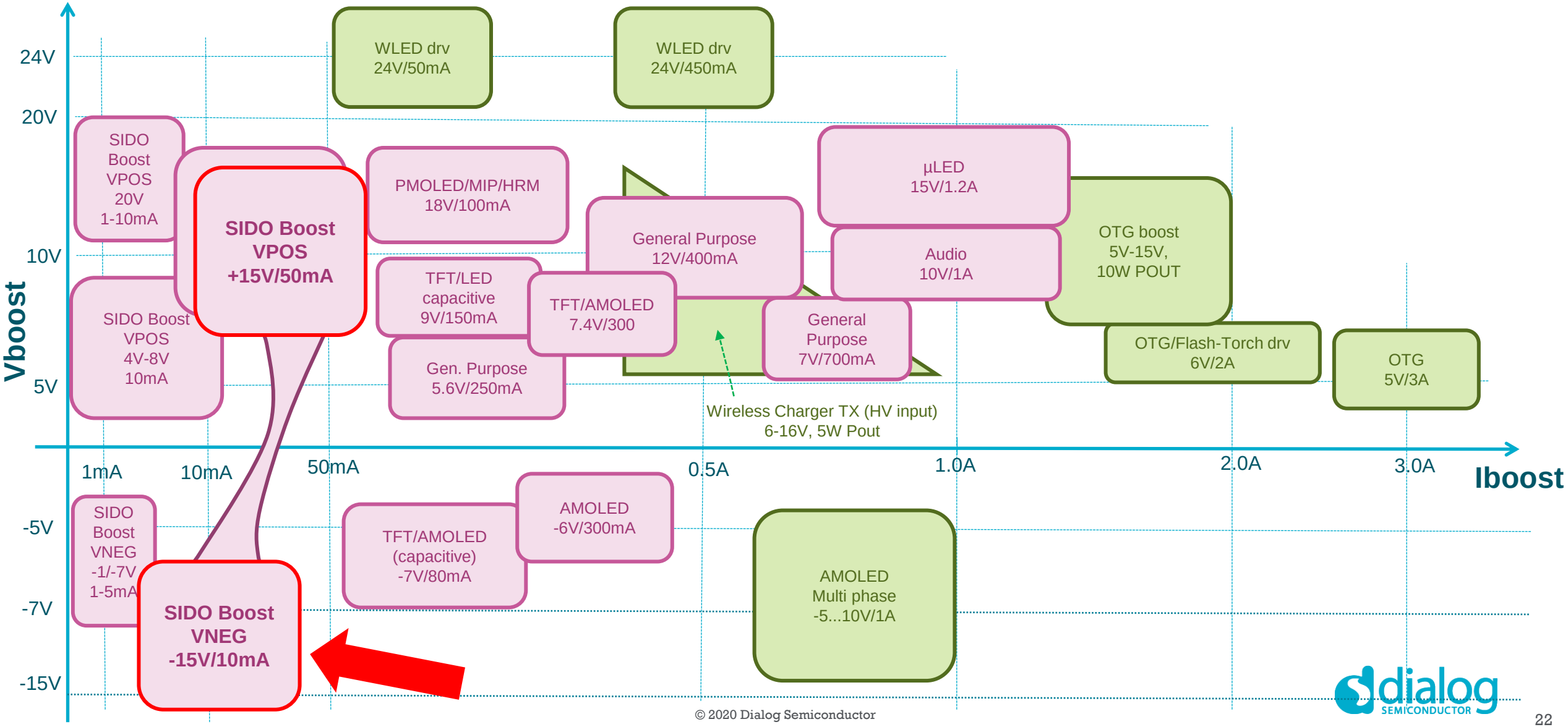
Reduced BOM | Performance

100mA 1A 10A

DLG technology portfolio: DC/DC **boosts**

Best suited for Wearable

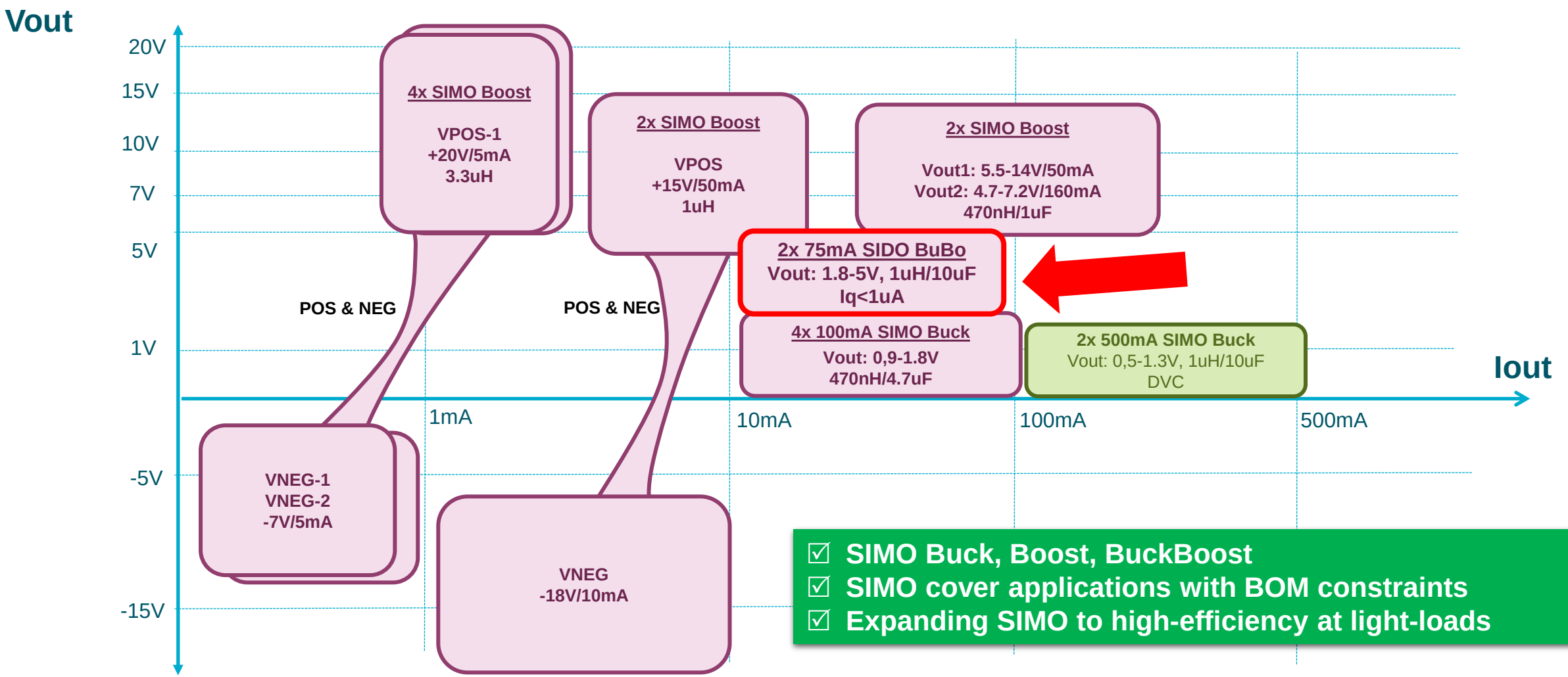
Best suited for other applications



DLG technology portfolio: **multi-output** DC/DC

Best suited for Wearable

Best suited for other applications

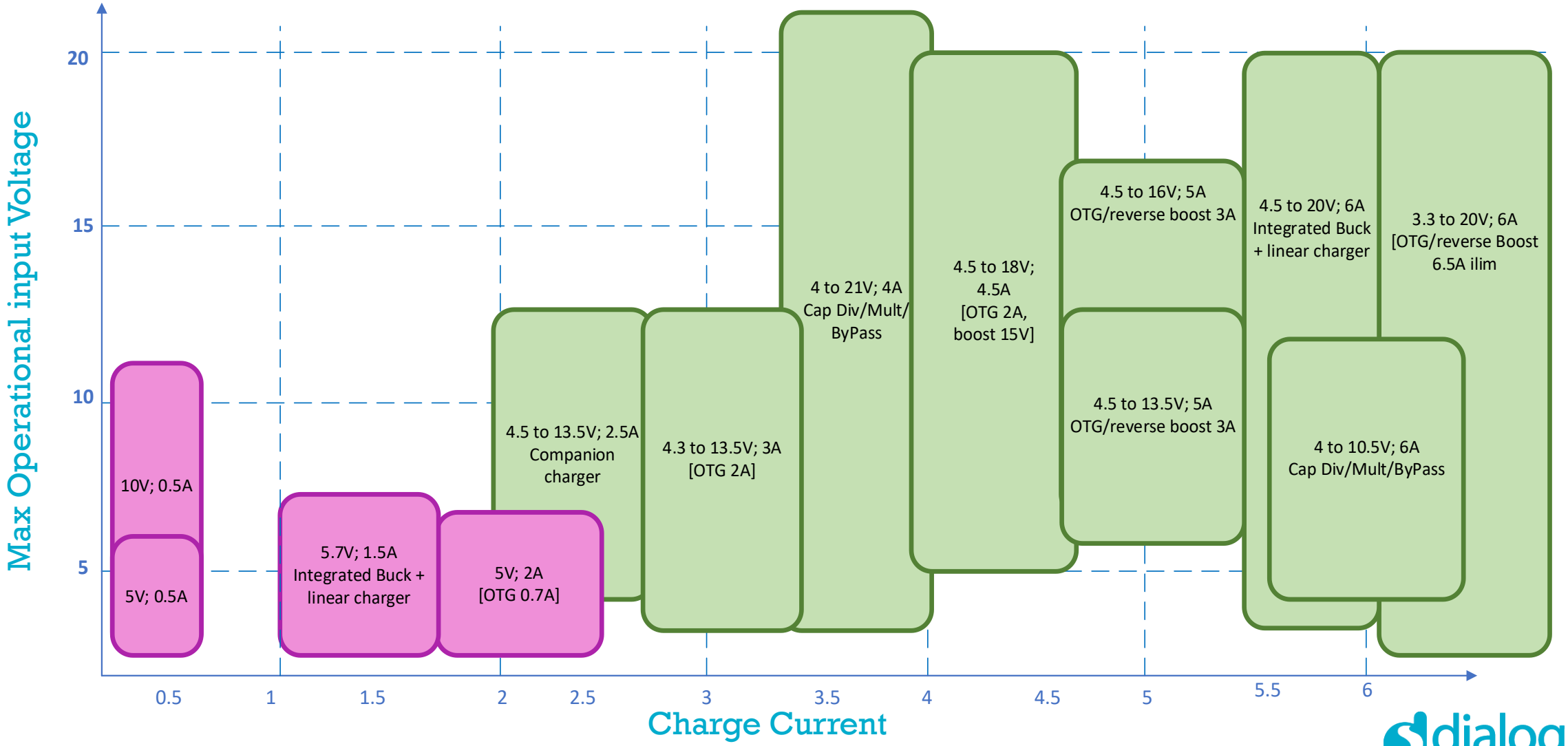


- ☑ SIMO Buck, Boost, BuckBoost
- ☑ SIMO cover applications with BOM constraints
- ☑ Expanding SIMO to high-efficiency at light-loads

DLG technology portfolio: DC/DC **battery chargers**

Best suited for Wearable

Best suited for other applications



Thoughts on Future

Wearable requirements driving the need for integrating functionalities & components in PMICs

- System level approach required to address this challenge of highly integrated PMICs
  - Novel architectures - multi-phase (uncoupled, coupled), ultra-low-Iq, SIDO, SIMO
  - Novel functionalities – SIMO, negative supplies
  - Novel external components - low profile, low loss passives
  - Novel integration technology – Ultra-thin 2.5D System-in-Packages

- DLG developing innovative solutions to address all aspects of Wearable PMICs
- DLG working with external partners to develop new passives with improved loss performance, power densities

Open challenges for future

- Increase output power with reduced solution size
  - Hybrid architectures - DLG novel “hybrid“ inductive/capacitve solutions (patents pending)
- Trade off between higher integration vs performance vs costs
  - Adding value to integrated PMIC

Powering the Smart Connected Future

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