Prospective Applications for PwrSoC

Magnetics and Packaging Technologies

IEEE PwrSoC Corridor Webinar

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Revision: vsubmit2

Tyndall National Institute, Institiúid Náisiúnta
MCCI Microelectronic Circuits Centre Ireland
UCC University College Cork, Ireland, Coláiste na hOllscoile Corcaigh
Rialtas na hÉireann Government of Ireland
Tionscadal Éireann Project Ireland 2040
Ireland's European Structural and Investment Funds Programmes 2014-2020
Co-funded by the Irish Government and the European Union
European Union
European Structural and Investment Funds

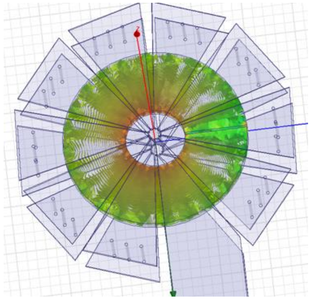
Introduction

Planar inductors for PwrSiP/PwrSoC POL or SoC iVR.

Resonant transformers for isolated bias, large step ratio POL

Gate Drivers: Isolated power and signal coupling

ULP Smart Sensor node for IoT



400 µm substrate embedded toroid

4 µm films in planar solenoid format **(MoS)**

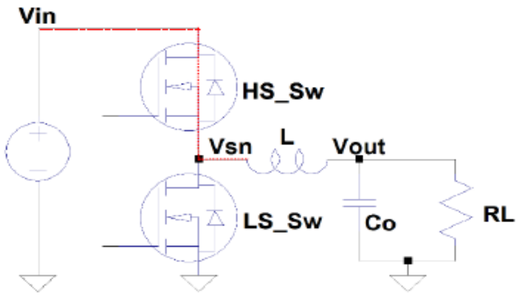
95+% efficient magnetic components, at high frequencies, to cater for deep levels of integration

Topologies & Requirements for 4 nH to 1 µH magnetising inductance

Systems Perspective: L/mm^2, Q_{AC_LS}, DCR, η_{DEVICE}, $I_{SAT,}$ $C_{CM,}$ $C_{IO,}$ $\mu_{A\_DCbias,}$ Near field/flux containment

Multi-Level Reduces Inductance Value

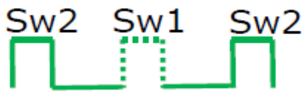
1. Typical 5 – 1V8 @ 1A POL for portable device is a 3 MHz Buck converter with 1 µH inductor; typically a multi-layer ferrite chip; 1008 case size (2.5 X 2 X 1 mm).
2. iVR for SoC inductor: a 100 MHz, 1V8 – 1V @ 0.5A requires 4 – 10 nH

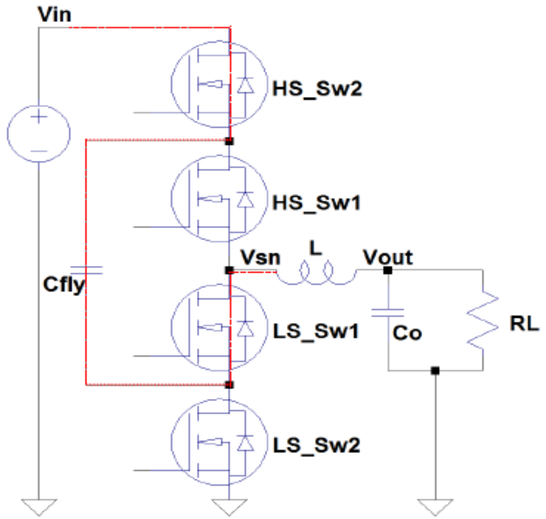


Basic Buck Converter (2-L)

Vsn (2-L)

Vsn (3-L)





3-Level Buck Converter

Cfly = Vin/2

$V_L.dt=L.di=N.A_e.dB$

Multi-Level reduces ***volt.seconds***

3-L => ½ switch node voltage

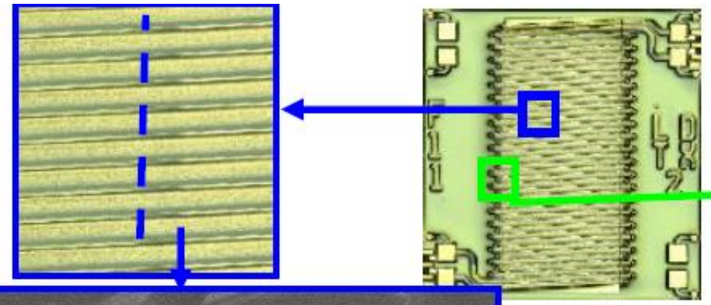
3-L => 2 X inductor frequency vs *fs*

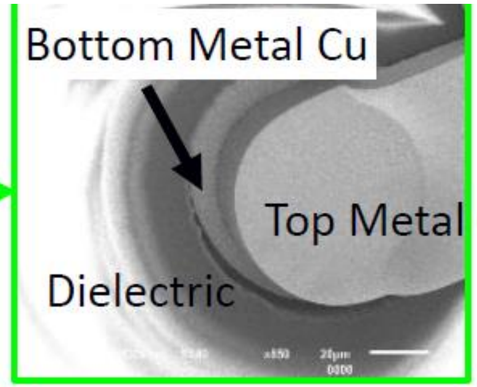
3-L => 2 X Duty Cycle – *possibly very useful for effective coupling!*

4-L => 9 X Reduction in volt-seconds and combine with resonant waveshapes => L value reduction to 10 nH demonstrated for a 5 MHz switcher[1]

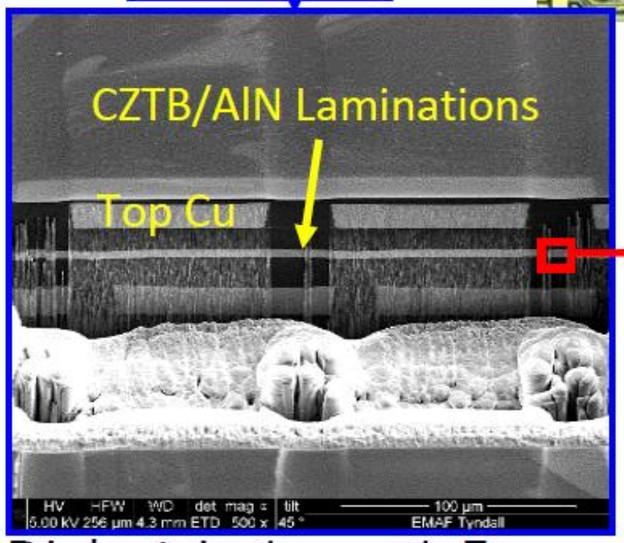
"A 93.8% Peak Efficiency, 5V-Input, 10A Max ILOAD Flying Capacitor Multilevel Converter in 22nm CMOS Featuring Wide Output Voltage Range and Flying Capacitor Precharging", Christopher Schaef et al., *ISSCC 2019, Session 8.1"*

Solenoid Micro-fabricated Device (SEM, FIB, Photo)

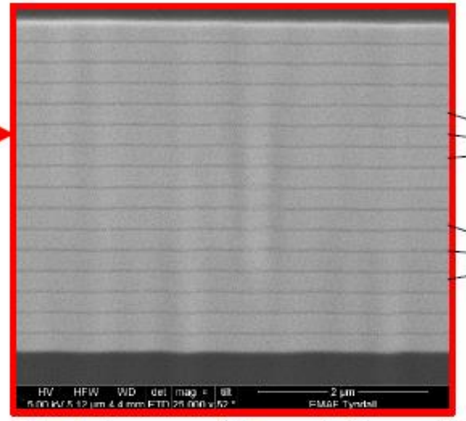




Top copper to bottom copper via connection



Top Passivation
ILD 2
ILD 1
Bottom Cu



CZTB
AlN

16 layers CZTB-AlN laminations

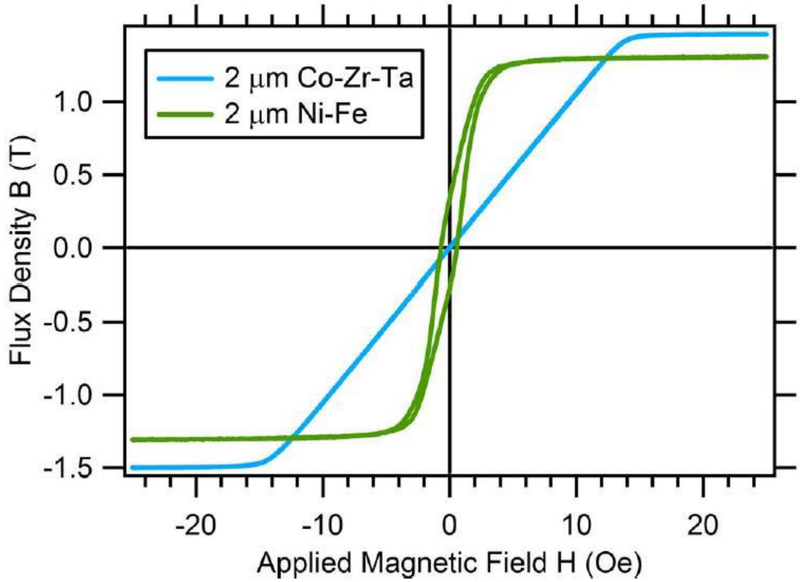
Dielectric 1 1.5um
Adhesion Layer 20nm
Laminated Core 4.8 um

Bottom Cu 16 - 18um
Top Copper 14 - 16um
Cu Via interconnect 14um

EI “MagPwr” Project CF-2017-0791-P

Cobalt Based Thin Film Devices, CZT(B)

Symbol [Unit]	No core/ Air-core	Ferrite core	Metallic thin film
μ_r	1	15 – 150 @ 10 MHz+	**100 – 700** 4 um
f_{SW} [MHz]	∞	**< 12**	10 - 200
B_{sat} [Tesla]	∞	0.1 – 0.2 @ 10 MHz+	1.2 – 1.5 @ 10 MHz+
-	Excellent	Incompatible	Compatible



- High saturation magnetisation √
- Sputtered Cobalt devices achieve adequate Q_{LS} for 95+% efficient devices over 10 – 200 MHz; 1 – 5 mΩ/nH and 10 -50 nH/mm² √

Donald S. Gardner et al. (INTEL)
Review of On-Chip Inductor Structures With Magnetic Films
IEEE TRANSACTIONS ON MAGNETICS, VOL. 45, NO. 10, OCTOBER 2009

- Best ferrite power devices really struggle above 10 MHz. CZT good to 100+ MHz √
- CZT devices increase L density by 6X (< ~ 10 nH) and 20X (> ~ 100 nH) over air-core √

2-L 5V @ 30 MHz with 50 nH Inductor

Tyndall fabricated 50nH, 80 mΩ inductor presented at IEEE PwrSoC 2018, [2] P. Podder et al.,

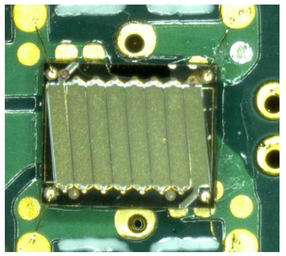
Solenoidal inductors are high Q, because of the “air-gap” portion (excl. adjacent eddy losses). Slightly higher than projected for race-track, [1] Jaime Lopez et al.

Device in 2-L (1-ϕ) Buck Converter @ 30 MHz

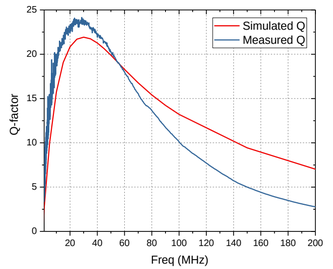
3.45 V to 1.45 V @ 0.5 A = 81 %,

Inductor Loss =4.31%

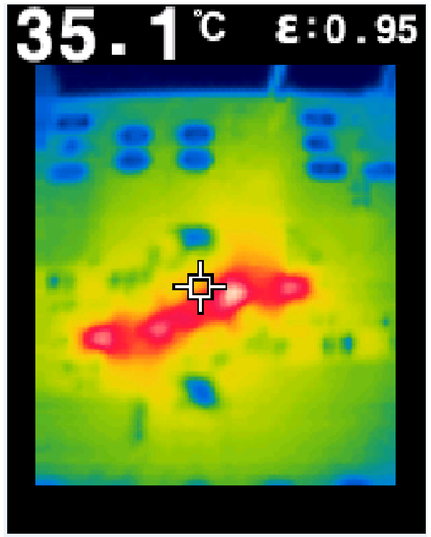
DCR Loss = 3.4%, AC Loss = 0.91%



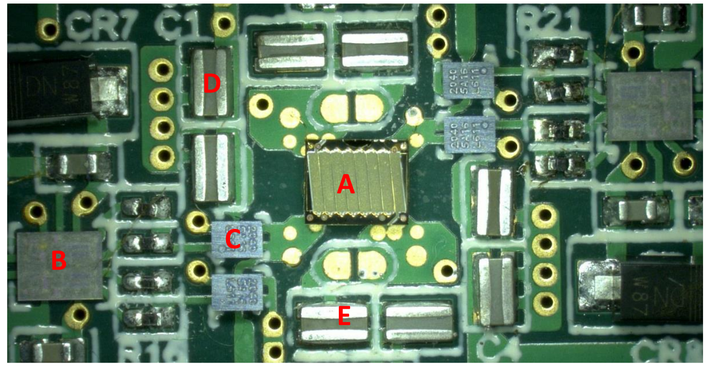
50 nH thin film CZTB
2 X 1.8mm



Qss = 24 @ 30 MHz



2 –ϕ Unit: inductor does not show on heat map



Symmetrical 2-Phase Buck Converter
A. Thin Film CZTB 50 nH on Silicon
B. Murata-Peregrine-Semi PE29102 Driver
C. EPC 2040 eHEMT GaN 24mΩ Switches
D. Input Capacitors (0306 – low ESL)
E. Output Capacitors (0306 – low ESL)

L	50nH	B_{SAT}	1.2T
DCR	125mΩ	I_{SAT}	0.9A
Core Thickness	4 µm	SRF (FMR)	300MHz
Material	CZTB	C_{SELF}	3pF(1GHz)
CZTB Lamination	250nm	Cu	15µm
Q_ss_peak	24		

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EI “MagPwr” Project CF-2017-0791-P

Single Inductor Solenoid: Q scaling

Table 1 Design specifications for single and coupled inductors and transformers

Device type	Device ID	Parameters			
		L [nH]	k12	Footprint [mm^2]	f_{SW} [MHz]
Single inductor	SL1	10.4	-	0.5	40
	SL3	105.7	-	2.1	40
	SL4	243.4	-	4.1	40
Coupled inductor	CL2	53.6	0.7	2.6	40
	CL3	104.6	0.8	4.4	40
Transformer	TX1	103.5	0.9	5.1	30
	TX2	40.2	0.9	2.3	30

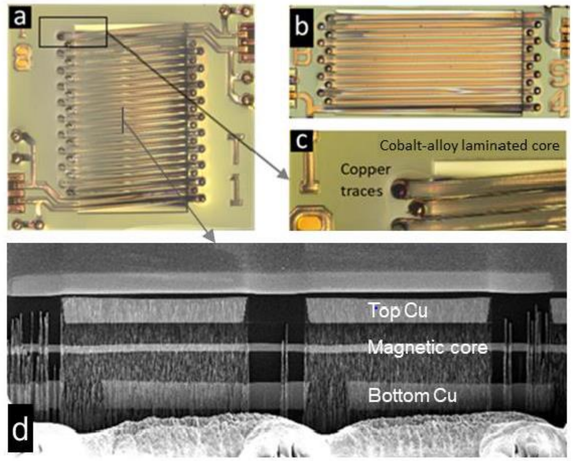
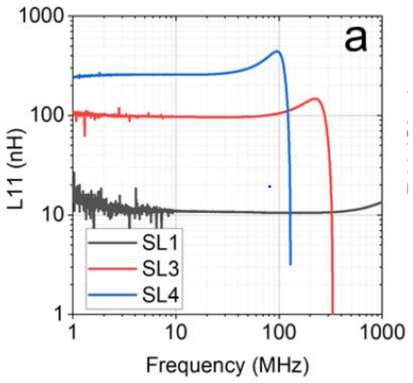
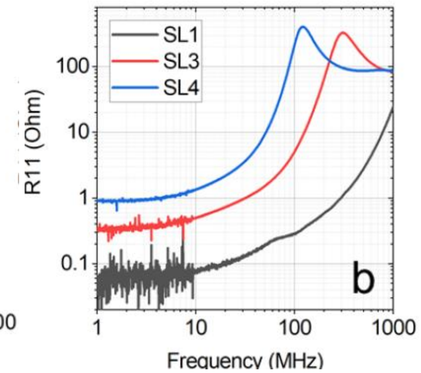
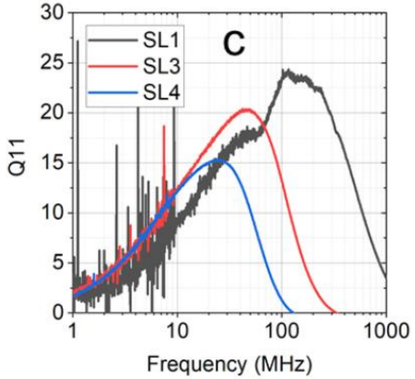
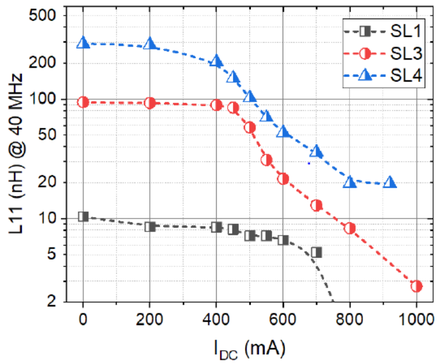


Figure 2 Fabricated devices a) Transformer, b) Single inductor, c) Enlarged view of cobalt-alloy based laminated core enclosed by copper traces in solenoid construction. d) SEM of the fabricated micro-inductors cross-section.









[3] P. Podder et al., Tyndall, Chor Shu Cheng et al., Global Foundries

- $f_{\_Qpeak}$ scales inversely with

  N or √L

  - a nice property!

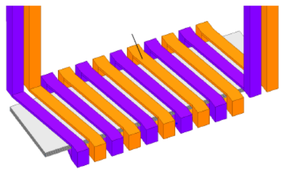
- L/DCR ~ 0.25 nH/mΩ

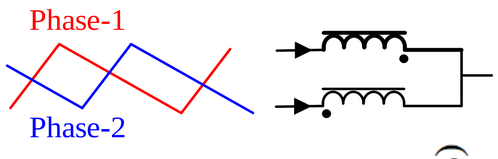
  - ~1.5% inductor DC loss for Tyndall 100 MHz 4 nH L on 28 nm CMOS

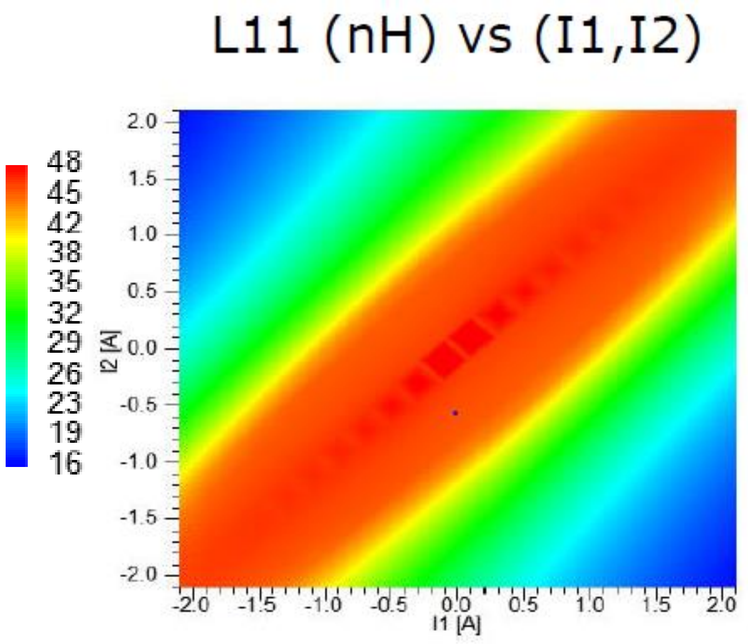
- Energy storage density is quite good and may have thicker films (2-3X 28 nm power bridge size)

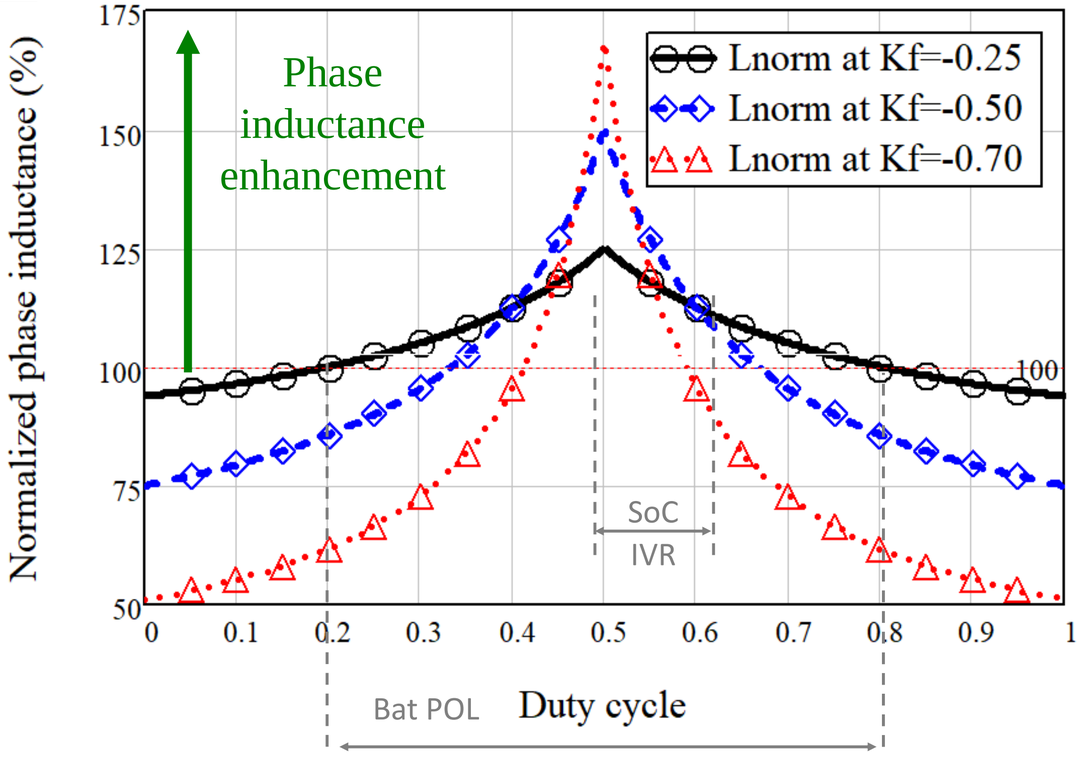
- Planar solenoids are quite a high Q structure

2-Phase Inverse Coupled Inductor



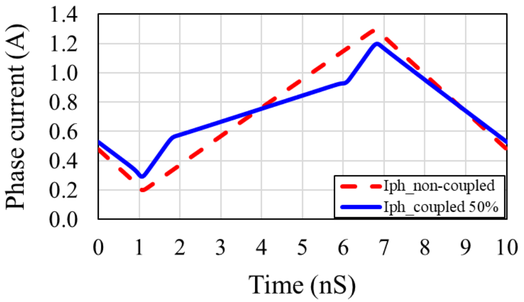




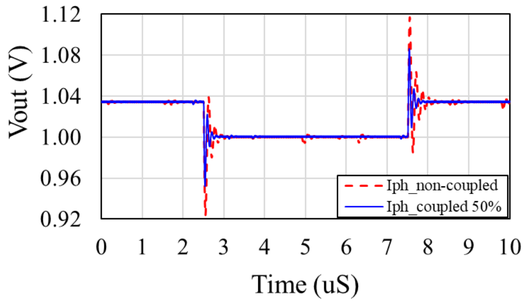


Phase current: 1.8 to 1 V

$\Delta I_{non\text{-}coupled}$=1.1A, $\Delta I_{Coupled}$=0.9A



Open loop transient response



- Considering SoC iVR and wide-input-range general purpose battery powered POL
- Reduces DC/ AC fields, size, ripple, increases L_{SS}, increases I_{SAT} , improves ΔV_{TR}

[4] Youssef Kandeel, NUIG, et al., APEC 2019

Thin Film Solenoids – Other General Observations

Q_{ls} remains flat or increases slightly with increasing DC bias √

Generally Q_{ls} remains high (>13 device Q) up to $I_{AC\_pk} > 50\% I_{SAT}$ √

For some lower inductance devices, $Q_{ls} > 80\% Q_{ss}$ @ $I_{AC\_pk} = I_{SAT}$

Practical, high-Q, inductor density (L/mm2) = X6 over air-core (tf-solenoid) for ~10 nH and X25 over air-core for ~ 100 nH √

Thin Film magnetic Layers on PCB

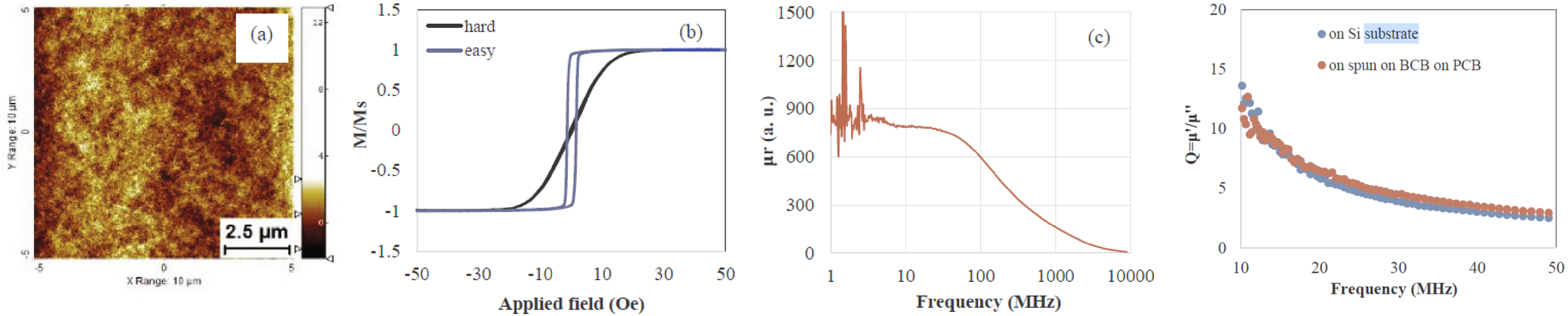


Fig. 6. (a) AFM results for BCB spun onto PCB before any deposition of magnetic material, (b, c) *B-H* loop and high frequency permeability for $Ni_{45}Fe_{55}$ deposited on BCB spun on to PCB (with O_2 treatment) respectively.

$Ni_{45}Fe_{55}$ Properties similar to on-silicon if pre-treat. Average roughness, Ra = 23 nm (PCB) vs 0.4 nm (Si)

This enables electroplated or sputtered films to be deposited on PCB with good high frequency properties

[5] Zhara Ghaferi et al., Tyndall. EU H2020 “GaNonCMOS” www.ganoncmos.eu

PwrSiP: Multi-Layer CZTB in Flip Chip PCB

Tyndall National Institute
Institiúid Náisiúnta

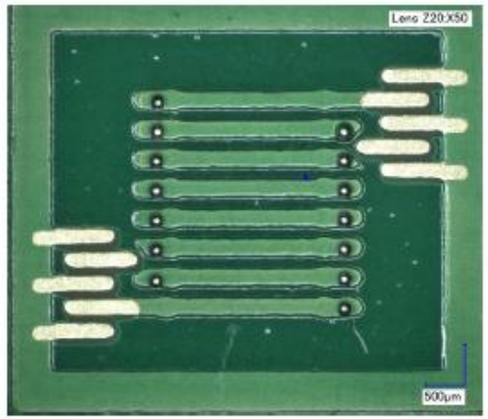
Solenoidal inductor device design

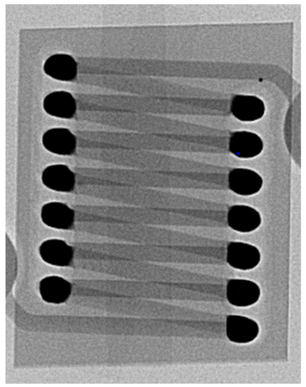
Enables 70 – 150 um Cu thickness

Retains high Q at 40 MHz (Q= 23)

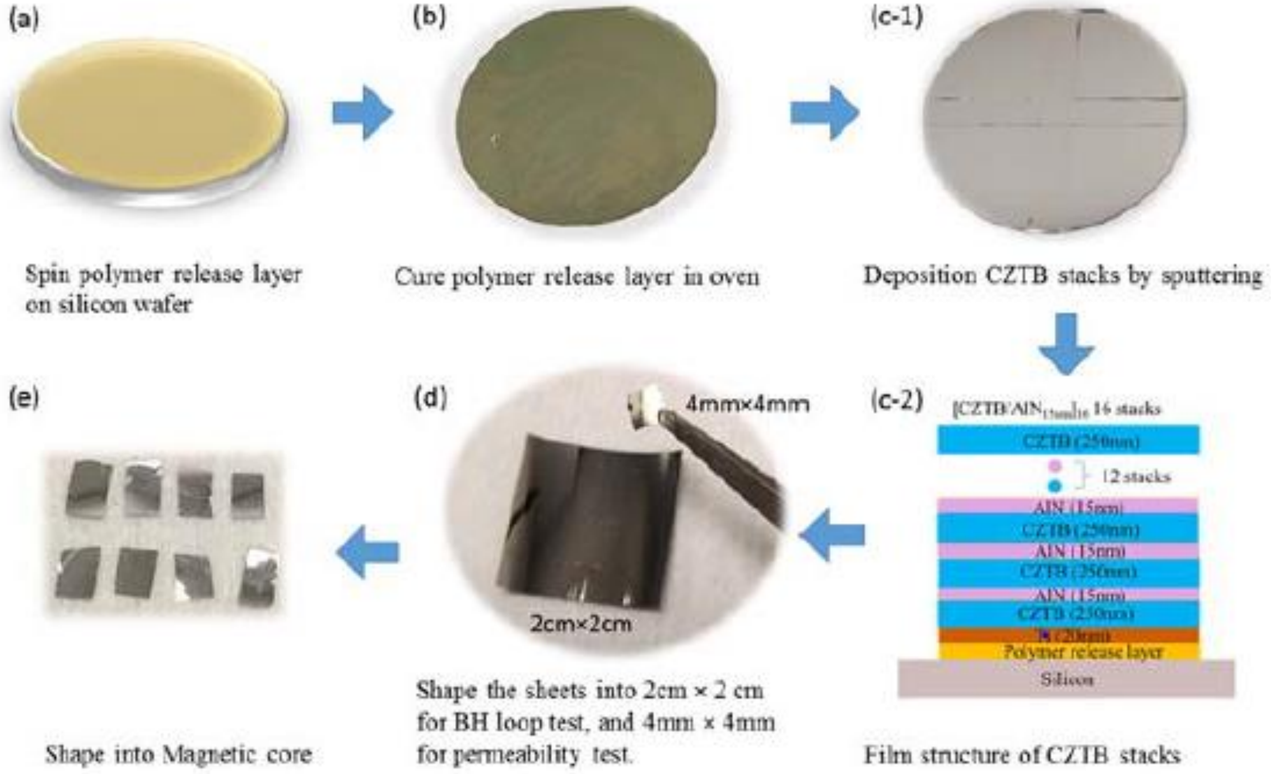
Cost effective Flip Chip approach

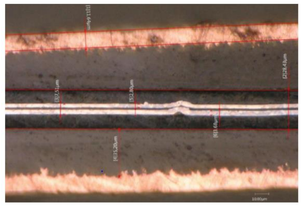
No via drill holes, Good DCR





[6] Declan Jordan et al. Tyndall 2 X 2.8 mm CZTB film





Layers	2
Layer Thickness	2 um
Layer Separation	2 um

Embedded Tyndall laminated film has passed reliability trials in GaNonCMOS program

AT&S

Co-sputtering SiO_2 and CZTB

- Increases Q – small signal >> 100 @ 300 MHz
  - (single layer films have very high μ and Q)
- Maintains well-aligned uniaxial magnetic anisotropy
- P CZTB-SiO_2 increases to 224 μΩ cm to allow higher lamination thicknesses (< skin depth)
  - Fewer laminations, lower cost
- Enables an additional control handle over permeability.
  - High frequency power ferrites achieve low loss by reducing μ_r to 15-50 range.
  - Potential advantage for closed-core (race-track)

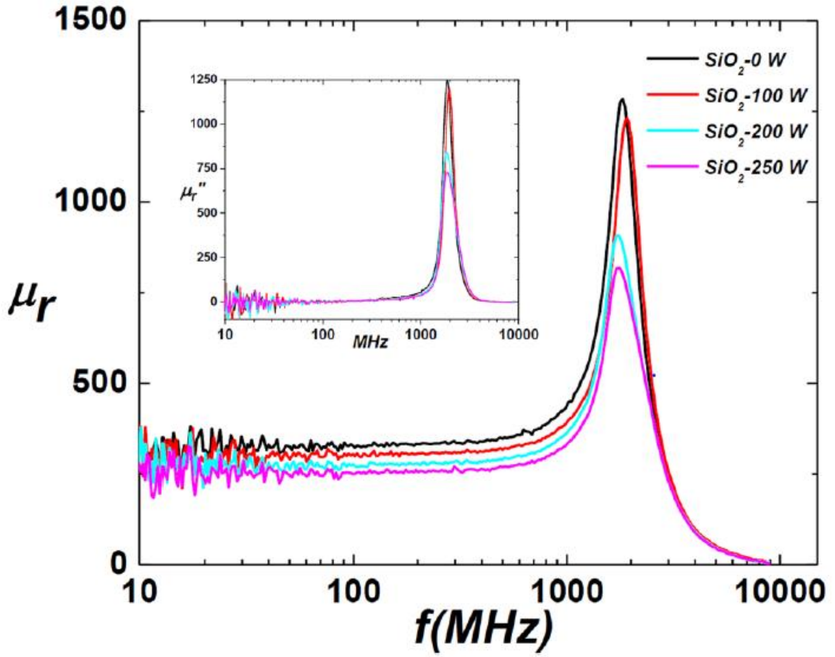


FIG. 8. The high-frequency permeability (μ_r) response of the CZTB–SiO_2 composite films deposited at different powers of SiO_2. The inset presents the imaginary part (μ'') of the films.

SFI No. R17121 "Adept" Project

[7] Darragh Cronin et al., Tyndall

Energy Harvesting, Ultra Low Power IoT Sensor Node

Majority of ULP PMICs are *Boost* and the inductor value/size is relatively huge.

> 10 µA minimum average current and smaller cycle ripple peak currents (10 -100 mA pk.)

=> 10 – 22 µH L value

Require low DCR for low voltage driving of the current ramp-up $v(t) = R.i(t) + L.di(t)/dt$

The topology for ULP requires development!

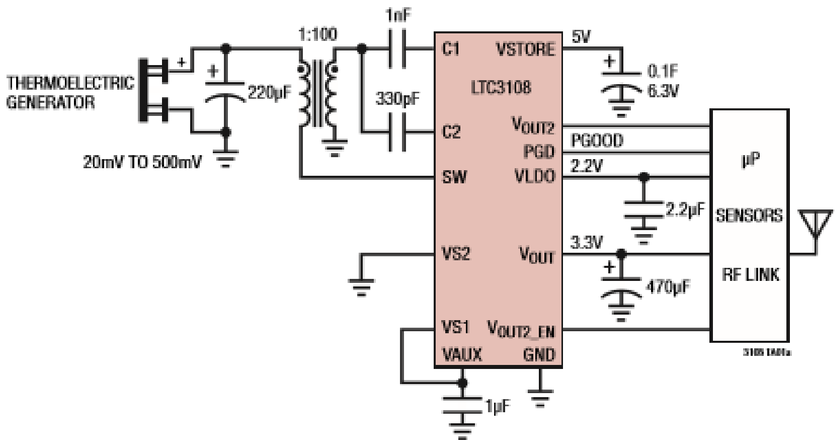
For now we will look at the cold-start challenge.

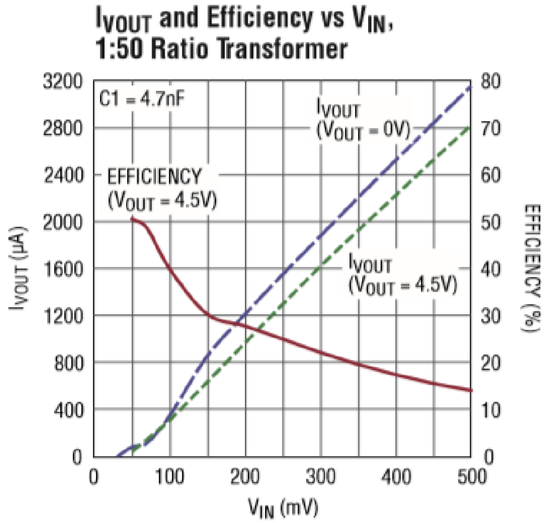
Ultra Low Power (high Rs) is desirable; 3 uW+ is commercially available (www.e-peas.com)

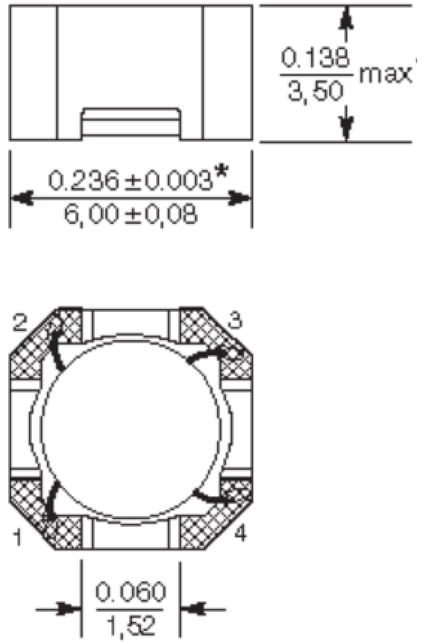
Ultra Low Voltage (for TEG) is desirable; 20 mV+ is commercially available

Commercial Low Voltage Cold Start

LTC3108







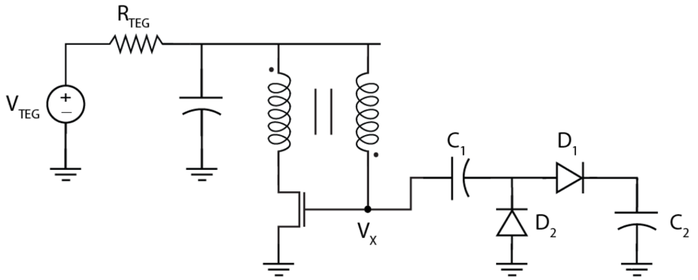
1:100 Tx => Start-up at 20mV, Iin > 3mA

f_0 recommended 10 – 100 kHz

Resonant 1:N coupled-inductor is relatively huge at **6 X 6 X 3.5** mm

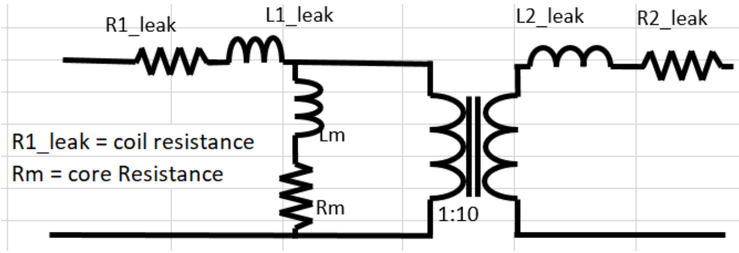
https://www.analog.com/media/en/technical-documentation/data-sheets/LTC3108.pdf

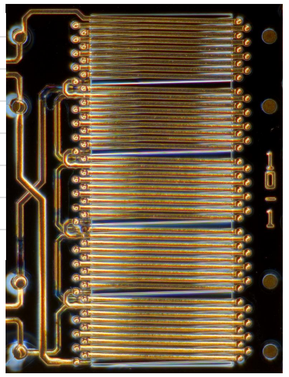
4:40 tf-MoS Meissner Oscillator based:



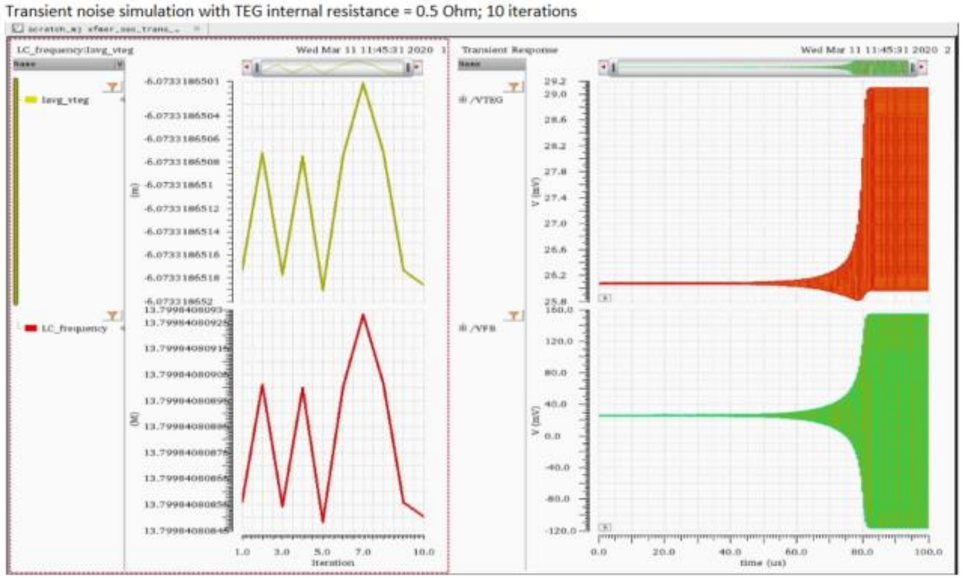
Meissner Oscillator [12]

	100 Hz	15 MHz	20 MHz
Lm [nH]	4	16.4	18.7
L1_leak [nH]	4	19.2	19.1
L2_leak [nH]	100	90	80
Rm [Ohm]	0.001	0.261	0.972
R1_leak [Ohm]	0.049	0.53	0.568
R2_leak [Ohm]	0.8	6.7	7.8





- 180 nm CMOS *simulation* using measured S Parameter Model:
  - 14 MHz = f_0
  - 4.2 mA Iin @ 30 mV (SCH)
  - 200 X 100 um Dep. Device
  - k ~ 0.65



Feature	Dimension
Cu trace width	80 um
Cu trace thickness	16 um
Via diameter	100 um
Bond-pad diameter	160 um
Die size after dicing	4 × 5.2 mm^2
Die size before dicing	4.6 × 5.9 mm^2

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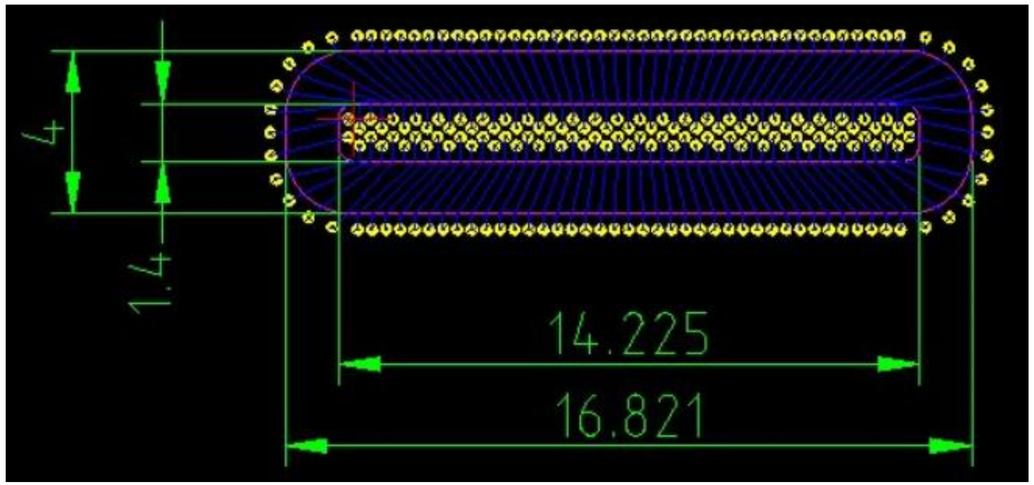
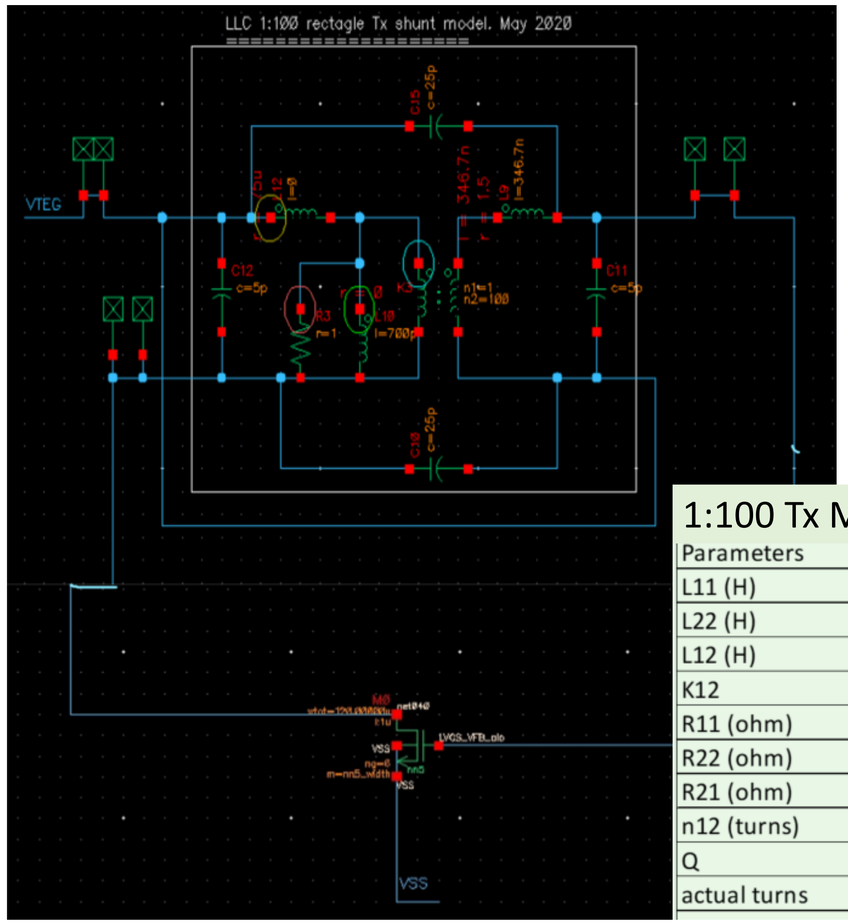
PCB Embedded Tx Meissner Oscillator





1:100 Tx Model

Parameters	
L11 (H)	6.93548E-10
L22 (H)	6.93548E-06
L12 (H)	6.5887E-08
K12	0.95
R11 (ohm)	2.25E-03
R22 (ohm)	2.33E+01
R21 (ohm)	2.18E+01
n12 (turns)	100
Q	20
actual turns	95

- 180 nm *simulation* (nn5 128x120um) using characterised device model for 1:95 Tx, 100 um film
- I_{MAG} = 2mA, Iin = 6.6 mA, 7.5 MHz, Vin= 15mV (SCH)
- Standard PCB Design Rules, 35 µm Cu
- 3M EM15TF ferrite sheet; μ_r = 150
- Very large path length, l_e !
- Single 3M film gives 5 X L_{MAG} and 3 X Size vs MoS

EnABLES EU H2020 Grant No. 730957

1:1 MoS Gate Driver Signal Tx (MoS GD Tx)

Galvanic Isolation 1 - 5 kV for Primary-Side/Functional Isolation (Operational Insulation per IEC950)

Signals and isolated bias for flying Gate–Driver/Control Telemetry in the Smart Switch Application

10 V.ns application, 40 nH L_{MAG}

48 to 1 V POL

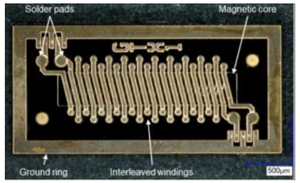
Multi-Level Converters with 20 - 200 V cells

Primary bridge drives for wireless power transfer

Resonant bias supplies

Secondary-side SR drives

Measured Tx parameters match FEM simulated



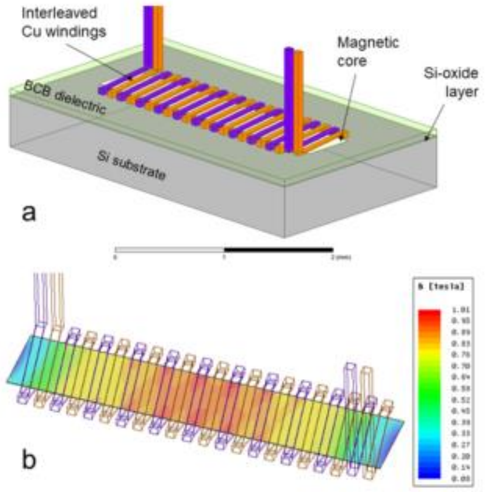
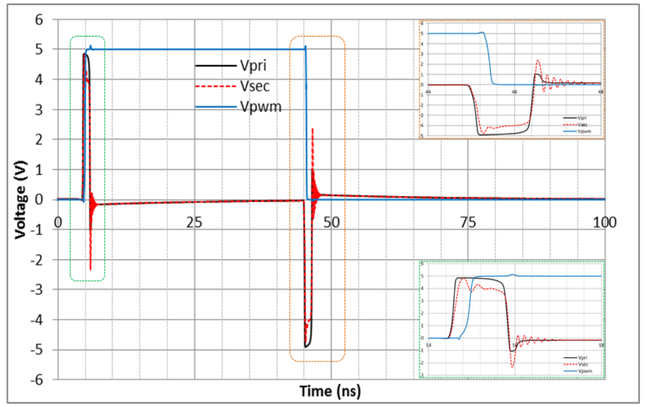


Table 2 Summary of FEM simulation results

Parameter	Values	
Switching frequency (f_{SW}) [MHz]	20	
Magnetizing inductance (L_{11}) @ f_{SW} [nH]	39.3	
Coupling coefficient (k_{12})	0.83	
DC resistance (R_{DC}) [mΩ]	310	
Quality factor @ f_{SW}	13.7	
Si-oxide base thickness [μm]	1	5
Parasitic capacitance (C_{12}) [pF]	10.76	3.68



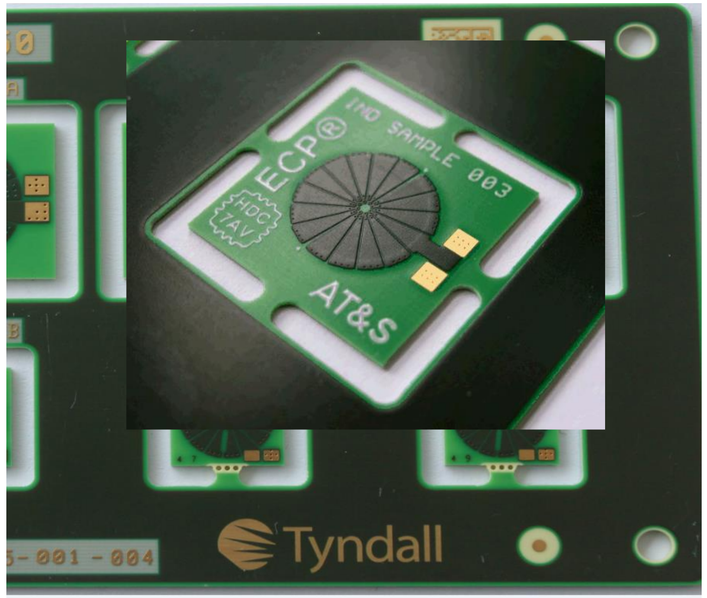
Simulated for 130 nm CMOS

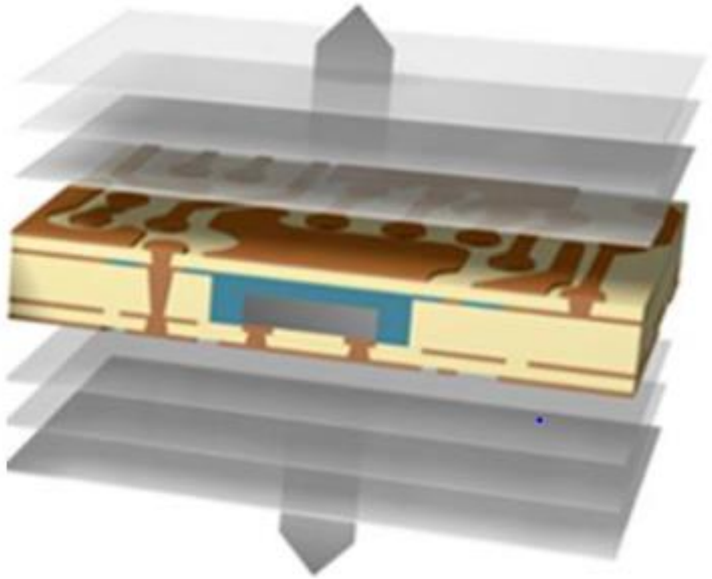
[8] Z. Pavlovic,Tyndall, et al. EU H2020 “GaNonCMOS” www.ganoncmos.eu

Characterisation of Substrate Embeddable Materials

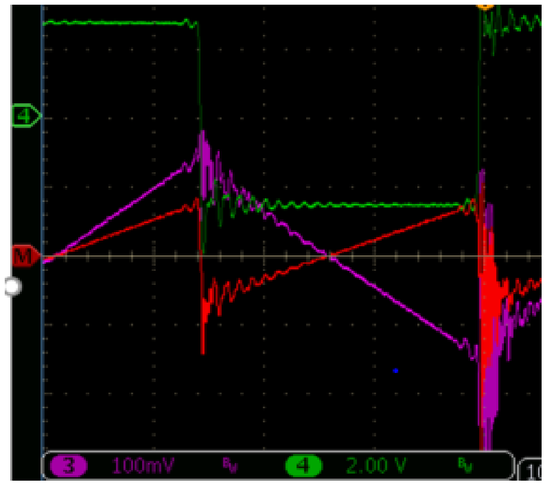
Q_Isic Large signal in-converter Q.

Particularly elucidating regarding intrinsic material capacitances, HF magnetic loss damping, EMI impact, B-H loop tracing,..



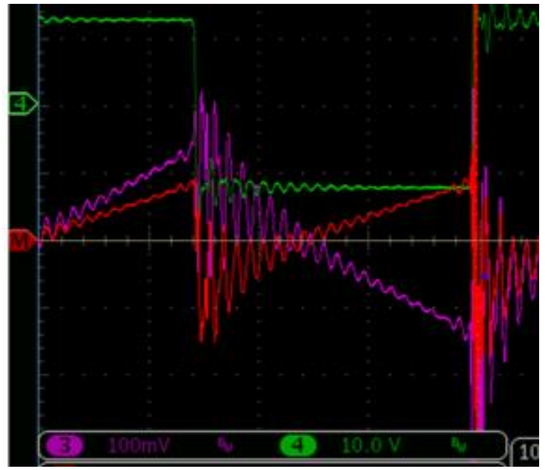


Centre Core Embedding,
CCE, AT&S



Ferrite particles in post cure resin

V_L (green),
I_L (purple)
V_L*I_L



Metal sheets in resin

[9] R. Murphy, Tyndall, et al., G. Weidinger et al., AT&S, EU H2020 “GaNonCMOS” www.ganoncmos.eu

Commercial Magnetic Materials Characterisation &Embedding Qualification

www.ganoncmos.eu

"GaNonCMOS" program with AT&S: a variety of new materials are emerging, which are suitable for embedding and exiting reliability trials

- Sintered ferrites (some are parylene coated)
- Ferrite loaded epoxies, polymers
- Magnetic particles in polymer
- Laminated metallic strips in polymer
- Flex sheets with ferrite powders
- Embedded Tyndall thin film CZT(B)

Some materials will marginally advance the 9 MHz ***Performance Factor*** achieved by low permeability ferrite, Alex Hanson et al. in 2016 [10] – these still appear to be ferrite based!

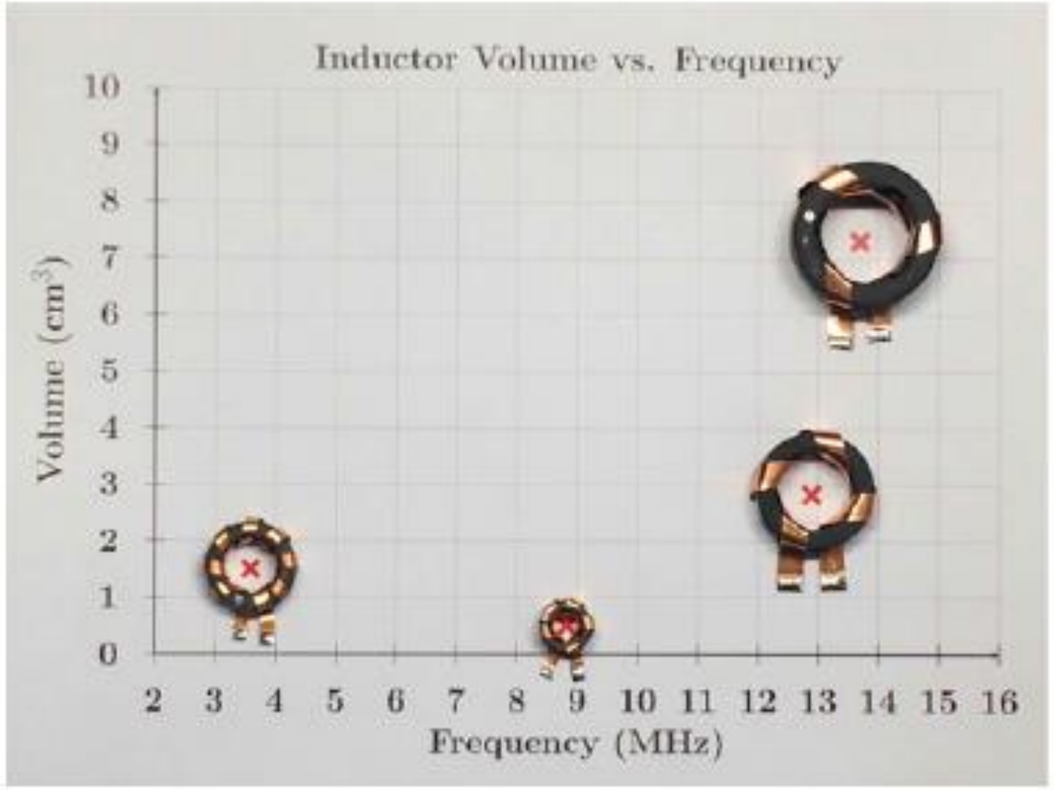


Fig. 4. Inductors using ungapped toroidal cores of Fair-Rite 67 material

[10] Alex Hanson et al.,

$\mu_r = 40$

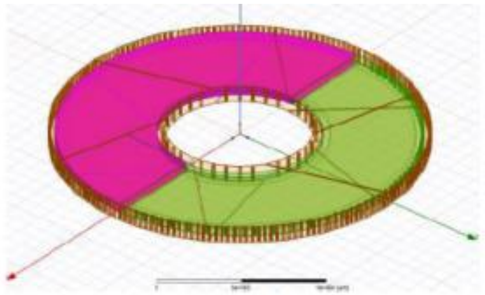
Embedded 6:1:1 LLC Transformer Design

300 nH L_{MAG} , 30 nH Leakage Resonance, 95% target at 10 MHz, 2.5A DC output.

Embedded commercial material, 3M15TF, achieves large signal Q = 20 at 10 MHz

Up to 4 sheets of 0.1mm film compatible with standard PCB core thickness

LLC design comprises 5 V rated SR's and GaN primary switches all driven by MoS GD Tx

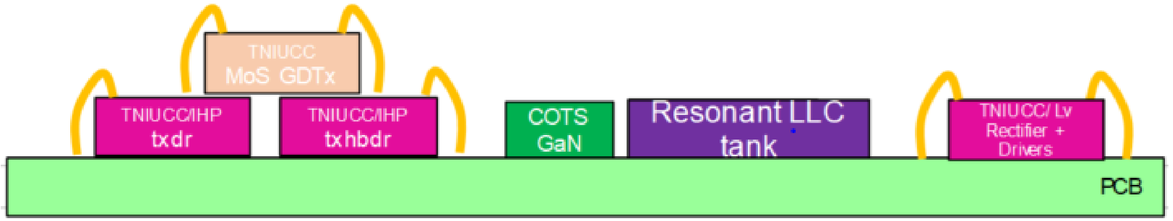


LLC Transformer modelled in Maxwell with Large signal material-in - device measured Q = 20 at 10 MHz, 17 mT.

WP = brown, WS = pink, green

Transformer simulation results

	Device dimensions	L_{pl} (nH)	R_p (mΩ)	L_m (nH)	R_c (mΩ)	L_{sl} (nHΩ)	R_s (mΩ)
Design 1 7x 100um 3M, 35um Cu	OD = 18 mm H = 1.5 mm	13	15	285	1263	0.3	1.7
Design 2 **4x 100um 3M, 35um Cu**	**OD = 23 mm** **H = 1 mm**	**13**	**24**	**285**	**975**	**0.3**	**1.4**
Design 3 4x 100um 3M, 35um Cu	OD =22 mm H = 0.5 mm	68	80	247	935	7.3	9.5



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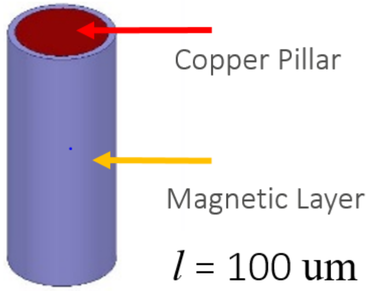
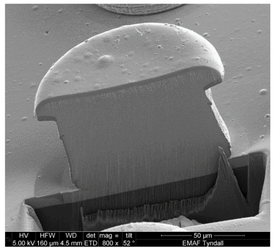
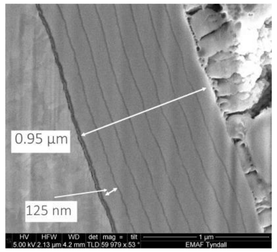
Vertical Inductors Array for SoC iVR

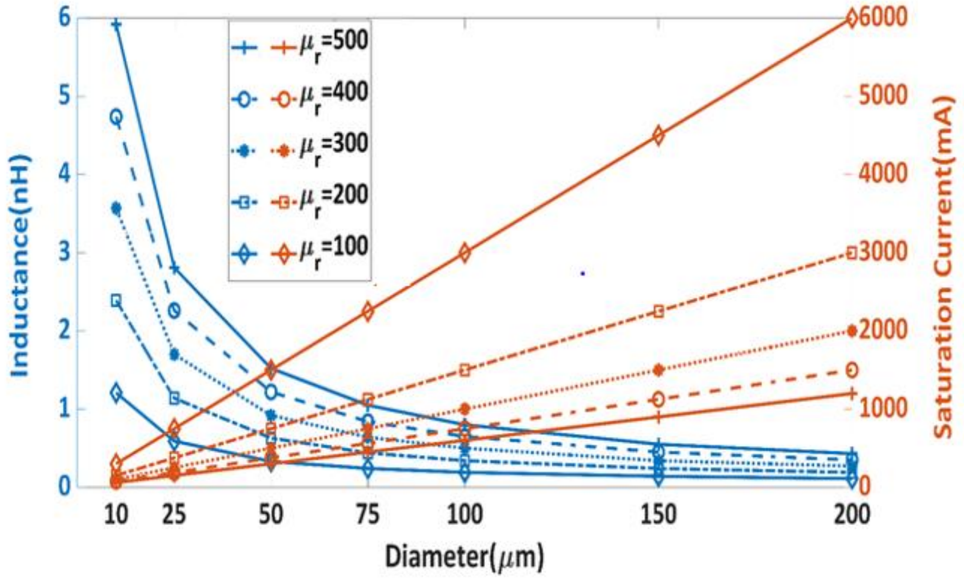






Vertical Interconnect

- Increasing pillar aspect ratio (& L value) adds value for high phase count
- 6 A/mm^2 – area match-up with 28 nm CMOS VR power switching bridge
- High Saturation Current (N=1) $\boldsymbol{I_{sat} = \frac{B_{sat} l}{N \mu}}$
- Other TSV inductor systems, N>=1

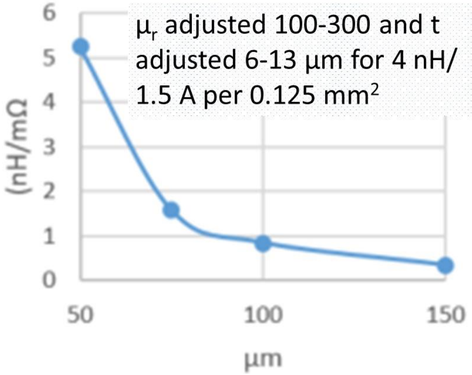


Parameter \ Types	Solenoid (2D)	Adept 3D (Aircore)	Existing TSV Inductor [11]	Adept 3D Inductor	SMT 0402-0805 CHIP INDUCTOR[3]
Inductance Density (nH/mm^2)	15	3.5	91	32 [1] 4 [2]	53
L (nH)/DCR(mΩ)	0.6	0.16	0.002	5.24	0.61
Current Density (A_{DC}/mm^2)	<1	*	1	0.75 [1] 6 [2]	1.23

[1] series, [2] parallel

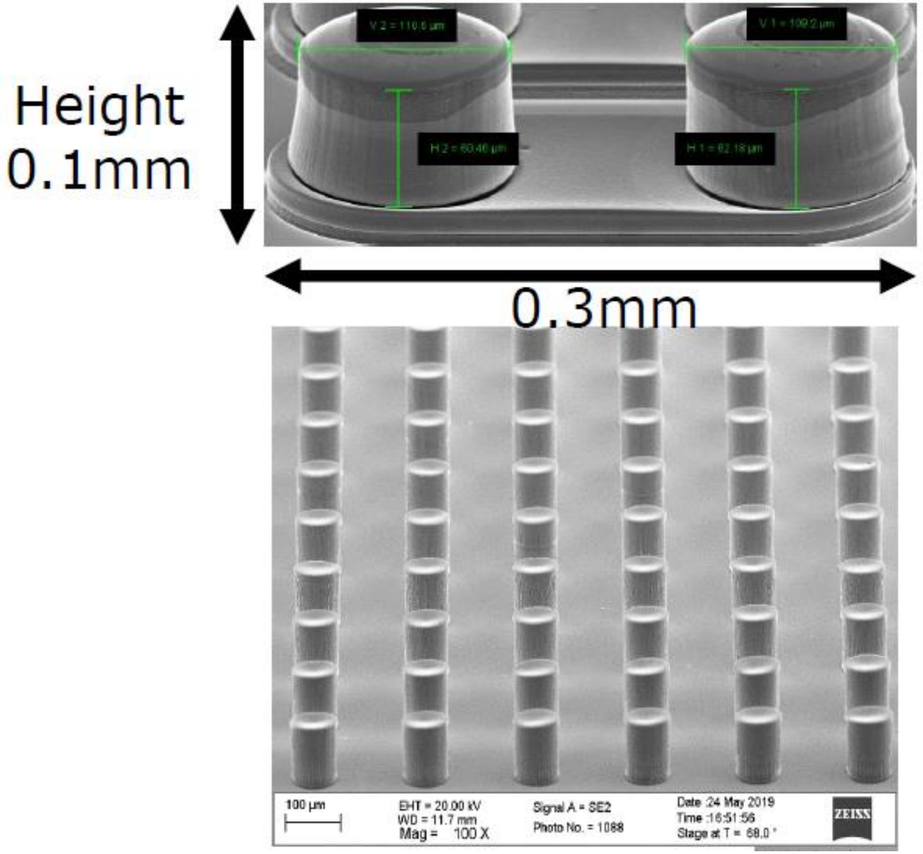
Design Space Study

L/DCR versus Diameter



C. O' Mathúna et al., Science Foundation Ireland ADEPT Project –2017-2020

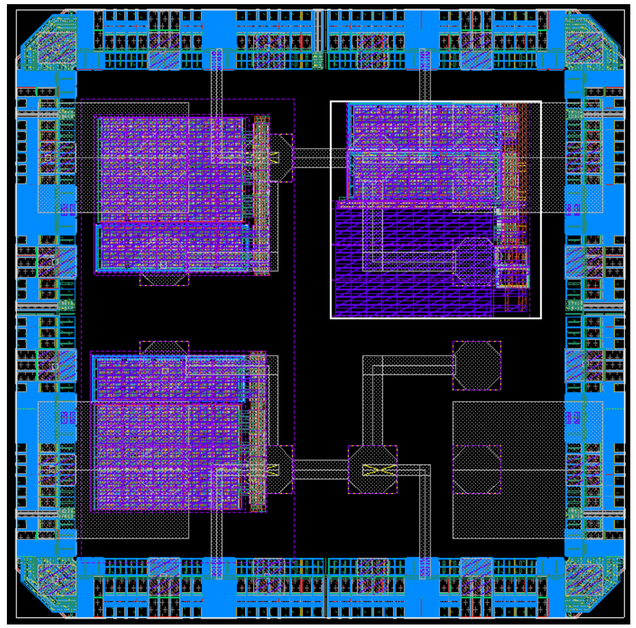
Tyndall Vertical Inductors Array



C. O' Mathúna et al., Science Foundation Ireland ADEPT Project –2017-2020

~3 nH/pillar

Designed for Tyndall (www.mcci.ie)
28 nm iVR; 4nH , 0.75ADC per phase,
0.125 mm^2 power switch



1 X 1 mm 28 nm PMIC test-chip with PN Buck for 88%, 100MHz, 0.75A per 0.125mm^2 block

Conclusions

The laminated thin film CZT(B) planar solenoidal inductor offers a high Q (95+%) inductor solution over 10-100+ MHz

> 6X inductance density improvement over air-core for 10 nH +

Inductance density and L/R ratio improve with scaling for higher phase count

Solution size reduction with inverse-coupling and multi-level for optimum duty cycle set

PCB/Substrate/Interposer embedding of *stacks* of laminated thin films offers the prospect of ***low DCR*** & relatively ***high L_{MAG}*** & ***10 – 100 MHz*** inductor devices

High frequency transformer (higher permeability/L_{MAG}) based applications such as LV cold-start and resonant bias appear well suited to PCB embedding or tf-MoS for areas such as EH IoT.

The vertical inductors array could offer attractive parameters such as I_{SAT}, DCR in packaging systems which exploit 3-D

Acknowledging

Paul McCloskey, Cian O'Mathúna, Michael Hayes, www.mcci.ie

GaNonCMOS project partners, www.ganoncmos.eu

References

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[4] "Comparison of Coupled vs. Non-Coupled Microfabricated Inductors in 2W 20MHz Interleaved Buck Converter", Youssef Kandeel, NUIG, et al. APEC 2019

[5] Zhara Ghaferi et al, "Characterization and enhancement of magnetic performance of electrodeposited Ni45Fe55 on PCB for high frequency application", Journal of Magnetism and Magnetic Materials (2020)

References

[6] D. Jordan et al, “High Q-Factor PCB Embedded Flip-Chip Inductors with Multi-Layer CZTB Magnetic Sheet for Power Supply in Package (PwrSiP)”, DOI 10.1109/JESTPE.2020.2983125

[7] D. Cronin et al., “Soft magnetic nanocomposite CoZrTaB–SiO2 thin films for high-frequency applications”, J. Applied Physics (2020)

[8] “Thin-film Magnetics-on-Silicon Integrated Transformer for Isolated Signal and Power Coupling Applications”, Zoran Pavlovic et al., 11th International Conference on Integrated Power Electronic Systems; Berlin, Germany. March24-26th, 2020

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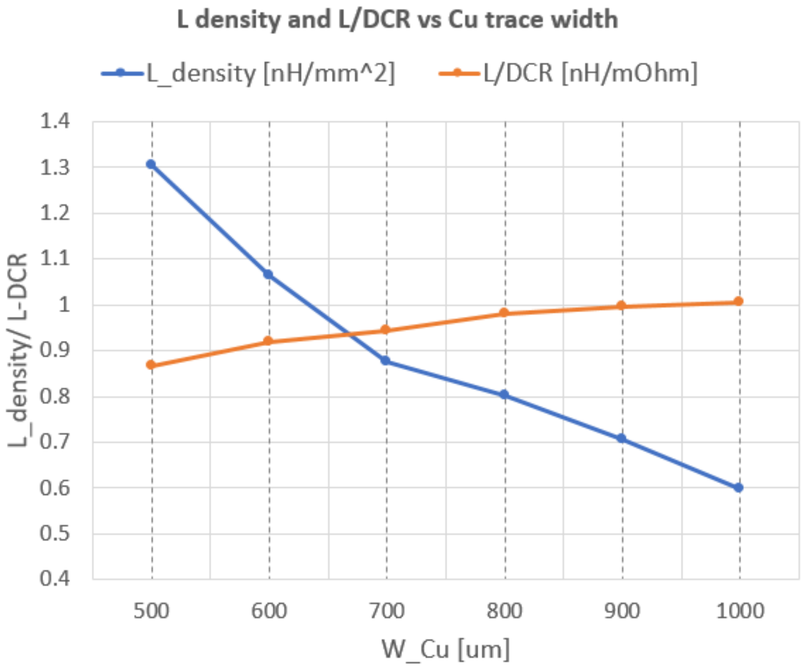
[10] “Measurements and Performance Factor Comparisons of Magnetic Materials at High Frequency “, Alex Hanson et al., IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 31, NO. 11, NOVEMBER 2016

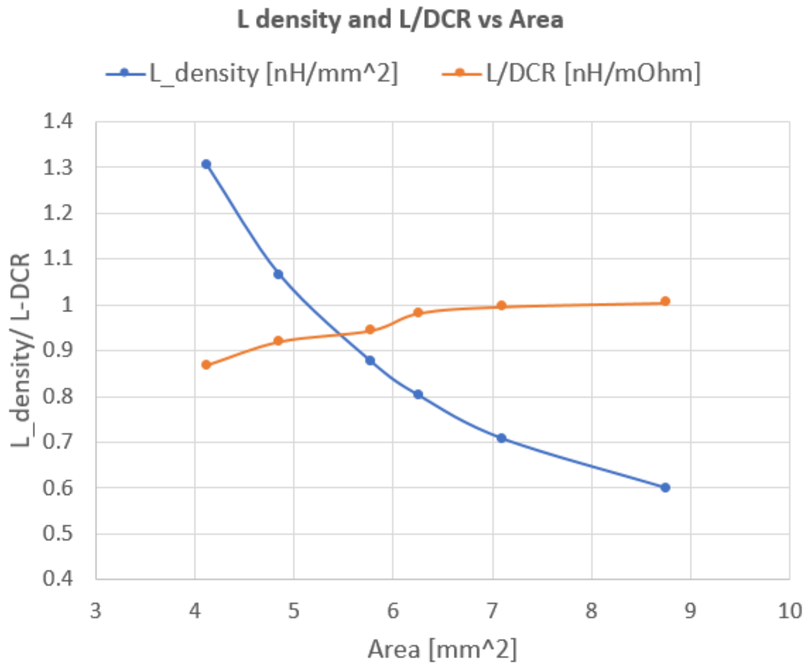
[11] H. K. Krishnamurthy et al., "A Digitally Controlled Fully Integrated Voltage Regulator With 3-D-TSV-Based On-Die Solenoid Inductor With a Planar Magnetic Core for 3-D-Stacked Die Applications in 14-nm Tri-Gate CMOS," in IEEE Journal of Solid-State Circuits, vol. 53, no. 4, pp. 1038-1048, April 2018, doi: 10.1109/JSSC.2017.2773637.

[12] “Fully Integrated Ultra Low Voltage Cold Start System for Thermal Energy Harvesting”, Preetinder Garcha, Master of Science in Electrical Engineering and Computer Science at the MASSACHUSETTS INSTITUTE OF TECHNOLOGY June 2016

Background – A Design Space Exploration

L-density and L/DCR vs Cu width and footprint





For increasing Cu trace width, Inductance density decreases (i.e. inductor footprint increases) at a faster rate than the increase in the L/DCR ratio.