# ****PwrPACK Workshop  2019****

# ****A Satellite PwrSoC Event****

# ****Workshop on Packaging and Integration in Power Delivery (PwrPack)**** ****– An Exploratory Discussion Leading to PwrSoC**** Oct. 31- Nov. 1, 2019

**Host:**

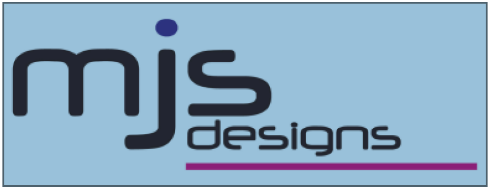
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**(National Science Foundation Efficient Vehicle and Sustainable Transportation)**

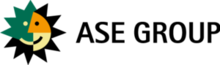
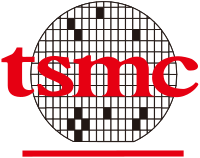
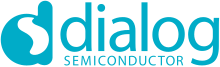
**Sponsored by:**

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**Speakers from:**



# Wireless Connection

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# Workshop Mission

#### This Workshop uniquely spotlights technology and manufacturing advancement of miniaturization and integrationof power conversion and power management solutions.

#### The Power Sources Manufacturers Association (PSMA), in partnership with IEEE Power Electronics Society (PELS), is sponsoring a Phoenix Workshop on Packaging and Integration in Power Delivery at Arizona State University’s SkySong Innovation in Scottsdale, AZ **starts 12:00 Noon October 31- and ends at 1:30 PM Nov. 1, 2019 Pacific Time.** This two half-day event is An Exploratory Workshop Leading to the [2020 International Workshop on Power Supply on Chip (PwrSoC)](http://pwrsocevents.com/), in Philadelphia, PA.

#### In recent years power electronic devices’ overall form factor have scaled-down significantly for a broad range of applications and power levels. This two-half day workshop will focus on two topics related to power delivery in a package:

#### Power system in package (PSiP) power modules

#### Process and integration of multi-die power delivery in package,

#### with invited speakers from both industry and academia to address the challenges and opportunities in miniaturization and efficient power delivery that benefits increasing application areas. Sessions will consist of presentations followed by active discussions between IC designers, assembly experts and substrate/materials providers bringing innovative solutions to address power delivery in package challenges.

[](http://pwrsocevents.com/wp-content/uploads/2019/08/Hongbin-Yu.jpg)

#### Workshop General Chair Professor Hongbin Yu commenting on this workshop’s venue: “We are excited to have this workshop in Phoenix area, where there are many microelectronics companies in the Valley area that are very active in developing new semiconductor devices that will require innovation in the scaling of power integration and much-improved efficiency. Through this workshop, we hope to foster much stronger collaboration between academia and industry in this region resulting in new and key contributions in power delivery innovations.”

#### [/var/folders/d8/ljq7pf3x4v77jc8nfg7c596dn2f6wy/T/com.microsoft.Word/WebArchiveCopyPasteTempFiles/Jim-Doyle-Lighter.png](http://pwrsocevents.com/wp-content/uploads/2018/09/Jim-Doyle-Lighter.png)Technical Program Chair Jim Doyle from Dialog Semiconductor points out “The workshop intends to bring together technical experts on SOC packaging mainly from the Phoenix area, the line between pure integration and multichip SIPs have become blurry since processes such as InFo, MCeP,WLP/RCP,WL-esip, 3D TSV offered by different foundries and packaging companies, provide area effective solutions competitive with full integration.  This could revolutionize the decision to integrate or not to integrate. Join us to learn more about the options and trade-offs.”

# Organizing Committee

General Chair:

* Prof. Hongbin Yu, *Arizona State University,* [yuhb@asu.edu](mailto:yuhb@asu.edu)

Technical Program Chair:

* Jim Doyle, *Dialog Semiconductor,* [Jim.Doyle@diasemi.com](mailto:Jim.Doyle@diasemi.com)

Treasurer:

* Shamala Chickamenahalli, *Arizona State University* [Shamala.Chickamenahalli@asu.edu](mailto:Shamala.Chickamenahalli@asu.edu)

PwrSoC Steering Committee representatives:

- Arnold Alderman, *Anagenesis*, [arnold.alderman@anagenesis-inc.com](mailto:arnold.alderman@anagenesis-inc.com)

- Prof. Hanh-Phuc Le, *University of California*, San Diego, [hanphuc@ucsd.edu](mailto:hanphuc@ucsd.edu)

- Francesco Carobolante, *IoTissimo,* [carobolante@](mailto:carobolante@iee)[ieee.org](mailto:hanhphuc@Colorado.EDU)

Session Chairs:

- Ambreesh Bhattad, *Dialog Semiconductor*, [ambreesh.bhattad@diasemi.com](mailto:ambreesh.bhattad@diasemi.com)

- Francesco Carobolante, *IoTissimo* [carobolante@ieee.org](mailto:carobolante@ieee.org)

- Vasudeva Atluri, *Renavitas Technologies,* [vpatluri@ieee.org](mailto:vpatluri@ieee.org)

- Jihong Ren, *Facebook*, [Jihong.Ren@Oculus.com](mailto:Jihong.Ren@Oculus.com)

Technical Support:

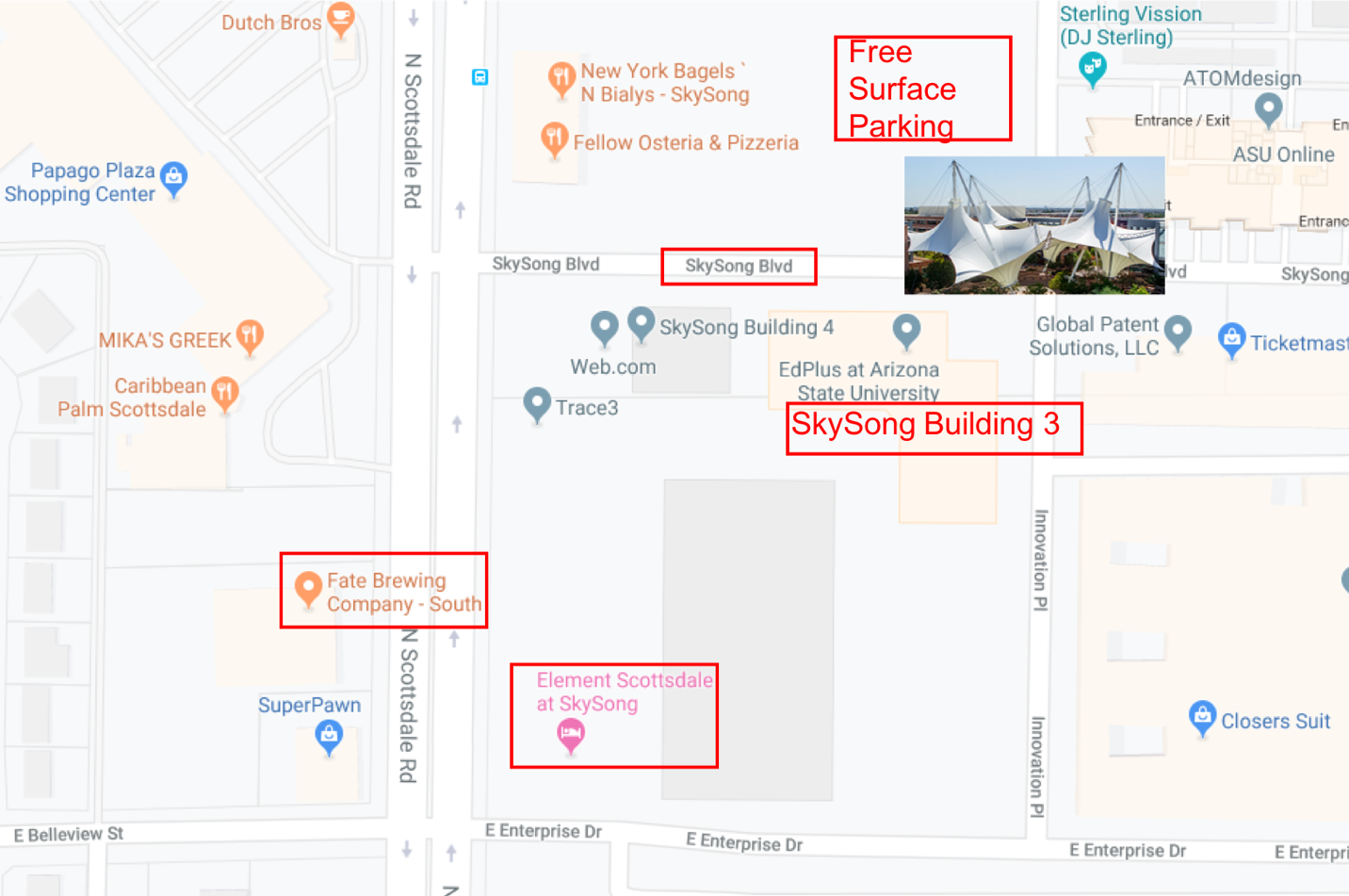
* Christopher David Lue Sang, *Clue Media*, [christopher@cluemediallc.com](mailto:christopher@cluemediallc.com)

Local support team

* Yanze Wu, *Arizona State University*
* HaokaiYang, *Arizona State University*

# Map of Workshop Venue, Hotel Element and dinner reception site.

These three sites are very close to each other, within walking distance.

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**Workshop Venue: ASU SkySong Synergy I**

**Address:**

Arizona State University SkySong

1365 North Scottsdale Road

Scottsdale AZ 85257

Room: SkySong Building 3 Room 130 Synergy I (Conference Room)

<http://skysong.com/properties/skysong-3/>



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# Accommodations & Banquet Venue

**Hotel: Element Scottsdale at SkySong; need names and nights for reservation asap.**

Just opened in June 2019, you may not see the finished hotel on Google map or Apple Map. But it is very nice.

Address:

1345 N Scottsdale Rd, Scottsdale, AZ 85257

Room rate for our workshop: $149 per night plus tax.

They have not set up online group rate for our workshop, so please let me know asap if you need to stay at this hotel and which nights.

**Dinner Reception Site on Oct. 31: Fate Brewing Company, location. 6:00-10pm**

# Fate Brewing Company - South

1312 N Scottsdale Rd

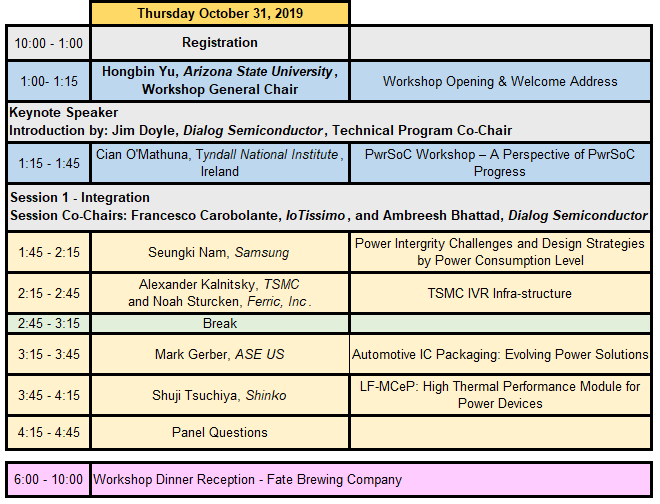
Scottsdale, AZ 85257

(480) 656 - 9100

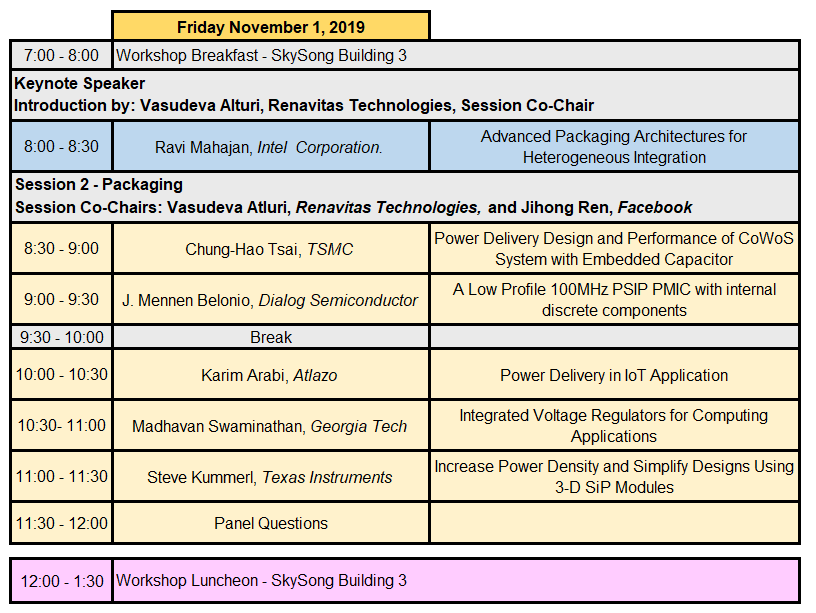
Website: https://fatebrewing.com

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# Program Details & Schedule



**Notes.**

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**Notes.**

# Keynote Speakers

**Keynote #1**

**PwrSoC Workshop – A Perspective of PwrSoC Progress**

**Cian O’Mathuna, FIEEE**

**Tyndall National Institute, University College Cork, Ireland**

[**www.tyndall.ie**](http://www.tyndall.ie)**;** [**cian.omathuna@tyndall.ie**](mailto:cian.omathuna@tyndall.ie)

**Abstract**

The concept of fully integrated dc-dc conversion and voltage regulation has been discussed in both industry and academia for more than a decade. Currently, the major challenge being addressed by many companies is the miniaturization and integration of bulky inductor components in dc-dc converters for power delivery to micro-processors and systems-on-chip (SoC) in electronic systems These inductors can take up to 50% of the power management footprint on the motherboard, introduce an unacceptable height profile, add to the bill-of-materials cost and introduce circuit parasitics which impact power efficiency and high-speed transient performance. Commercial solutions for monolithic integration of thin-film magnetic-core inductors continue to be explored by a number of companies, the major roadblocks being the availability of high-volume foundry capability and high frequency power management ICs. Some companies have stepped back from the monolithic solution and are exploring inductor integration into or on top of the processor package or substrate. Other companies are exploring the alternative use of air-core inductors. This presentation will explore the progress and evolution of the PwrSoC concept. Special attention will be given to the opportunities and challenges that exist for the OSAT and package substrate industries in the evolving technology roadmap.

**Biography**

Prof O’Mathuna has more than 30 years’ experience in applied research and technology transfer to Irish and international industry. His research is focused on the convergence of microelectronics and microsystems to address the future technological challenges that will enable the 1 trillion sensor economy. Cian is Head of Centre for MicroNano Systems at Tyndall which is focused on developing a fundamental understanding of how to interface intelligent, autonomous microelectronic systems: \* with the built and the natural environment to improve the sustainability of our natural resources and the quality of our environment through monitoring and control and \* with the human body to enhance our health and well-being through wearable and in-vivo diagnostics and therapeutics.

Cian has been a co-founding member of national industry-academic research clusters in the areas of surface mount technology (Smart Group Ireland), wireless sensor networks (WiSEN) and power electronics (PEIG). In 2010, he was an Irish Government appointee on the National Innovation Task Force Implementation Group. He is a Research Professor in the College of Engineering, University College Cork. Cian has been associated with the PSMA for more than 20 years as a Board Member and as Co-Chair of the Packaging Committee. In 2008, he founded the International Workshop on Power Supply on Chip (PwrSoC) which is now the PSMA and IEEE flagship conference in this space. As a result, Prof. Ó Mathúna is recognized by the global semiconductor community for his thought-leadership in articulating and driving a vision to deliver the “holy grail” for fully-integrated power management of electronic systems, “Power Supply-on-Chip” (PwrSoC). In January 2013, he was named an IEEE Fellow in the field of power electronics.

**Keynote #2**

**Advanced Packaging Architectures for Heterogeneous Integration**

**Ravi Mahajan**

**Intel Fellow, Intel Corporation.**

**Abstract**

In recent years advanced packaging technologies have gained considerable attention because of their importance as compact, power efficient platforms for heterogeneous integration (HI).  This talk will trace the evolving role of packaging over the past decades and examine its value as an HI platform.  Different packaging architectures will be compared primarily on the basis of their physical interconnect capabilities.  Key features in leading edge 2D and 3D technologies, such as EMIB, Silicon Interposer, Foveros and Co-EMIB will be described and a roadmap for their evolution will be presented.  The talk will conclude with a discussion of opportunities and challenges in driving the package roadmap forward.

**Biography**

**RAVI MAHAJAN** is an Intel Fellow and the Co-director of pathfinding and assembly and packaging technologies for 7-nanometer (7nm) silicon and beyond in the Technology and Manufacturing Group at Intel Corporation. He is responsible for planning and carrying out multi-chip package pathfinding programs for the latest Intel process technologies, led efforts to define and set strategic direction for package architecture, technologies and assembly processes at Intel since joining the company’s Assembly and Test Technology Development organization in 2000, spanning 90nm, 65nm, 45nm, 32nm, 22nm and 7nm silicon. Earlier in his Intel career, he spent five years as group manager for thermal mechanical tools and analysis.

A prolific inventor and recognized expert in microelectronics packaging technologies, Mahajan holds more than 30 patents, including the original patent for a silicon bridge that became the foundation for Intel’s Embedded Multi-Die Interconnect Bridge technology. His early insights also led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques used for thermo-mechanical stress model validation. Ravi has written several book chapters and more than 30 papers on topics related to his area of expertise.

Ravi joined Intel in 1992 after earning a bachelor’s degree from Bombay University, a master’s degree from the University of Houston, and a Ph.D. from Lehigh University, all in mechanical engineering. His contributions during his Intel career have earned him numerous industry honors, most recently the SRC’s 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI award from SEMITHERM and the 2016 Allan Kraus Thermal Management Medal from the American Society of Mechanical Engineers. He has also been nominated as an IEEE EPS Distinguished Lecturer.  He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently Co-Editor for Special Topics of IEEE T-CPMT.  Additionally, he has been long associated with ASME’s InterPACK conference and was Conference Co-Chair of the 2017 Conference.  Ravi is a Fellow of two leading societies, ASME and IEEE.  He was named an Intel Fellow in 2017.

# Invited Talks

1. **Power Integrity Challenges and Design Strategies by Power Consumption Level**

**Sungwook Moon**

**Samsung**

**Abstract**

This talk will introduce the power consumption level by various applications and their design challenges from the viewpoint of system-level power integrity considering chip, interposer, PKG and set board. To check the power integrity risk due to these design challenges at early design stage, the system-level PDN(Power Distribution Network) analysis method will be explained. In addition, our design strategies and various efficient solutions for system-level power integrity will be suggested.

**Biography**



Seungki Nam has worked in Samsung Electronics from 2005 after receiving the Ph. D. degrees in Microwave Engineering from Korea University, Seoul, Korea. Currently, he is developing the design and analysis methodologies of system-level power distribution network for mobile, automotive, HPC/AI platforms.

1. **TSMC IVR Infra-structure**

**Alexander Kalnitsky**

***TSMC***

**Abstract**

TSMC provides the following components as part of the IVR (integrated voltage regulator) infrastructure:

1. High density low parasitic inductance and resistance capacitor with low frequency densities ranging from 1.2uF/mm2 for 2020 production to ~3.5uF/mm2 in 2023. Capacitors are currently produced and new generations developed in 12” fabs. This component is most commonly used today as a decoupling capacitor mounted on the high current load package.
2. Ferric Semiconductor high inductance, low series resistance inductor that can be integrated either on a 12” CMOS wafer or on a 12” capacitor wafer.
3. A variety of CMOS processes, not discussed in this presentation.

An example of the integrated voltage regulator performance built on the 28nm CMOS process will be presented.

**Biography**

**Dr. Alexander Kalnitsky** is Vice President of More-than-Moore Technologies at Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC) and he joined TSMC in 2009 as Senior Director of the More-than-Moore Technologies Division.

Dr. Kalnitsky was elected as a TSMC Fellow in 2013. He is a well-respected technical leader in the industry with an excellent proven track record in HV/Power/Analog/RF/CIS/MEMS and embedded NVM processes development. Dr. Kalnitsky has over 180 U.S. patents. He also has over 150 publications in technical journals and conference presentations.

Prior to joining TSMC, Dr. Kalnitsky worked for over 30 years in the semiconductor industry at international companies such as Intersil, Maxim Integrated Product, National Semiconductor, ST Microelectronics and Northern Telecom. Dr. Kalnitsky received his M.S. degree in Applied Sciences from the University of Toronto, Canada and Ph.D. in Electrical Engineering from Carleton University, Canada.

**Dr. Noah Sturcken** has focused on the integration of switched-inductor power conversion with CMOS integrated magnetic inductors for nearly a decade. Dr. Sturcken is a founder and CEO of Ferric, which sells integrated voltage regulator products and related technologies. Dr. Sturcken holds a PhD from Columbia University and has over 25 publications and patents, primarily related to CMOS integrated power conversion.

1. **Automotive IC Packaging: Evolving Power Solutions**

**Mark Gerber**

**Sr. Director Engineering and Technical Marketing, ASE US Inc.**

**Abstract**

Current and future automotive and industrial applications are facing power and performance challenges.  Semiconductor packaging will play a key role in enabling the next generation of IC and Module based solutions that address these challenges.  As device switching speeds increase and power efficiencies become more critical, new packaging methodologies are required to address performance and reliability challenges.  This presentation will explore these barriers and look at the next generation of power packaging solutions to enable the next generation of automobiles and industrial products.

**Biography**

****Mark Gerber is Sr. Director of Engineering and Marketing of Flip Chip

and SiP at ASE (US) Inc. and provides technical support for customer activities around the 5G and Automotive market segments with package platform focus areas including Flip Chip, Copper Pillar and SiP Packaging Technologies.  Mark has 25 years of semiconductor packaging experience working for ASE, Texas Instruments, Motorola SPS and Maxim Integrated Maxim Integrated in various areas of manufacturing, assembly and testing of electronics components and systems, with an emphasis on the development of new technologies and processes.  Mark holds a Bachelor’s degree in Mechanical Engineering from Texas A&M University, has written +20 papers and holds over 32 semiconductor packaging patents.

1. **LF-MCeP : High Thermal Performance Module for Power Devices**

**Shuji Tsuchiya**

**Shinko**

**Abstract**

Shinko has been developing a new device embedded package which provides both high thermal dissipation and a small package size. A three-dimensional package structure and the adoption of Lead-frame are the key attributes. This enhanced module structure can be constructed with an existing assembly process and equipment. Shinko describes capabilities and simulation results of the new package along with collected characteristics.

**Biography**

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Shuji Tsuchiya graduated from Nagano Technical College majoring in Techniques of Electrical and Electronic Circuit Systems. Shuji joined SHINKO ELECTRIC INDUSTRIES CO., LTD. in 1999. He currently leads the Assembly Design Engineering Department, and experienced in production and design for various packaging solutions, particularly small size packages, embedded modules, high heat dissipation modules and MCeP products. He also experienced in multilayer board and electrical characteristic design with a comprehensive knowledge from board design through package assembly.

1. **Power Delivery Design and Performance of CoWoS System with Embedded Capacitor**

**Chung-Hao Tsai**

**Technical Manager,** **TSMC**

**Abstract**

High performance computing (HPC) cores require on-die capacitor to mitigate voltage noise from power delivery network. As the required power consumption of computing cores increases, current on-die capacitor is not enough to fulfill the high current consumption of processor cores. As a result, the power delivery design of HPC system becomes challenging.

In this work, an on-interposer capacitor, such as MiM capacitor, on CoWoS platform is proposed to overcome the challenge. From designer point of view, I will report the feature of on-interposer capacitor with density of 17 fF/um2 and the power delivery design from PCB to chip through CoWoS platform. According to the modeling results, this capacitor in CoWoS platform helps reduce the voltage droop level of a computing core and simultaneously switching noise (SSN) of HBM2 PHY by over 30%. Moreover, the eye margin and jitter of HBM2E is significantly improved.

**Biography**

****Chung-Hao Tsai received the PhD degree in communication engineering from National Taiwan University, Taipei, Taiwan, in 2012.

He is currently a technical manager with TSMC, Taiwan, in charge of SI/PI/RF design and modeling of 3DIC package and WLSI technology. In 2016, he received the young scientist award of IEEE APEMC for outstanding contribution in development of SiP technology for 5G mobile and high speed system application. He has held over 40 US patents and published over 20 papers in the field.

1. **A Low Profile 100MHz PSIP PMIC with internal discrete components**

**J. Mennen Belonio**

**Dialog Semiconductor**

**Abstract**

    A system in package is provided comprising an embedded trace substrate having redistribution layers therein, at least one or more  passive component mounted on one side of the embedded trace substrate and embedded in a first steps  of encapsulation molding process , and  one silicon die mounted on an opposite side of the embedded trace substrate and embedded in a second molding  encapsulation steps wherein electrical connections are made between silicon die  AP layer with Cu Pillar Bump  connected and the passive components  connected through the Cu Traces of  Organic Substrate  layers, with solder balls mounted through Mold Via openings in the second molding layer to the trace Via  of the Substrate pads  wherein the solder balls provides package I/O‘s .

Significant Results include the module passed Customer Reliability requirements in all level of checkpoints including package level (ex. MSL3 ,TC1000, uHAST, HTST). Also, Board level   
(ex. TCoB 1000, THD, Random Vibration & Drop Test.

**Biography**



Senior Group Manager for Dialog Semiconductor IC Packaging Advance Package Development/Innovation. Experience includes 29years of Semiconductor Packaging Technology Experience. Published No. of technical articles and Packaging Patents on the following Packages & Technology including Fan -Out WLP , SIP Package Technology.

1. **Power Delivery in IoT Application**

**Karim Arabi**

**CEO Atlazo Inc**

**Abstract**

Power delivery for ultra-low power IoT applications:

Ultra-low power IoT applications are emerging as one the highest volume opportunity for edge AI technology. These applications impose strict size restrictions and need to operate under 1mA active power using a small battery. A new generation of PMIC and power delivery solutions is therefore required. This presentation introduces requirements and solutions for ultra power edge AI IoT applications.

**Biography**

Dr. Karim Arabi is founder and CEO of Atlazo, Inc. developing ultra-low power PMIC, AI SoC and software for the rapidly growing edge AI application. Previously, he was Vice President, R&D at Qualcomm where he was head of Corp. R&D ASIC. Dr. Arabi was Executive Chairman of Appulse Power, an innovative AC/DC semiconductor chip designer, acquired by Silanna Semiconductor in 2018. Karim was also VP at Dialog Semiconductor responsible for driving overall technology and new product development. Karim held technical positions at PMC Sierra and Cirrus Logic and was co-founder of Opmaxx, an innovative startup in mixed-signal design and test acquired by Credence in 1998. Karim obtained his Ph.D. and M.Sc. in Electrical Engineering from Polytechnique Montréal, Canada and his B.Sc. in Electrical Engineering from Tehran Polytechnic. Dr. Karim Arabi is a frequent keynote speaker and has published more than 100 papers in accredited journals and international conferences and holds several key patents.

1. **Integrated Voltage Regulators for Computing Applications**

**Madhavan Swaminathan**

**Georgia Tech**

John Pippin Chair in Microsystems Packaging & Electromagnetics

Director, 3D Systems Packaging Research Center

School of Electrical and Computer Engineering

School of Materials Science and Engineering

Georgia Tech (GT), USA

[www.prc.gatech.edu](http://www.prc.gatech.edu)

**Abstract**

Data Centers consume 70 billion KWh today in USA alone. For every 2W of power drawn from the grid roughly 1W of power is wasted by the computing elements resulting in large amounts of heat being generated. This wastage comes from two main sources, i) inefficient power delivery schemes and ii) leaky circuits. The focus of this presentation will be on integrated voltage regulators (IVR) that addresses the first problem.

This presentation will address the challenges associated with integrating the power delivery solution close to the SOC for 1.7V/3.3V/5V to 1V and 48V to 1V conversion ratios where packaging plays a very important role. Various circuit and integration technologies will be discussed including the ability to integrate inductors into the substrate for heterogeneous integration solutions.

**Biography**

 Madhavan Swaminathan is the John Pippin Chair in Microsystems Packaging & Electromagnetics in the School of Electrical and Computer Engineering (ECE), Professor ECE with a joint appointment in the School of Materials Science and Engineering (MSE), and Director of the 3D Systems Packaging Research Center (PRC), GT. He also serves as the Site Director for the NSF Center for Advanced Electronics through Machine Learning (CAEML). He formerly held the position of Founding Director, Center for Co-Design of Chip, Package, System (C3PS), Joseph M. Pettit Professor in Electronics in ECE and Deputy Director of the Packaging Research Center (NSF ERC), GT. Prior to joining GT, he was with IBM working on packaging for supercomputers. He is the author of 500+ refereed technical publications, holds 30 patents, primary author and co-editor of 3 books, founder and co-founder of two start-up companies, and founder of the IEEE Conference Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the EPS society. He is an IEEE Fellow and has served as the Distinguished Lecturer for the IEEE EMC society. He received his MS/PhD degrees in Electrical Engineering from Syracuse University in 1989 and 1991, respectively.

1. **Increase Power Density and Simplify Designs Using 3-D SiP Modules**

**Steve Kummerl**

**Texas Instruments**

**Abstract**

Today, designers are demanding an overall form-factor reduction to save board space, increase functionality, and allocate more circuit board real estate toward end-user applications – all with less space allocated to power management where not just the X-Y shrink but the 3D volumetric shrink is required. For example, in today’s Telecommunications Cloud Infrastructure systems, board space and power density are challenging particularly in power supply designs where several high-current point-of- load rails are present. End equipment such as enterprise servers and switches, workstations, base stations, network attached storage, FPGA testers, network testers, and other test and measurement equipment employ several high-current CPUs, ASICs, FPGAs, and DDR memory – all of which need high power, while the available board area is steadily decreasing. This paper will discuss volumetric co-design methodology and packaging construction trade-offs for 3D SiP power modules and also introduce the straddle mounted inductor assembly technique. Also provided are details around the SiP eco-system, co-design, construction, materials, and circuit topology.

Key words

3D PIP (Package in Package), 3D SIP (System in Package), DC-DC power converters, Electronics Packaging Integrated Circuits, Embedded SIP, Multichip modules, QFN (Qual Flat Pack No-Lead), SIP (System in Package), SMT (Surface Mount Technology), Stilted Inductors, Straddle Mount Inductors

**Biography**

Steven Kummerl received his B.S. degree in Mechanical Engineering from University of Texas El Paso. He is a member of technical staff at Texas Instruments supporting semiconductor packaging and has worked in the field of high volume/high mix surface mount assemblies for more than 13 years and over 10 years at TI supporting packaging R&D.  He holds over 29 patents in the field of package design and has authored multiple publications focused in packaging design, SMT package assembly, & reliability.