LF-MCeP
High Thermal Performance Module for Power Supply

Shuji Tsuchiya
IC Assembly Division
SHINKO ELECTRIC INDUSTRIES CO., LTD.
Outline

■ Introduction of device embedded package
  - MCeP® introduction

■ Requirements for power modules

■ Introduction of LF-MCeP
  - Heat dissipation
  - Miniaturization / Modularization
  - Substrate routing efficiency

■ Package Characteristics
  - PKG warpage
  - MSL Result

■ Conclusion
  - PKG structure road map
  - Future development challenge
Introduction of Device Embedded Package

**MCeP®**: Molded Core embedded Package

**MCeP® Advantages**
- Fine pitch flip chip interconnection w/ thin die
- Smaller package size than other PoP
- Flexible pad array on top substrate
- Low package warpage w/ thin body
- High yield, high reliability & short TAT
Features of Manufacturing Process Flow

FC bonding on tested bottom substrate

Tested top substrate with Cu core solder balls

✓ Device embedded structure used only assembly technologies
✓ Tested top and bottom substrates

✓ Short TAT
✓ High Yield

Connect top and bottom substrate

Encapsulate with transfer molding

Go to backend processes

Die last process (MCeP®) delivers high assembly yield.
<table>
<thead>
<tr>
<th>Application</th>
<th>MCeP sectional structure</th>
<th>PKG concept</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package under PoP (Mobile, DSC, etc.)</td>
<td><img src="image1.png" alt="Diagram" /></td>
<td>- Pre-stack memory PKG</td>
</tr>
<tr>
<td>RF, for antenna (high frequency)</td>
<td><img src="image2.png" alt="Diagram" /></td>
<td>- One substrate used for antenna</td>
</tr>
<tr>
<td></td>
<td><img src="image3.png" alt="Diagram" /></td>
<td>- Embedded Chip</td>
</tr>
<tr>
<td>For high-density mounting (Device embedded package, Module)</td>
<td><img src="image4.png" alt="Diagram" /></td>
<td>- Parts placement on PKG surface and Embedded layer</td>
</tr>
<tr>
<td></td>
<td><img src="image5.png" alt="Diagram" /></td>
<td>- Make Cu core ball into Cu post and embed passive components etc.</td>
</tr>
<tr>
<td></td>
<td><img src="image6.png" alt="Diagram" /></td>
<td>· The embedded layer can be thickened with a narrow pitch between posts</td>
</tr>
<tr>
<td></td>
<td><img src="image7.png" alt="Diagram" /></td>
<td>⇒ Favorable for built-in parts</td>
</tr>
</tbody>
</table>

**MCeP® is ideal for device embedded packages.**
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Request to Power Supply Module PKG

Heat dissipation requirements

Miniaturization / Modularization

Module for Power Supply Package

Increased substrate routing efficiency
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LF-MCeP Advantages

- Can use existing MCeP® assembly process
- Heat dissipation is advantageous by using LF
- Miniaturization / modularization possible
- Substrate routing efficiency (can shorten routing path)
- Low package warpage
Heat Dissipation Advantage (Mounting Application)

#1: By using LF as the PKG TOP surface, LF can be used as a heat sink.

#2: By making LF PKG Bottom, heat dissipation from the bottom of the PKG can be improved.
## Heat Dissipation Advantage (Thermal Simulation)

### Analysis model

<table>
<thead>
<tr>
<th>Leg.1</th>
<th>Leg.2</th>
<th>Leg.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCeP (2L+4L)</td>
<td>LF-MCeP (LF+4L)</td>
<td>LF-MCeP (LF+4L) with TIM</td>
</tr>
</tbody>
</table>

**Dimension**
- PKG size: 10 x 10 mm
- Chip size: 5 x 5 mm

**Thickness**
- 4L Substrate: 0.37mm
- 2L Substrate: 0.15mm
- LF: 0.15mm
- JEDEC Board: 1.6mm
Heat Dissipation Advantage (Thermal Simulation)

### Analysis conditions

**Solver** | FloTHERM v12.0
---|---
**Analysis type** | Steady state thermal fluid analysis
**Analysis area** | 304.5x342.9x100mm
**Ambient environment** | 25 °C, no wind speed
**Radiation** | Yes
**IC Power** | Chip : 2.0W

### Parts

<table>
<thead>
<tr>
<th>Parts</th>
<th>Thermal conductivity [W/m・K]</th>
<th>Radiation ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip</td>
<td>150</td>
<td>- - -</td>
</tr>
<tr>
<td>Solder</td>
<td>64.2</td>
<td>- - -</td>
</tr>
<tr>
<td>LF</td>
<td>220</td>
<td>- - -</td>
</tr>
<tr>
<td>TIM</td>
<td>30</td>
<td>- - -</td>
</tr>
<tr>
<td>Mold</td>
<td>3</td>
<td>0.9</td>
</tr>
<tr>
<td>NCP</td>
<td>0.54</td>
<td>- - -</td>
</tr>
<tr>
<td>SR</td>
<td>0.23</td>
<td>0.9</td>
</tr>
<tr>
<td>Core</td>
<td>0.73</td>
<td>- - -</td>
</tr>
<tr>
<td>Prepreg</td>
<td>0.73</td>
<td>- - -</td>
</tr>
<tr>
<td>JEDEC board</td>
<td>0.38</td>
<td>0.9</td>
</tr>
<tr>
<td>Air @ 25degC</td>
<td>0.026</td>
<td>- - -</td>
</tr>
</tbody>
</table>
**Heat Dissipation Advantage (Thermal Simulation)**

**Analysis result 1 : \( \theta_{ja} \), Chip temperature**

<table>
<thead>
<tr>
<th></th>
<th>Leg.1: MCeP (2L+4L)</th>
<th>Leg.2: LF-MCeP (LF+4L)</th>
<th>Leg.3: LF-MCeP (LF+4L) with TIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \theta_{ja} )</td>
<td>24.5[K/W]</td>
<td>22.9[K/W]</td>
<td>22.7[K/W]</td>
</tr>
<tr>
<td>Chip temperature</td>
<td>74.1°C</td>
<td>70.9°C</td>
<td>70.4°C</td>
</tr>
</tbody>
</table>

- The chip temperature and thermal resistance \( \theta_{ja} \) of LF-MCeP are lower than MCeP.
- When the TIM material is applied, the chip temperature and the thermal resistance \( \theta_{ja} \) are further reduced.
# Heat Dissipation Advantage (Thermal Simulation)

## Analysis result 2: Thermal flow analysis

<table>
<thead>
<tr>
<th></th>
<th>Leg.1: MCeP (2L+4L)</th>
<th>Leg.2: LF-MCeP (LF+4L)</th>
<th>Leg.3: LF-MCeP (LF+4L) with TIM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A</strong></td>
<td>0.953</td>
<td>1.333</td>
<td>1.333</td>
</tr>
<tr>
<td><strong>B</strong></td>
<td>0.988</td>
<td>0.632</td>
<td>0.547</td>
</tr>
<tr>
<td><strong>C</strong></td>
<td>0.978</td>
<td>0.598</td>
<td>0.510</td>
</tr>
<tr>
<td><strong>D</strong></td>
<td>1.916</td>
<td>1.920</td>
<td>1.920</td>
</tr>
<tr>
<td><strong>E</strong></td>
<td>1.913</td>
<td>1.916</td>
<td>1.917</td>
</tr>
</tbody>
</table>

- Most of the chip heat is dissipated from the JEDEC board.
- In the case of LF, the chip heat is transferred directly to the JEDEC board via LF.

Unit: [W]

- **Conduction**
- **Radiation**
### Miniaturization / Modularization

#### PKG area comparison Module PKG vs LF-MCeP

<table>
<thead>
<tr>
<th>Conventional (2D)</th>
<th>LF-MCeP (3D)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Conventional 2D" /></td>
<td><img src="image2.png" alt="LF-MCeP 3D" /></td>
</tr>
</tbody>
</table>

- **Surface mounting**
- **Backside mounting** (Embedded layer)

Shrink of 25% is possible in the PKG area ratio
By placing components on the front and back of the substrate, the routing path between components can be shortened.

**Calculation results of routing path**
⇒ Routing path can be shortened to about 1/4

**Calculation conditions**
- WLCSP : BGA 0.50mm Pitch
- SMT Size : 0603[mm]
- 4L Substrate : t=0.37mm
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PKG Warpage

- **Sample**
  - PKG size: 9.0mmSQ.
  - Embedded chip and component

[Diagram showing warpage analysis with temperature range from 28°C to 32°C, indicating small warpage range from room temperature to high temperature.]

**Small warpage range from room temperature to high temperature. Low warpage PKG possible.**
### MSL Result

**Sample**
- PKG size: 9.0mmSQ.
- Embedded chip and component

<table>
<thead>
<tr>
<th>MSL</th>
<th>Test condition</th>
<th>N</th>
<th>Result (SAT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSL3</td>
<td>Bake 125°C 24h ⇒ 30°C 60% 192h ⇒ 260°C Max Reflow × 3</td>
<td>10pcs</td>
<td>10 / 10pcs PASS</td>
</tr>
</tbody>
</table>

**Diagram:**
- 4L Substrate
- Embedded Layer
- Lead Frame

**Sample Details:**
- 10 / 10pcs PASS
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PKG Structure Road Map

- **Adoption of Cu Cube**
  - Improved thermal conductivity of upper and lower substrates.
  - Stable connectivity and lower electrical resistance.

- **High thermal conductive mold resin**

- **MCeP adoption of LF + LF**
  - Improves heat dissipation from the top and bottom of the PKG

- Thermally conductive resin is used on the back of the chip
Future Development challenge

■ Summary
  • Use of LF can improve heat dissipation of PKG.
  • Can be miniaturized and modularized by embedding components.
  • The routing length can be shortened by 3D PKG structure.

■ Improved heat dissipation
  • Development of high thermal conductive mold resin.
  • Development of high thermal conductive resin between chip and LF.
Thank you for your attention