SHINKO ELECTRIC INDUSTRIES CO., LTD.

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PwrPack2019

LF-MCeP

High Thermal Performance Module for Power Supply

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Outline

Introduction of device embedded package
- MCeP® introduction

Requirements for power modules

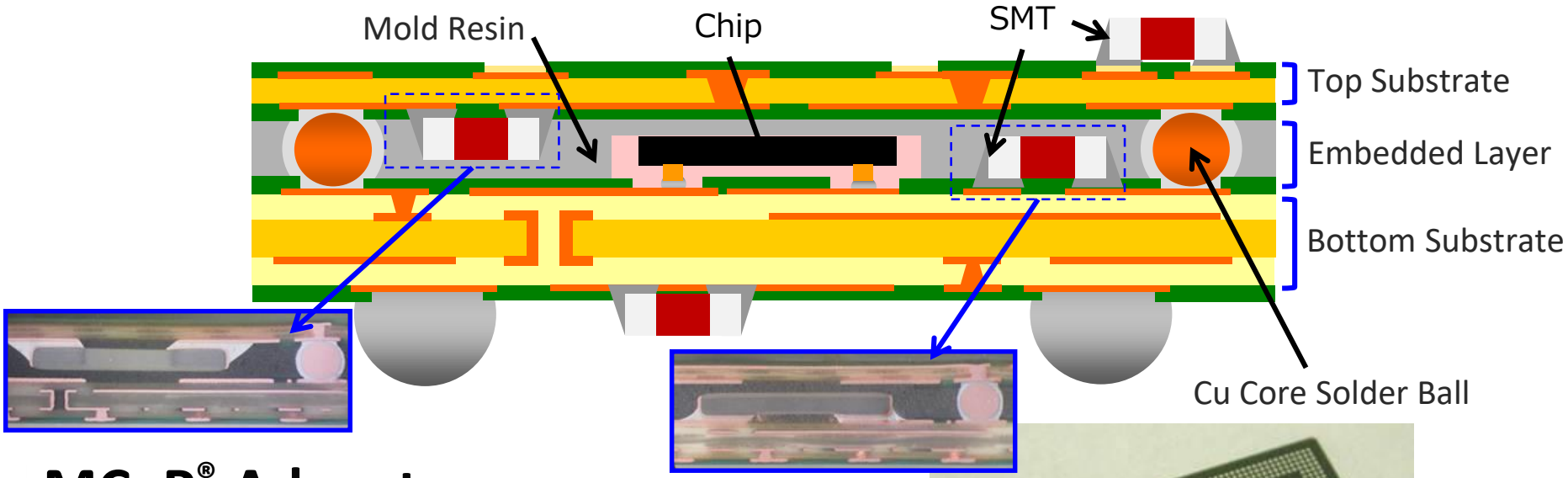
Introduction of LF-MCeP
- Heat dissipation
- Miniaturization / Modularization
- Substrate routing efficiency

Package Characteristics
- PKG warpage
- MSL Result

Conclusion
- PKG structure road map
- Future development challenge

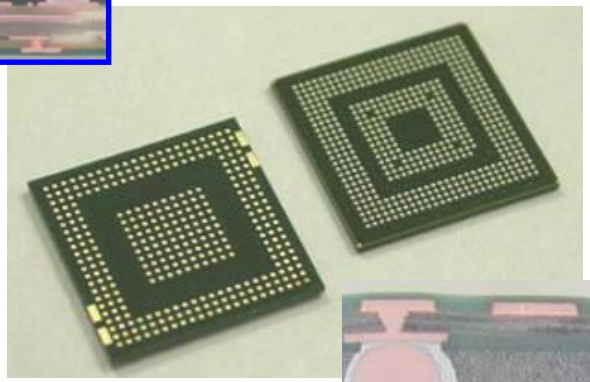
Introduction of Device Embedded Package

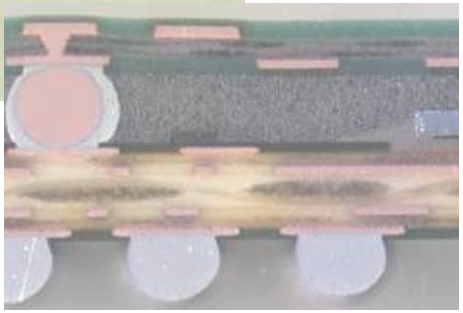
MCeP® : Molded Core embedded Package



MCeP® Advantages

- Fine pitch flip chip interconnection w/ thin die
- Smaller package size than other PoP
- Flexible pad array on top substrate
- Low package warpage w/ thin body
- High yield, high reliability & short TAT

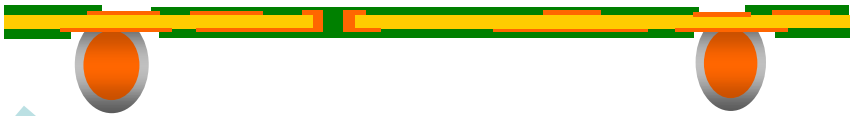




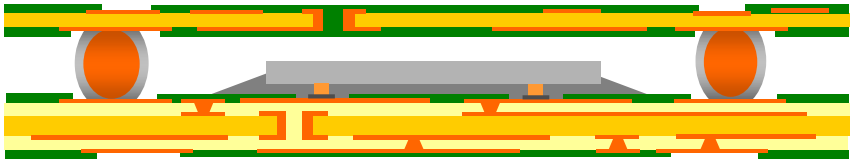
Features of Manufacturing Process Flow

FC bonding on tested bottom substrate

Tested top substrate with Cu core solder balls



Connect top and bottom substrate



Encapsulate with transfer molding

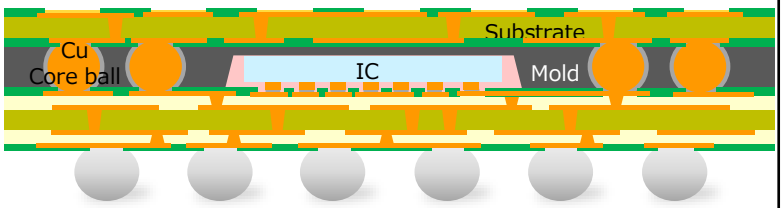
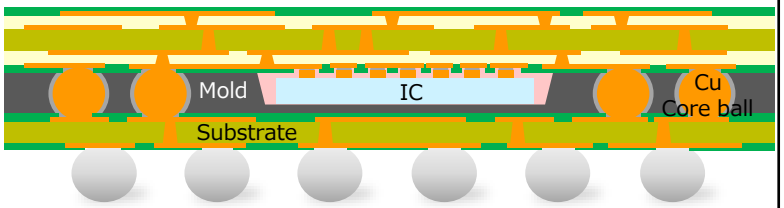
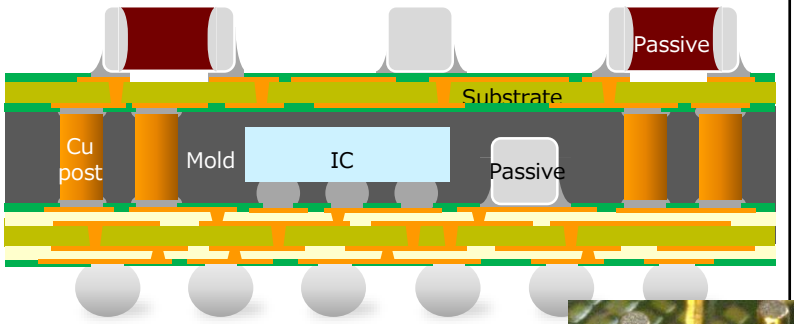
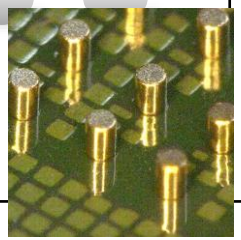
Go to backend processes

- ✓Device embedded structure used only assembly technologies
- ✓ Tested top and bottom substrates

- ✓Short TAT
- ✓High Yield

Die last process (MCeP®) delivers high assembly yield.

Modified MCeP®

Application	MCeP sectional structure	PKG concept
Package under PoP (Mobile, DSC, etc.)		- Pre-stack memory PKG
RF, for antenna (high frequency)		- One substrate used for antenna - Embedded Chip
For high-density mounting (Device embedded package, Module)	 	- Parts placement on PKG surface and Embedded layer - Make Cu core ball into Cu post and embed passive components etc. ・The embedded layer can be thickened with a narrow pitch between posts ⇒ Favorable for built-in parts

MCeP® is ideal for device embedded packages.

Outline

- Introduction of device embedded package
  - MCeP® introduction
- **Requirements for power modules**
- Introduction of LF-MCeP
  - Heat dissipation
  - Miniaturization / Modularization
  - Substrate routing efficiency
- Package Characteristics
  - PKG warpage
  - MSL Result
- Conclusion
  - PKG structure road map
  - Future development challenge

Request to Power Supply Module PKG

Heat dissipation requirements

Miniaturization / Modularization

Module for Power Supply Package

Increased substrate routing efficiency

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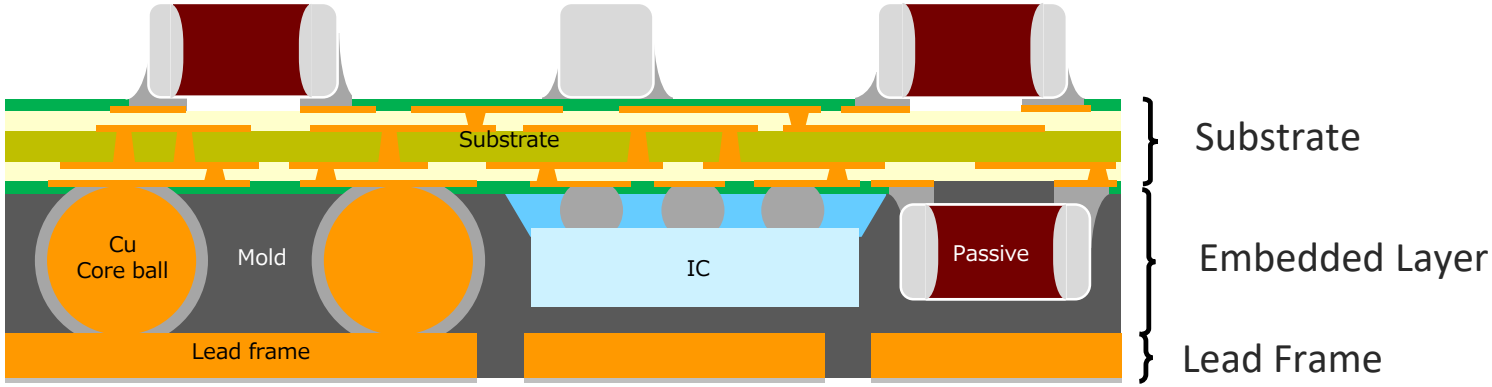
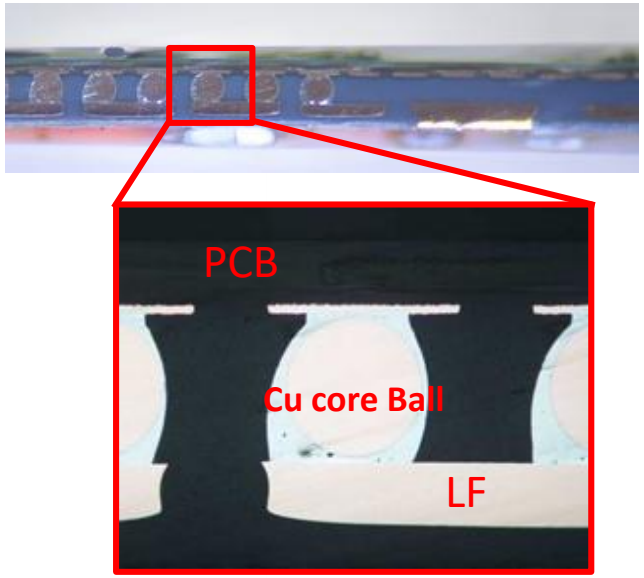
LF-MCeP Introduction

LF-MCeP : Lead Frame Molded Core embedded Package



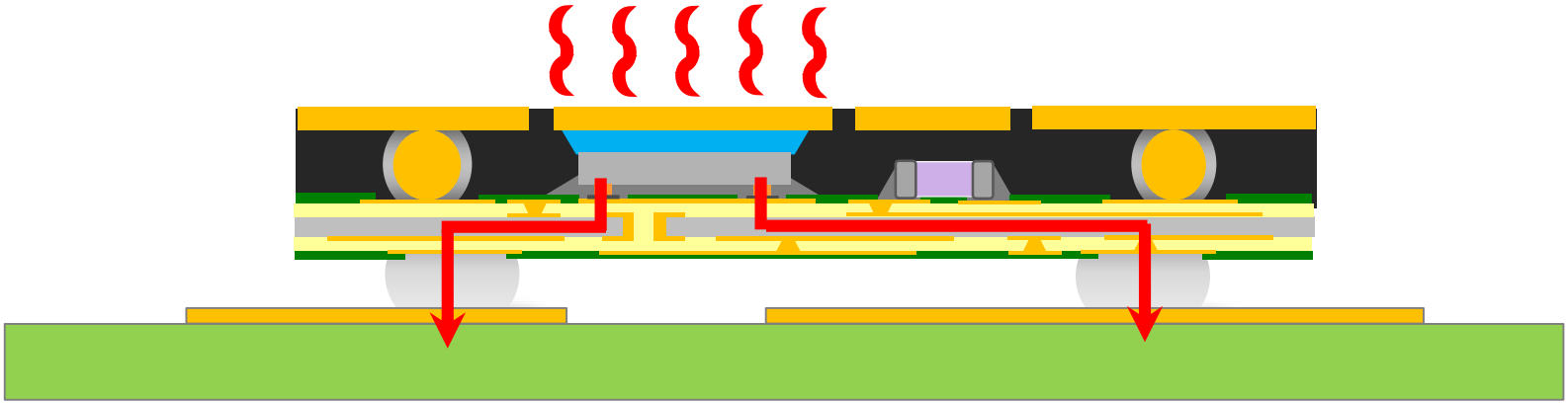
LF-MCeP Advantages

- Can use existing MCeP® assembly process
- Heat dissipation is advantageous by using LF
- Miniaturization / modularization possible
- Substrate routing efficiency
  (can shorten routing path)
- Low package warpage

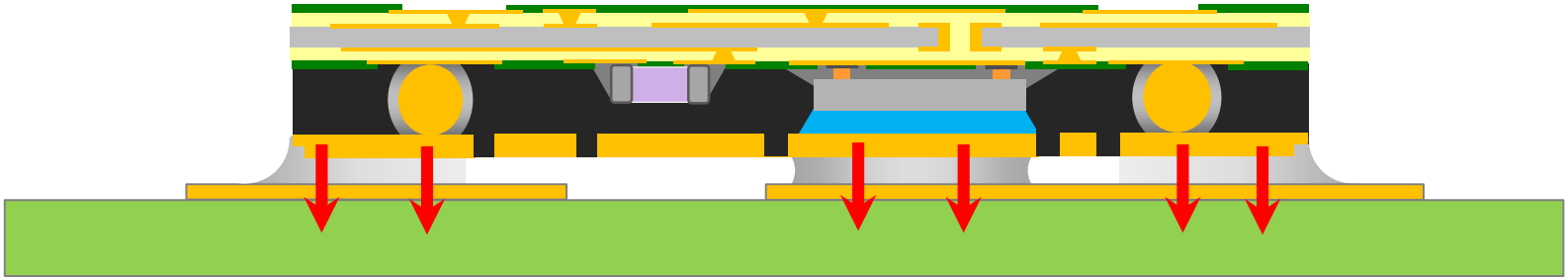


Heat Dissipation Advantage (Mounting Application)

#1 : By using LF as the PKG TOP surface, LF can be used as a heat sink.



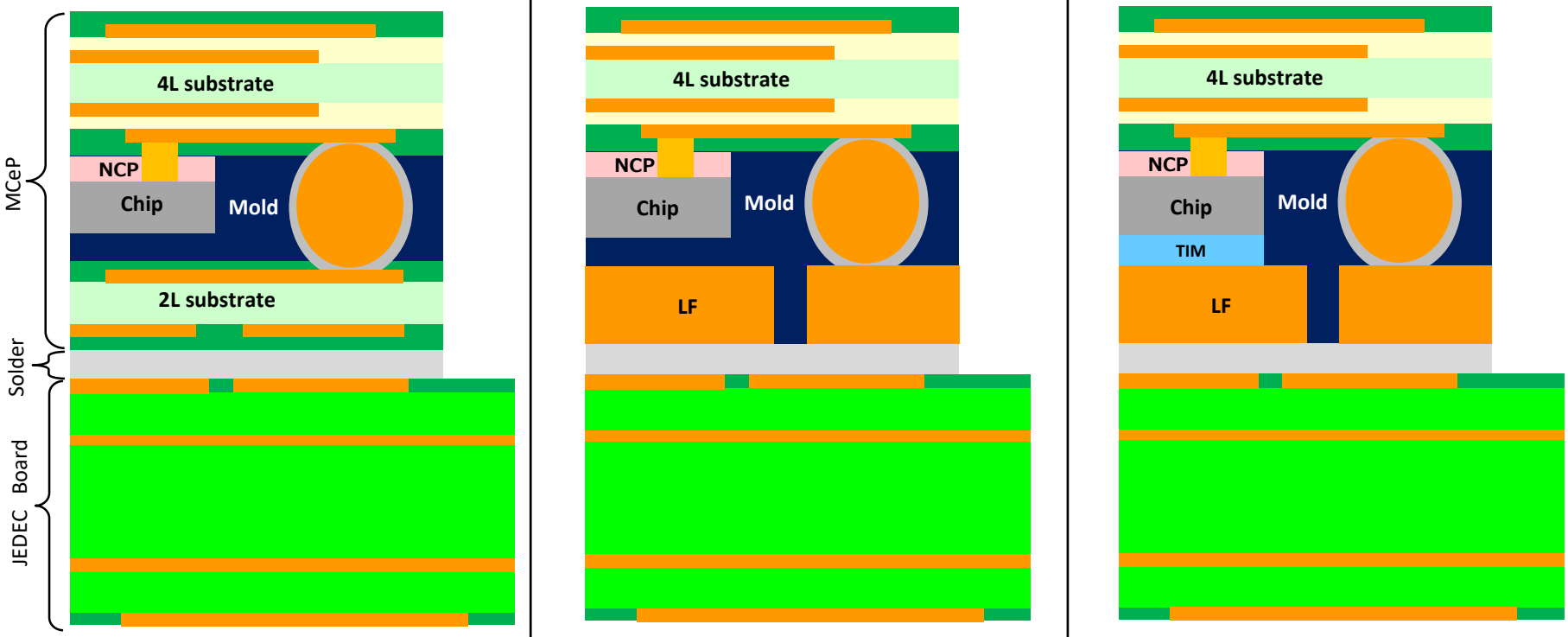
#2 : By making LF PKG Bottom, heat dissipation from the bottom of the PKG can be improved.



Heat Dissipation Advantage (Thermal Simulation)

■ Analysis model

Leg.1	Leg.2	Leg.3
MCeP (2L+4L)	LF-MCeP (LF+4L)	LF-MCeP (LF+4L) with TIM



Dimension

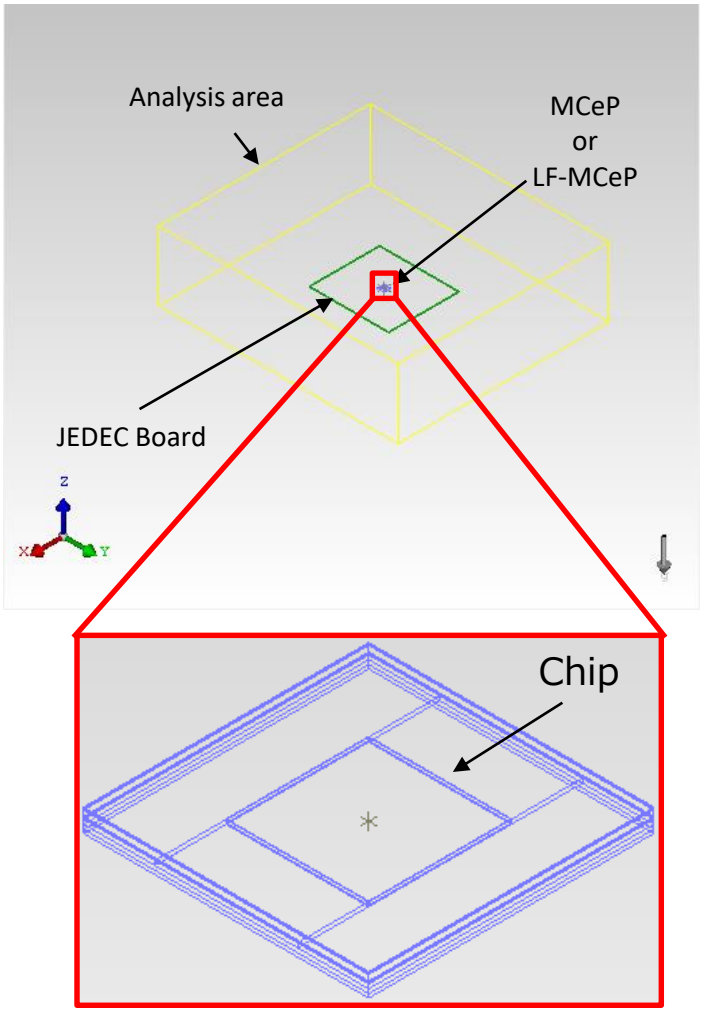
PKG size: 10 x 10 mm
Chip size: 5 x 5 mm

Thickness

4L Substrate : 0.37mm
2L Substrate : 0.15mm
LF : 0.15mm
JEDEC Board : 1.6mm

Heat Dissipation Advantage (Thermal Simulation)

Analysis conditions



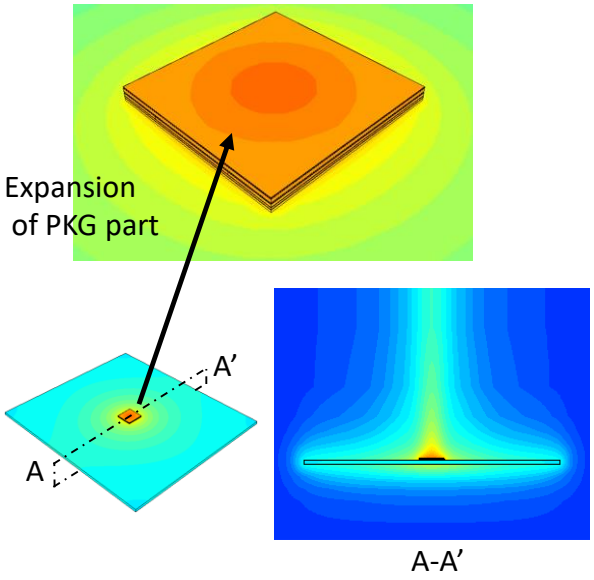
Solver	FloTHERM v12.0
Analysis type	Steady state thermal fluid analysis
Analysis area	304.5x342.9x100mm
Ambient environment	25 ℃, no wind speed
Radiation	Yes
IC Power	Chip：2.0W

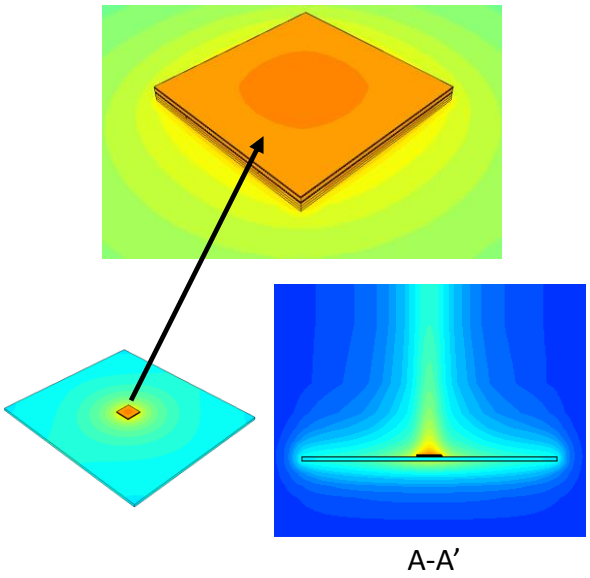
Parts	Thermal conductivity [W/m･K]	Radiation ratio
Chip	150	- - -
Solder	64.2	- - -
LF	220	- - -
TIM	30	- - -
Mold	3	0.9
NCP	0.54	- - -
SR	0.23	0.9
Core	0.73	- - -
Prepreg	0.73	- - -
JEDEC board	0.38	0.9
Air @ 25degC	0.026	- - -

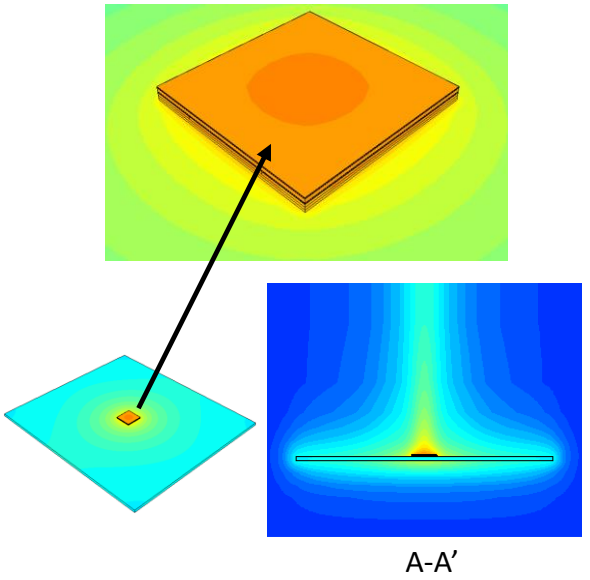
Heat Dissipation Advantage (Thermal Simulation)

■ Analysis result 1 : θja , Chip temperature

Leg.1	Leg.2	Leg.3
MCeP (2L+4L)	LF-MCeP (LF+4L)	LF-MCeP (LF+4L) with TIM
θja：24.5[K/W] Chip temperature：74.1℃	θja：22.9 [K/W] Chip temperature：70.9℃	θja：22.7[K/W] Chip temperature：70.4℃







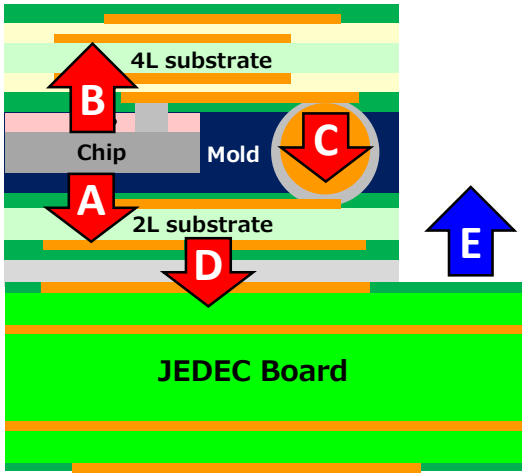
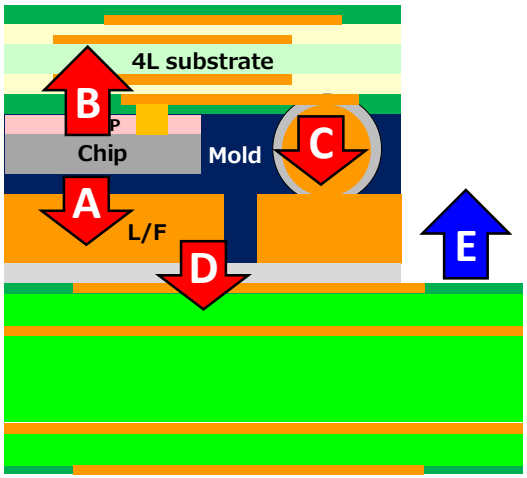
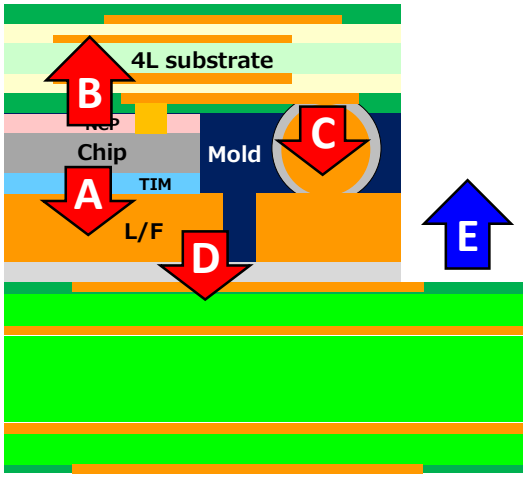
- The chip temperature and thermal resistance θja of LF-MCeP are lower than MCeP.
- When the TIM material is applied, the chip temperature and the thermal resistance θja are further reduced.

Heat Dissipation Advantage (Thermal Simulation)

: Conduction
: Radiation

■ Analysis result 2 : Thermal flow analysis

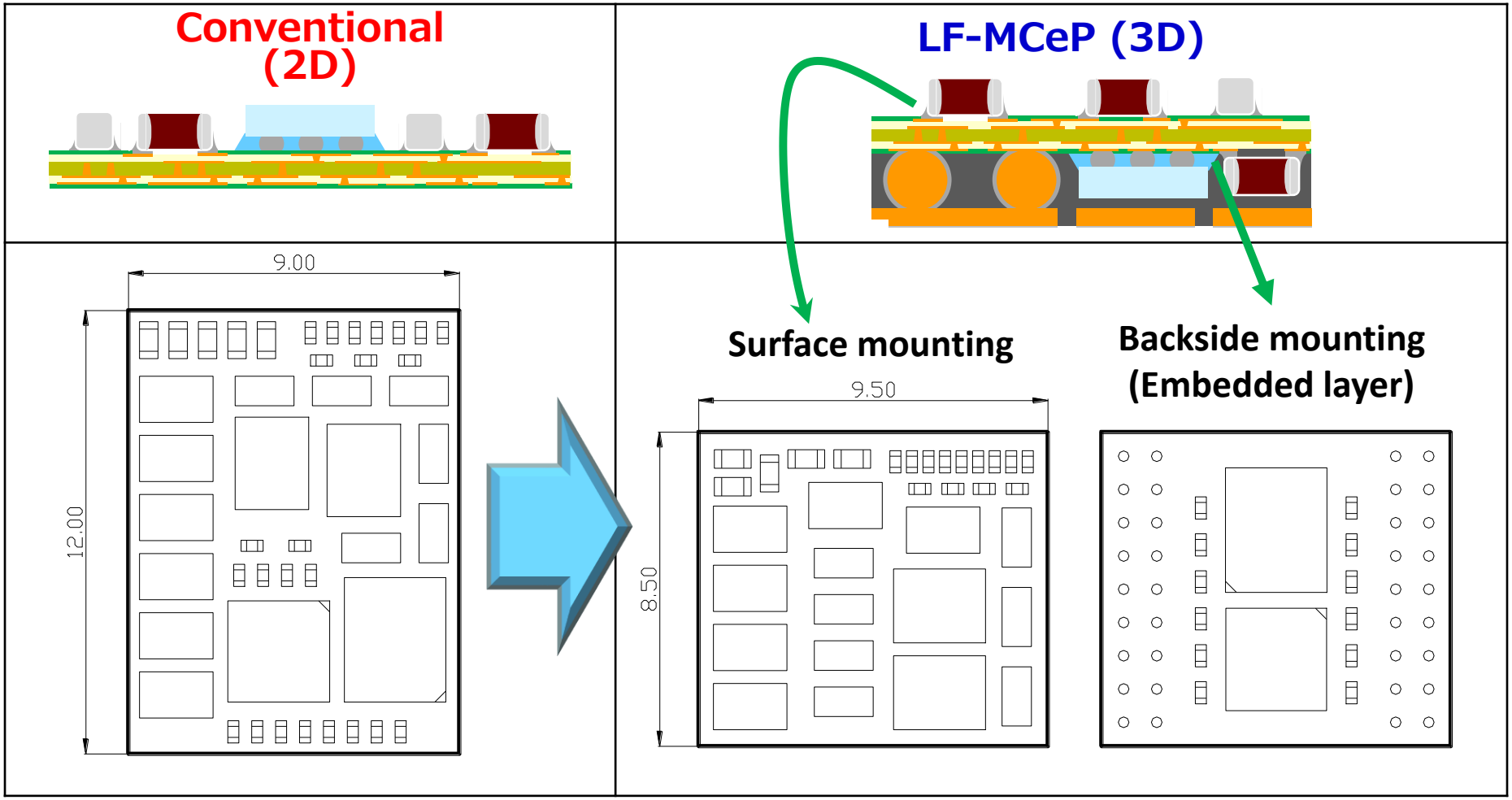
Unit: [W]

	Leg.1	Leg.2	Leg.3
	MCeP (2L+4L)	LF-MCeP (LF+4L)	LF-MCeP (LF+4L) with TIM
			
A	0.953	1.333	1.333
B	0.988	0.632	0.547
C	0.978	0.598	0.510
D	1.916	1.920	1.920
E	1.913	1.916	1.917

- Most of the chip heat is dissipated from the JEDEC board.
- In the case of LF, the chip heat is transferred directly to the JEDEC board via LF.

Miniaturization / Modularization

■ PKG area comparison Module PKG vs LF-MCeP

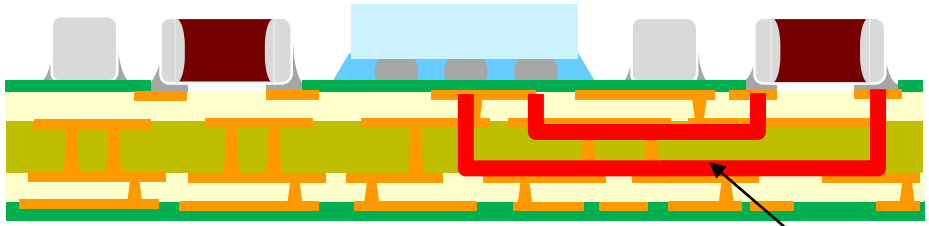


Shrink of 25% is possible in the PKG area ratio

Substrate Routing Efficiency

■ By placing components on the front and back of the substrate, the routing path between components can be shortened.

Conventional (2D)



LF-MCeP(3D)

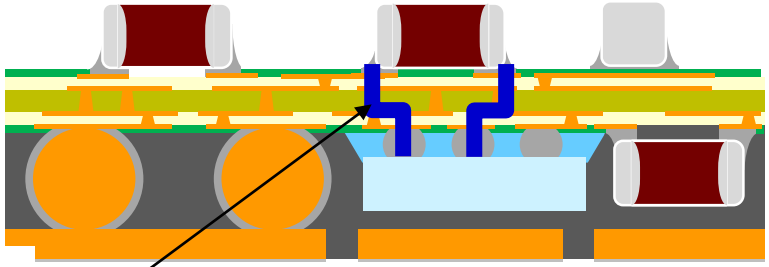


Image of routing path

Calculation results of routing path

⇒ Routing path can be shortened to about 1/4

■ Calculation conditions

- WLCSP : BGA 0.50mm Pitch
- SMT Size : 0603[mm]
- 4L Substrate : t=0.37mm

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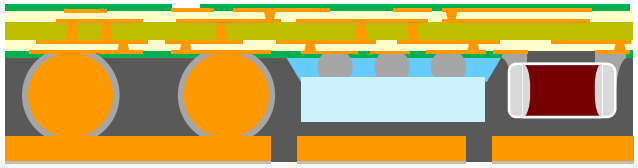
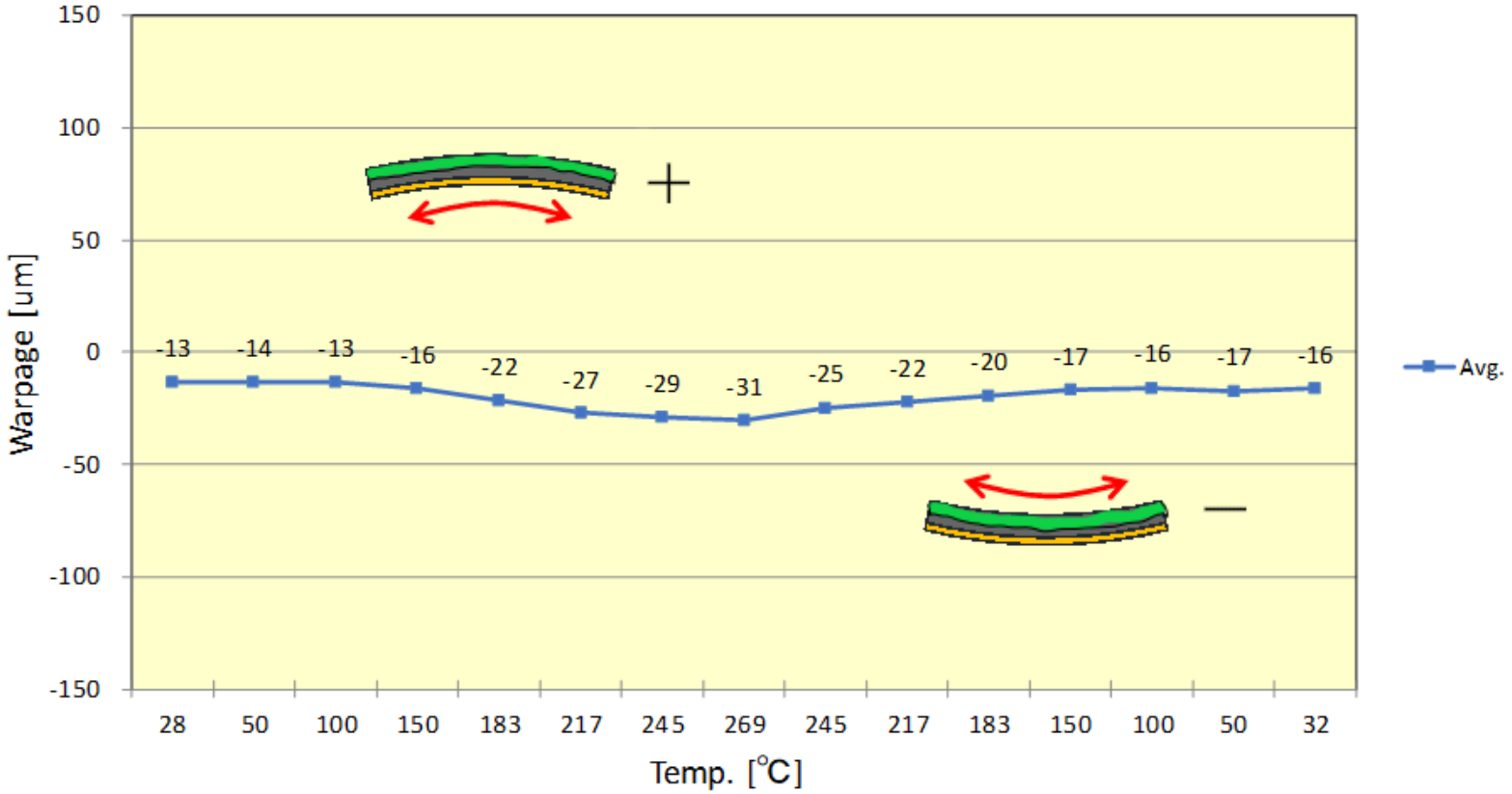
PKG Warpage

■ Sample

- PKG size: 9.0mmSQ.
- Embedded chip and component



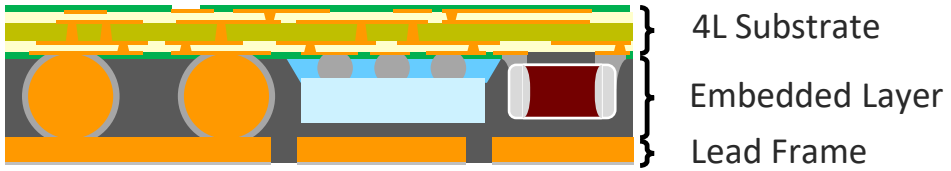


Small warpage range from room temperature to high temperature
Low warpage PKG possible

MSL Result

■ **Sample**

- **PKG size: 9.0㎜SQ.**
- **Embedded chip and component**



MSL	Test condition	N	Result (SAT)
MSL3	Bake125℃24h ⇒30℃60%192h ⇒260℃MaxReflow✕3	10pcs	10 / 10pcs PASS

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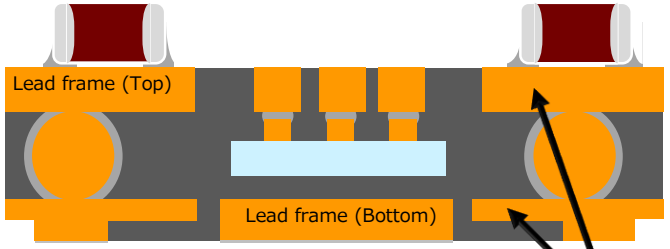
PKG Structure Road Map

High power module

Adoption of Cu Cube

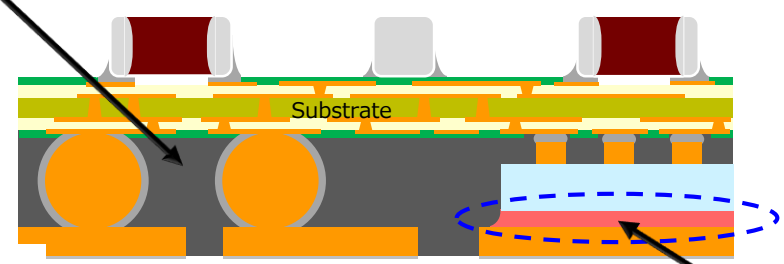
- Improved thermal conductivity of upper and lower substrates.
- Stable connectivity and lower electrical resistance.

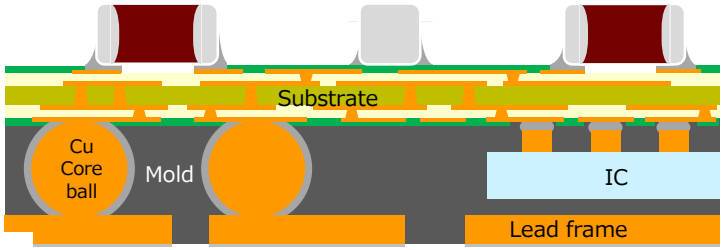


MCeP adoption of LF + LF

- Improves heat dissipation from the top and bottom of the PKG

High thermal conductive mold resin





Thermally conductive resin is used on the back of the chip

Voltage [V]

Electric current [A]

Future Development challenge

■Summary

- Use of LF can improve heat dissipation of PKG.
- Can be miniaturized and modularized by embedding components.
- The routing length can be shortened by 3D PKG structure.

■ Improved heat dissipation

- Development of high thermal conductive mold resin.
- Development of high thermal conductive resin between chip and LF.

Thank you for your attention