

# Power delivery in IoT applications with on device AI

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#### AI is Moving from Cloud to Edge Efficient On-Device AI a Must



Ample computing resources Availability of big data Better model accuracy Redundancy Security Best for training

Low latency, real-time Always-ON, continuous

Lower power
Privacy
No data overload
Best for inference

# 100X Lower Power Edge Computing

Miniaturized single chip solution with 100x improvement in performance and 2x reduction in cost

#### **Atlazo Innovations**

# Al @ the edge Ultra-low power design

#### Atlazo Value proposition

+10X Lower Computing Power

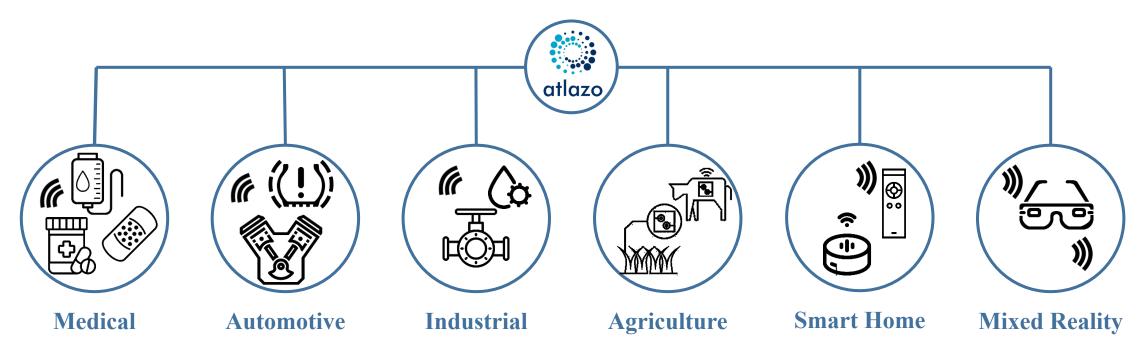
+10X Lower Sensing Power

+2X Lower Communication Power

+2X Smaller Board Space

# Low Cost Low Power AI at the Edge

Own the entire hyper-low power AI SoC and software space Billions of battery powered devices with intelligent monitoring everywhere



Precise sensing accuracy using dynamic calibration and fusion Hyper-low power inference and analytics in hard to reach and disposable parts and systems

#### PMIC Requirements for Hyper Low Power IoT

Ultra low load currents down to few uA

Computing workload under 1mA and always-on Wireless interface under 10mA and often-off

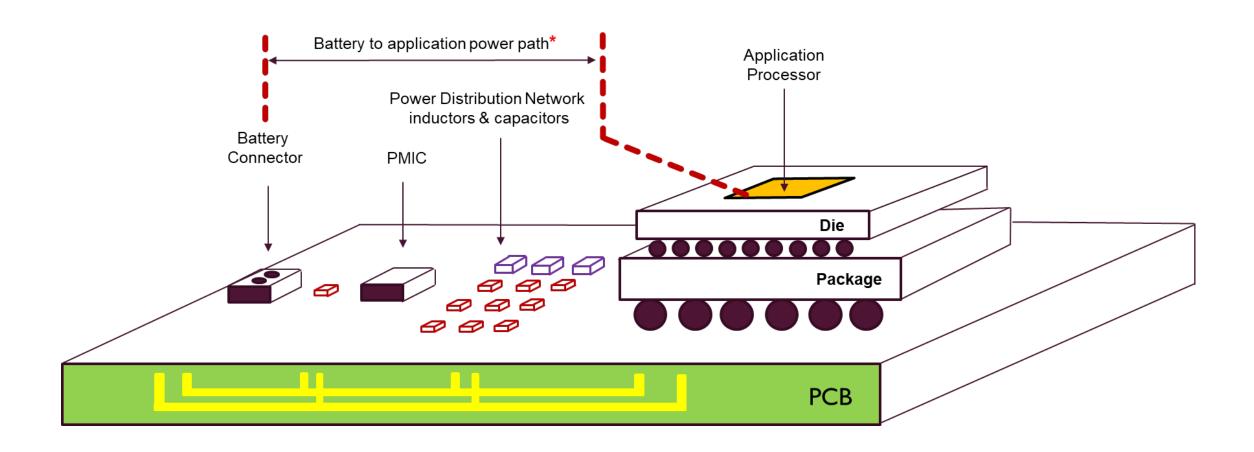
Low voltage operation down to 0.4V

Low area and low cost

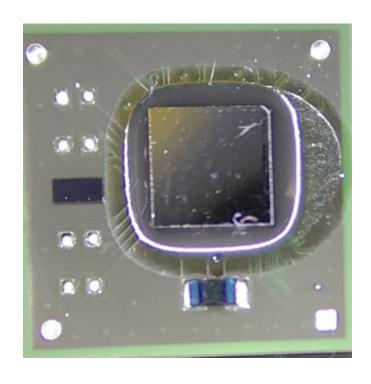
Spur management to mitigate system noise

Integrated charger, if applicable

#### Traditional PMIC



#### Atlazo ULP AI SoC with PMIC



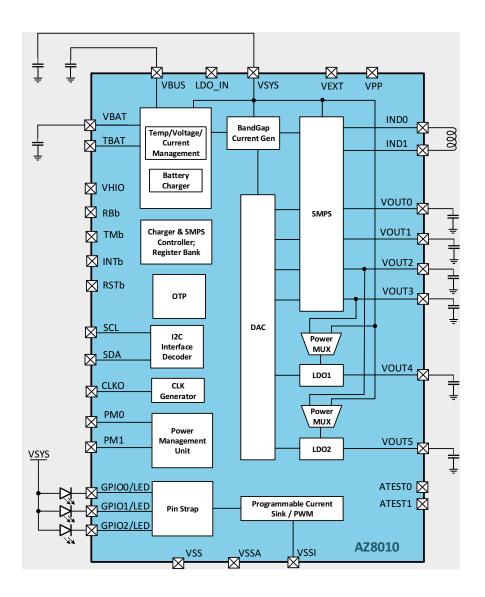
Novel digital controller and topology to work efficiently in low currents

Programmable spur management to mitigate system noise

Reduced number of passives and PCB area

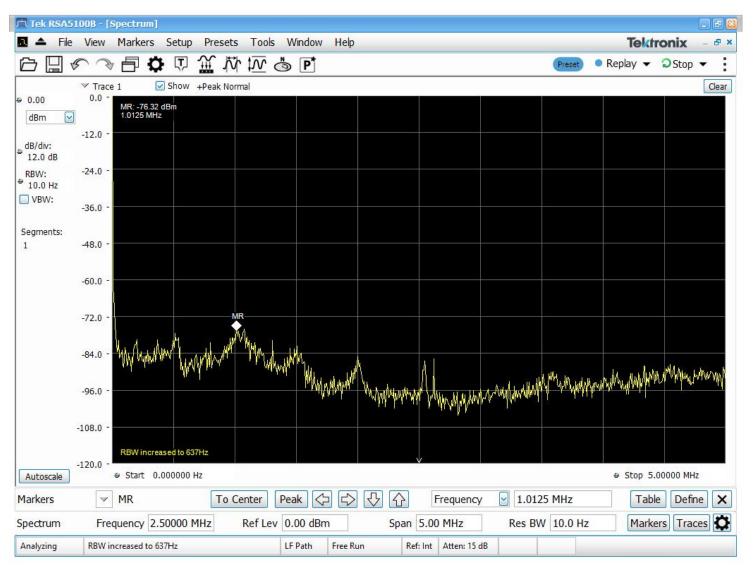
Sub-threshold design to lower quiescent current

#### Atlazo ULP PMIC



- Efficient power and battery management solutions featuring
  - Flat efficiency
  - >50% reduction in PCB area
  - Regulate down to 1uA load
- < 1uA operating quiescent current</p>
- 4 programmable SMPS outputs
  - 3 step down outputs
  - 1 step down /step up output
- 2 programmable LDO outputs
- Small integrated inductor and capacitors

# Silicon Result of Spur-Free Atlazo PMIC



### Atlazo PMIC Spur Management

#### SNR Improvement

Competitor
PMIC

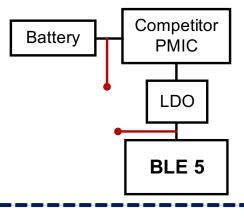
Wireless
Transceiver

RXout

RXOUT

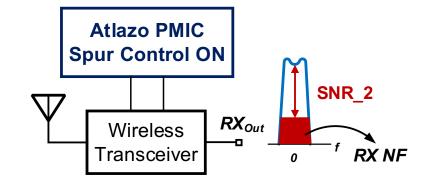
RX NF

#### Efficiency Improvement

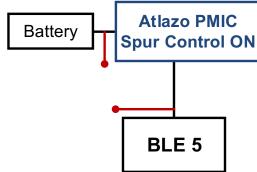


Atlazo

**Competitor** 

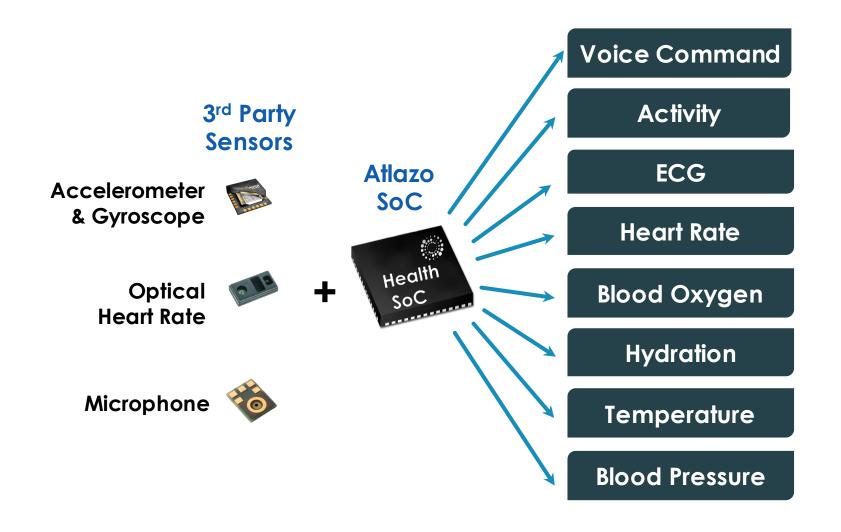


- Receiver SNR degrades due to the large in-band Spurs in PMIC
- Atlazo enables the technology to avoid SNR degradation due to PMIC Spurs

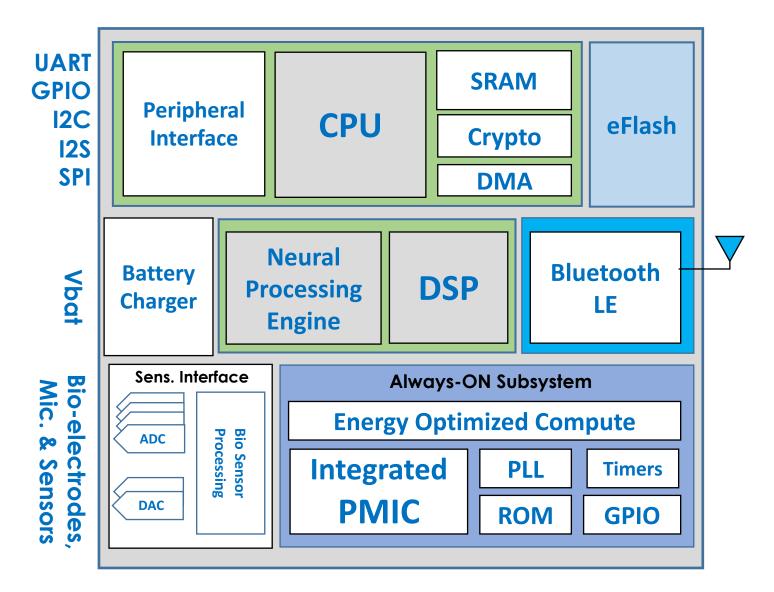


- To attenuate Spurs in PMIC, despite inferior efficiency LDO is added to the path of PMIC to the RFIC.
- Atlazo enables the technology to removes the in-band Spurs and avoid the LDO and the efficiency degradation

#### Atlazo ULP AI SoC Platform



#### Atlazo ULP AI SoC Platform



#### Thank You!