"A Low Profile 2.5 SIP Package Technology using Thin ETS Substrate, for Wearable Applications"

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Outline

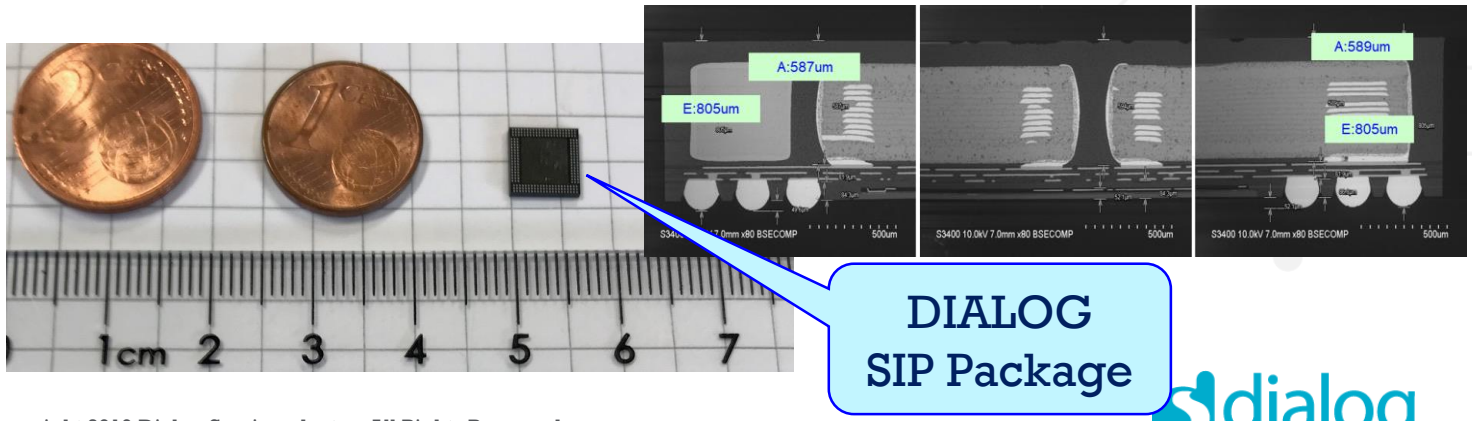
- Introduction of SIP Package Technology Dialog
- Technology Market Driver
- Evolution of SIP Technology
- Advantages & Differentiator of DLG 2.5D SIP vs other SIP Technology in the market
- SiP Package Technology Achievement
- Summary

Introduction

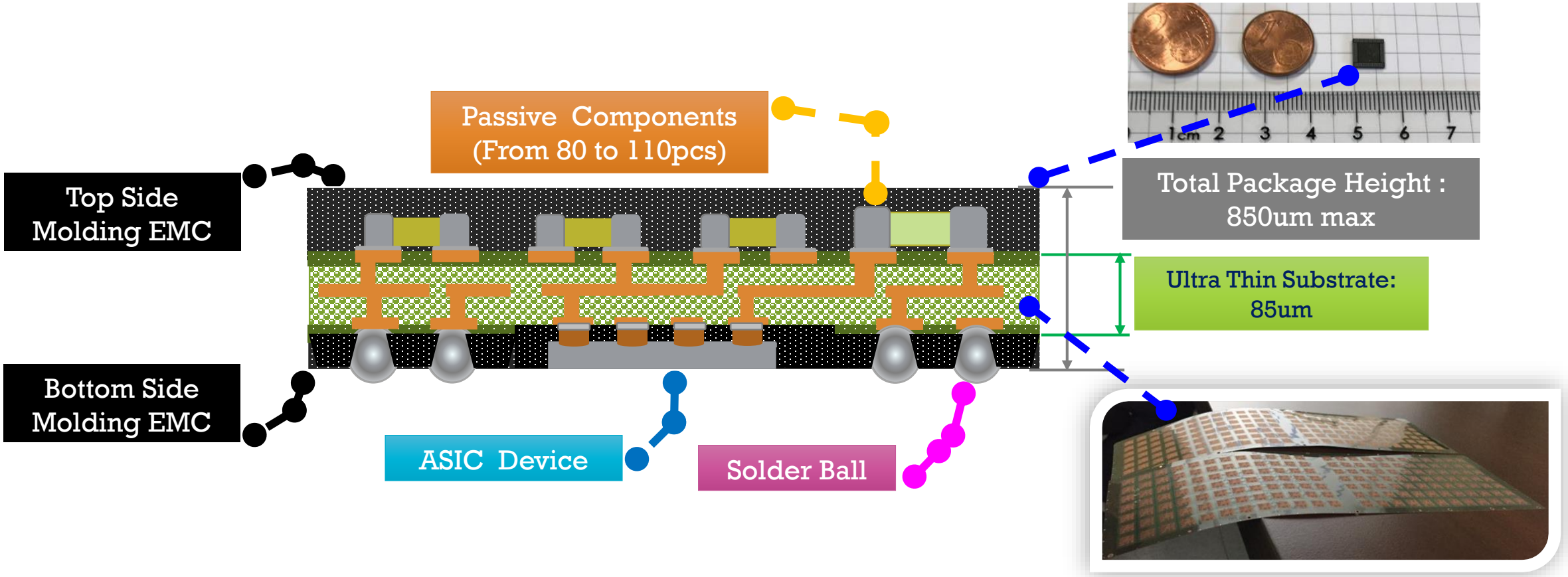
“A Low Profile 2.5 SIP Package Technology using 85um Thin , “ETS” Embedded Trace Substrate

Introduction :

- ✓ A 2.5 D **S**ystem **I**n **P**ackage is provided and structured using a **V**ery **T**hin **(ETS) E**mbedded **T**race **S**ubstrate in 3 or 4 layer structure having interconnect traces therein.
- ✓ One or more passive component mounted on one side connected to substrate trace pads and encapsulated by molding process on one side , and an ASIC die mounted on an opposite side of the embedded trace pads and embedded in a second molding encapsulation steps .
- ✓ Electrical connections were made between silicon die metal pads layer with Cu Pillar Structure ,and solder balls mounted through Mold Via openings connected to the Substrate trace pads that serves as Package I/O‘s.
- ✓ A 2.5D Ultra Thin SIP Package that have a Total Stack -up of 850um .



“ A Low Profile “2.5D SIP Package Technology using Thin ETS Substrate



- DLG Double Side Molded Thin ETS-SiP Package with Patent Pending ;
  - US Patent Application **15718080**
  - German Patent Application **102018207060.1**

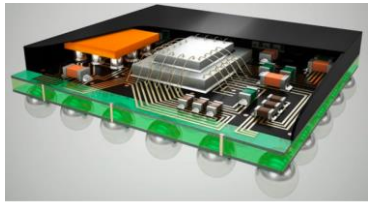
DIALOG Market Driver

DIALOG Technology Market Driver

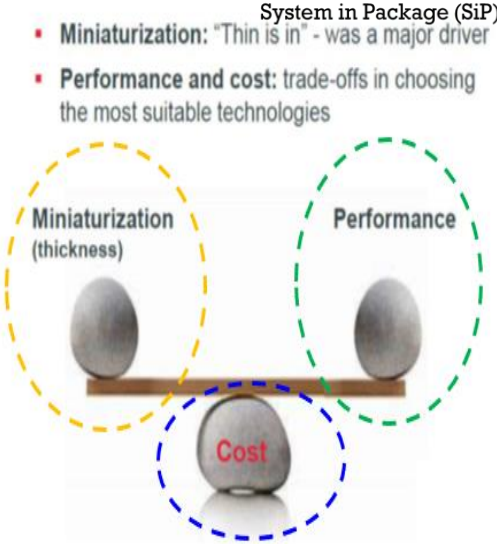
Driving Force In The Market

1) Lower cost, increase performance and functionality through advanced packaging
2) Multi-die packaging and System in Packaging (SiP) for functional integration
3) Form factor requirement (Smaller body size/ Thinner package thickness)

Source : IDC



System in Package (SiP)

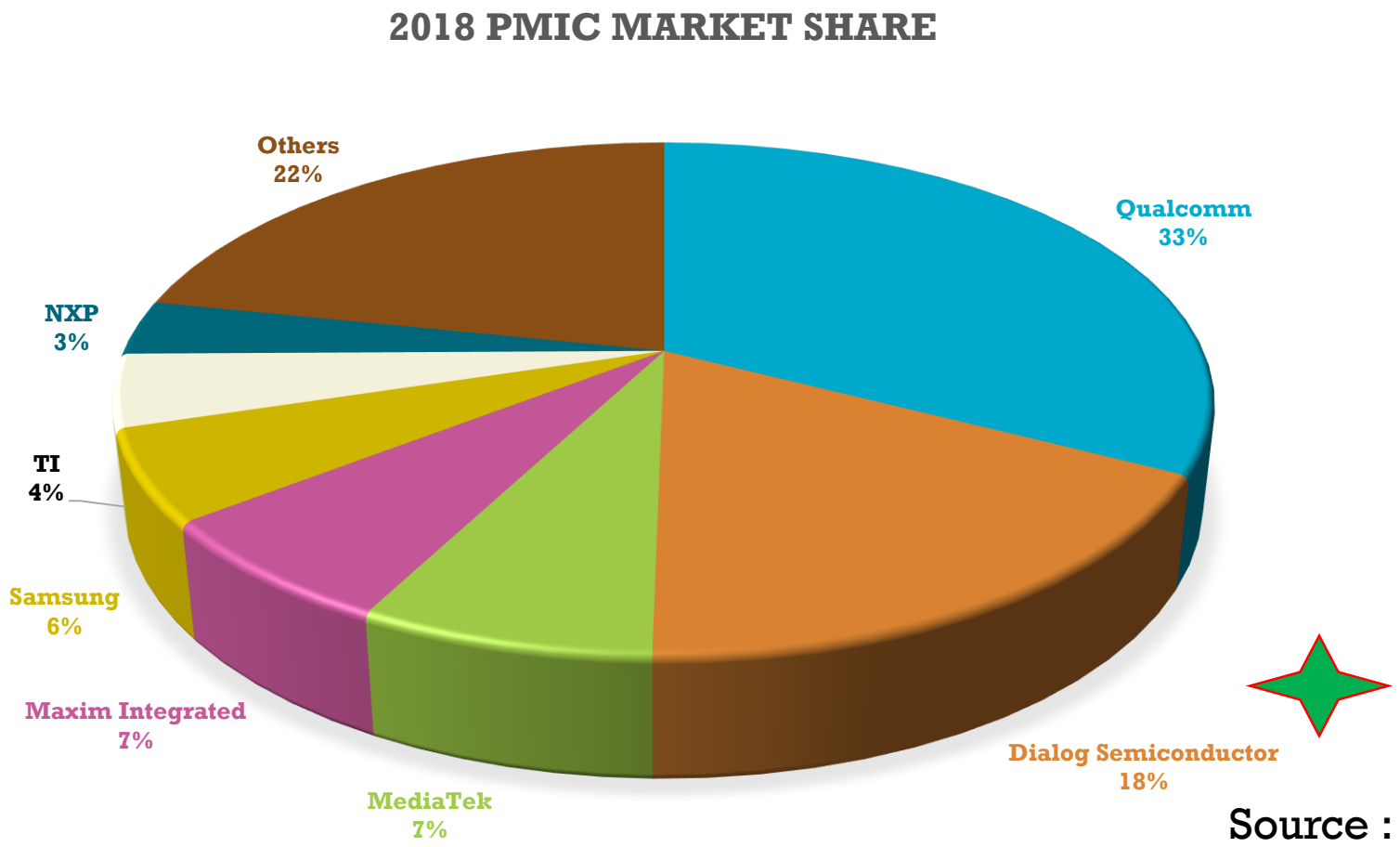


Source : Yole

Source : IDC

Power Management Market Share

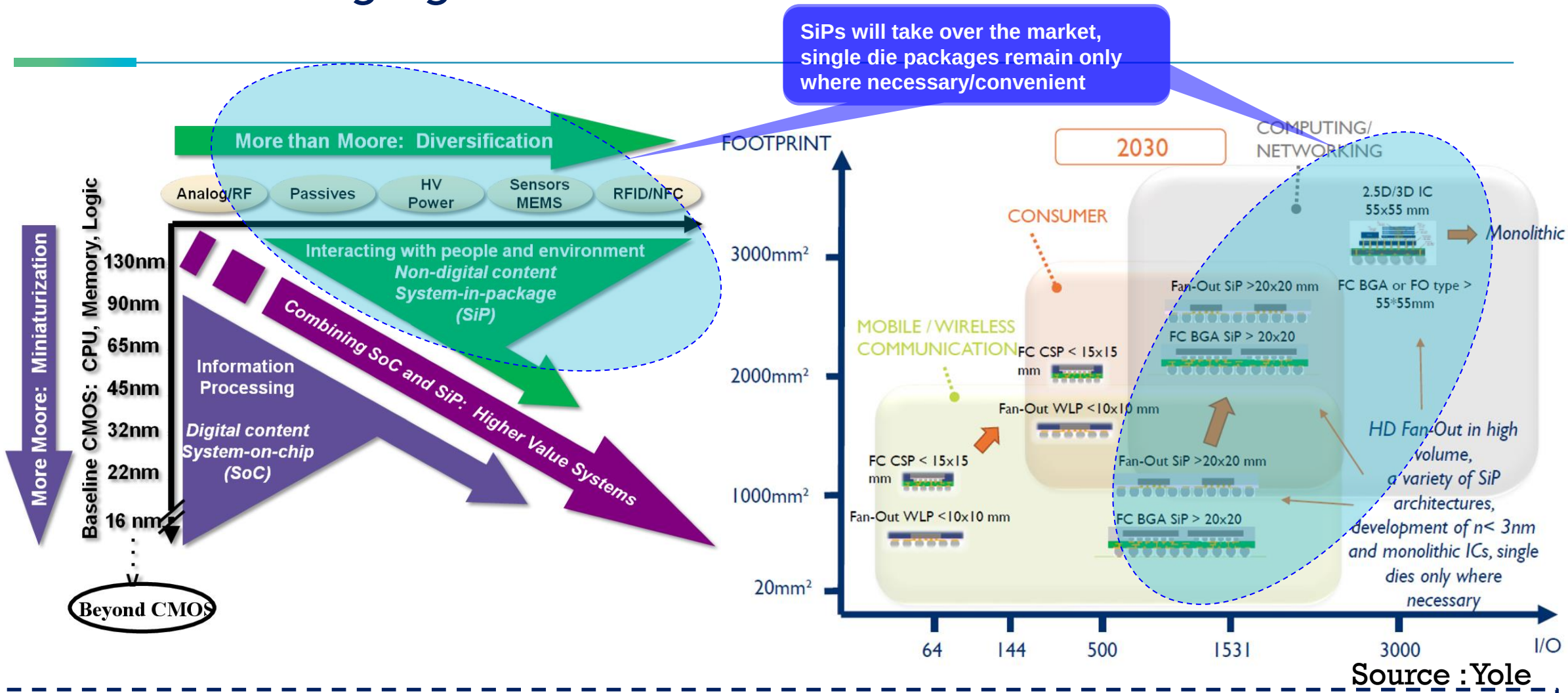
Dialog #1 Pure Play PMIC Supplier



Source : IHS Markit, Q2 2019

SIP Technology Evolution

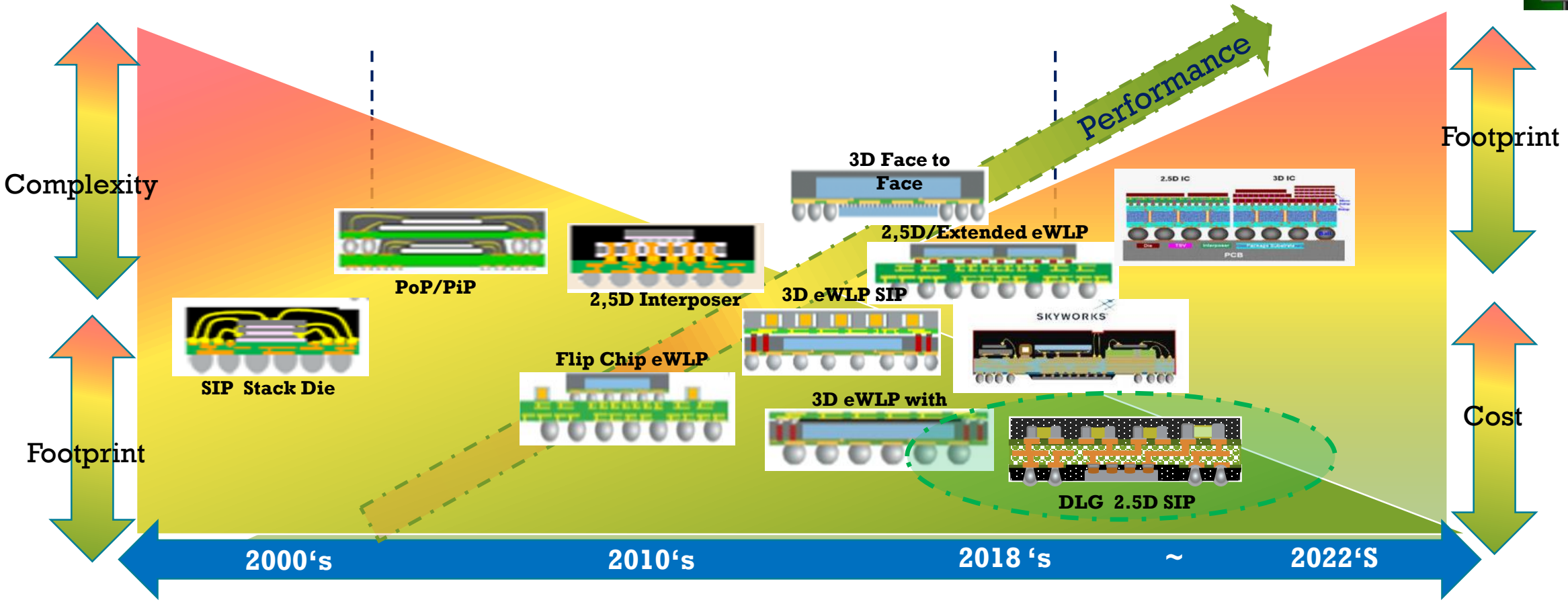
Advanced Packaging Market Diversification needs



Source : Yole

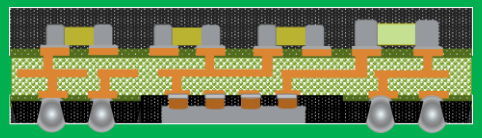
- OSATs are directing considerable effort to developing advanced wafer level & 3D IC packaging capability to support requirements for scaling & density/ Development of 2.5D/3D assembly capability as market grows
- With a variety of SiP architectures and technologies available, assembly and packaging houses will be distinguished by SiP customization offers/capabilities and turn around time

DLG SIP Packaging Evolution & Differentiator vs the Market



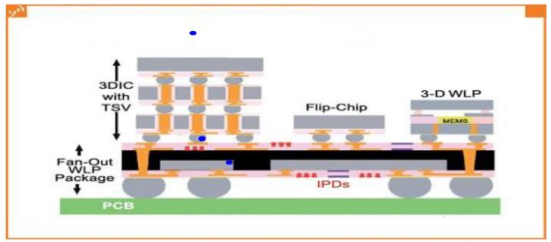
DLG SiP Snapshot vs other 2.5 D (ex . eWLP SIP) in the Market)

Dialog 2.5D SIP Technology



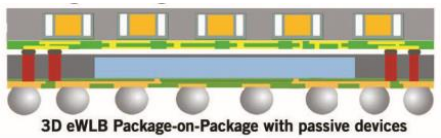
- 3 or 4 Layer Cu Trace
- High Integration of Passive (50 ~100pcs)
- Double Sided Package
- Ultra Thin Interconnect carrier
- Low Stand-of Z Package
- PMIC Application

Ex. Other Market References



Cross-Section of Advanced Packaging Assembly Methods
Image: Yole Development

Source : Yole

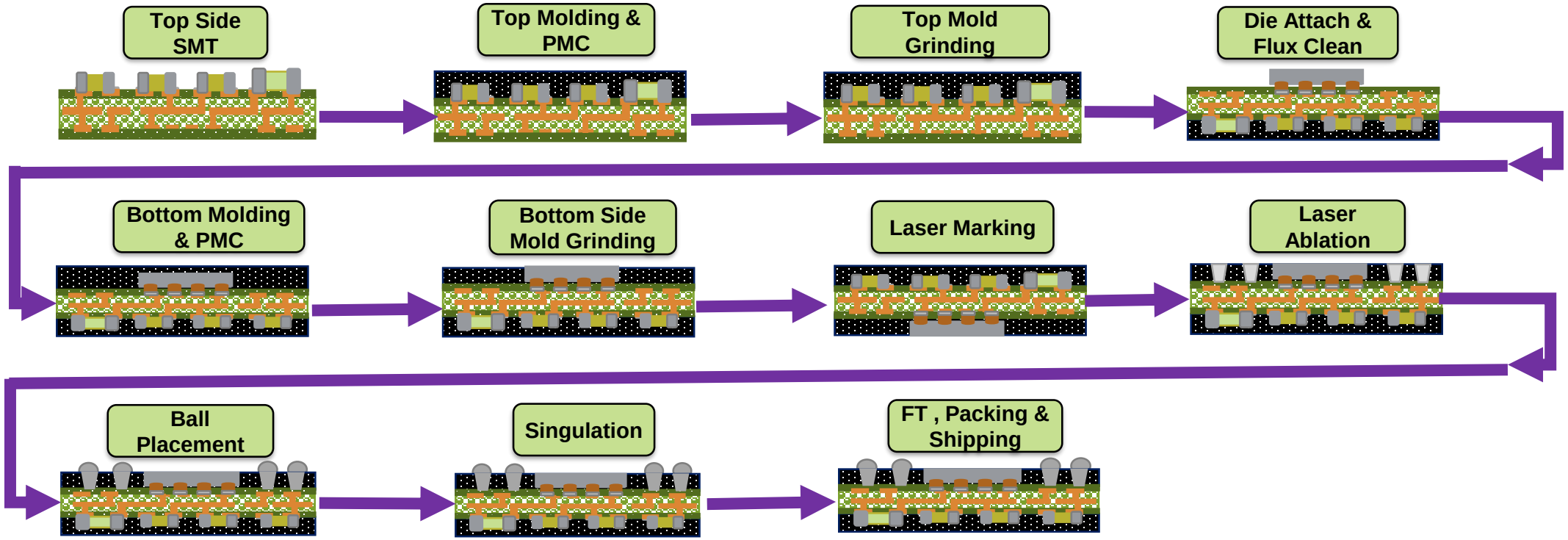


Source : STATS

- What Dialog ETS SIP 2.5D Pakages can offer ;
  - ✓ Lower Complexity vs the 3 Layer eWLP & TSV Technology
  - ✓ Lower Cost vs FO eWLP & TSV SIP Technology
  - ✓ Lower Manufacturing Cycle time vs the 2,5 0r 3D Package technology (FO or TSV Package Intterconnect Type)
  - ✓ Can Offer Higher Integration of Passive Components from 50 to 100 + Components in a SIP Package Structure
  - ✓ Can Offer Smaller Footprint of Package SIP similar to eWLP or 2.5D SIP Package Alternatives ..

DIALOG SIP Development Concept

Dialog Concept Flow for Double Side Thin ETS-SiP Package

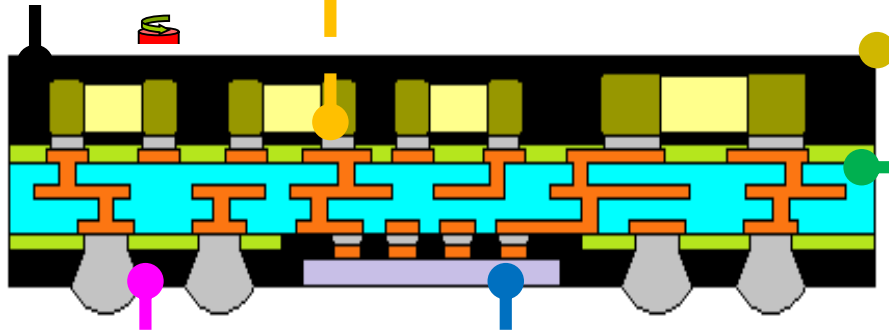


Challenges - SIP Development

Challenges - DLG Double Side Molding ETS-SiP Technology

✓ Mold UF Control (Delam/ Void performance)
✓ Strip form grinding for thickness control

✓ Stand off height control for Passive Components
✓ Mold Flow ability underneath the components



✓ Ultra thin package height control
✓ Warpage behavior & control

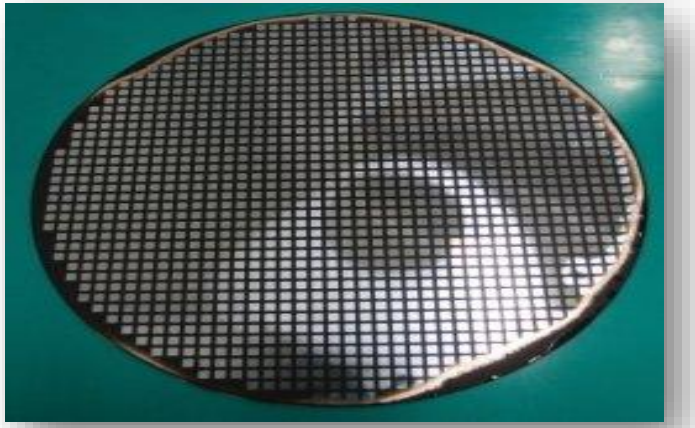
✓ Ultra thin substrate handling
✓ Assembly & Process Manufacturability
✓ Yield

✓ ASIC Die thickness control
✓ Strip form grinding for composite materials (Si Die/EMC)

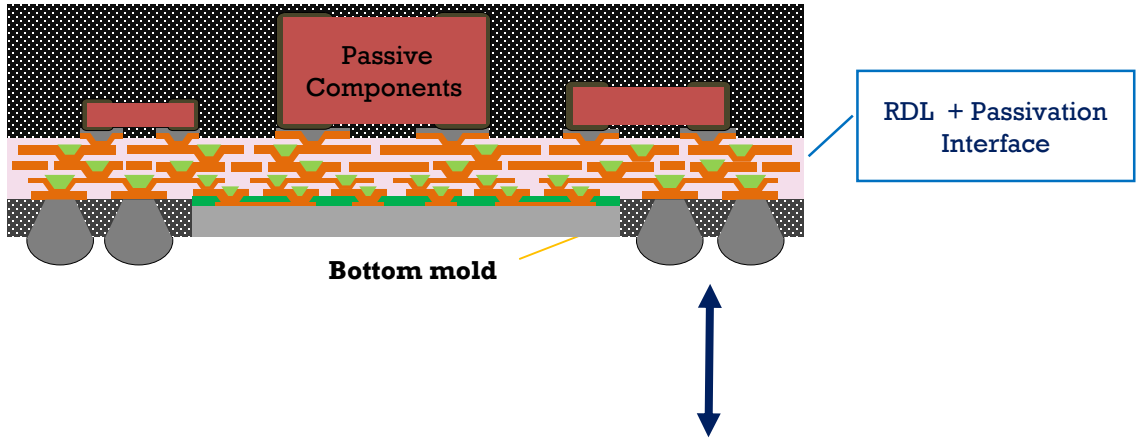
✓ Laser Ablation performance (pad damage/ surface cleanliness)
✓ Via hole profile control
✓ Solder ball protrusion control

SIP Alternative Technology

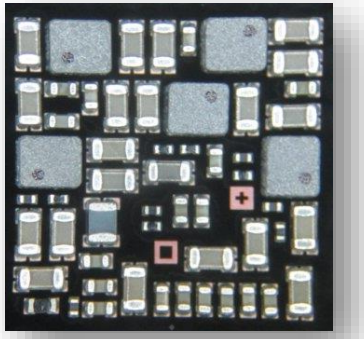
DLG SiP Alternative Technology explored



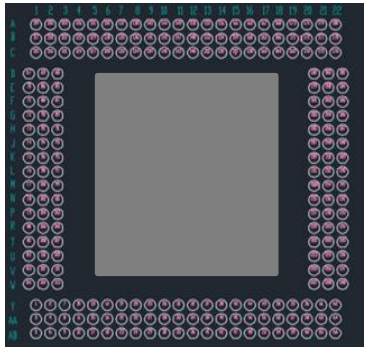
300mm wafer fan-out reconstituted



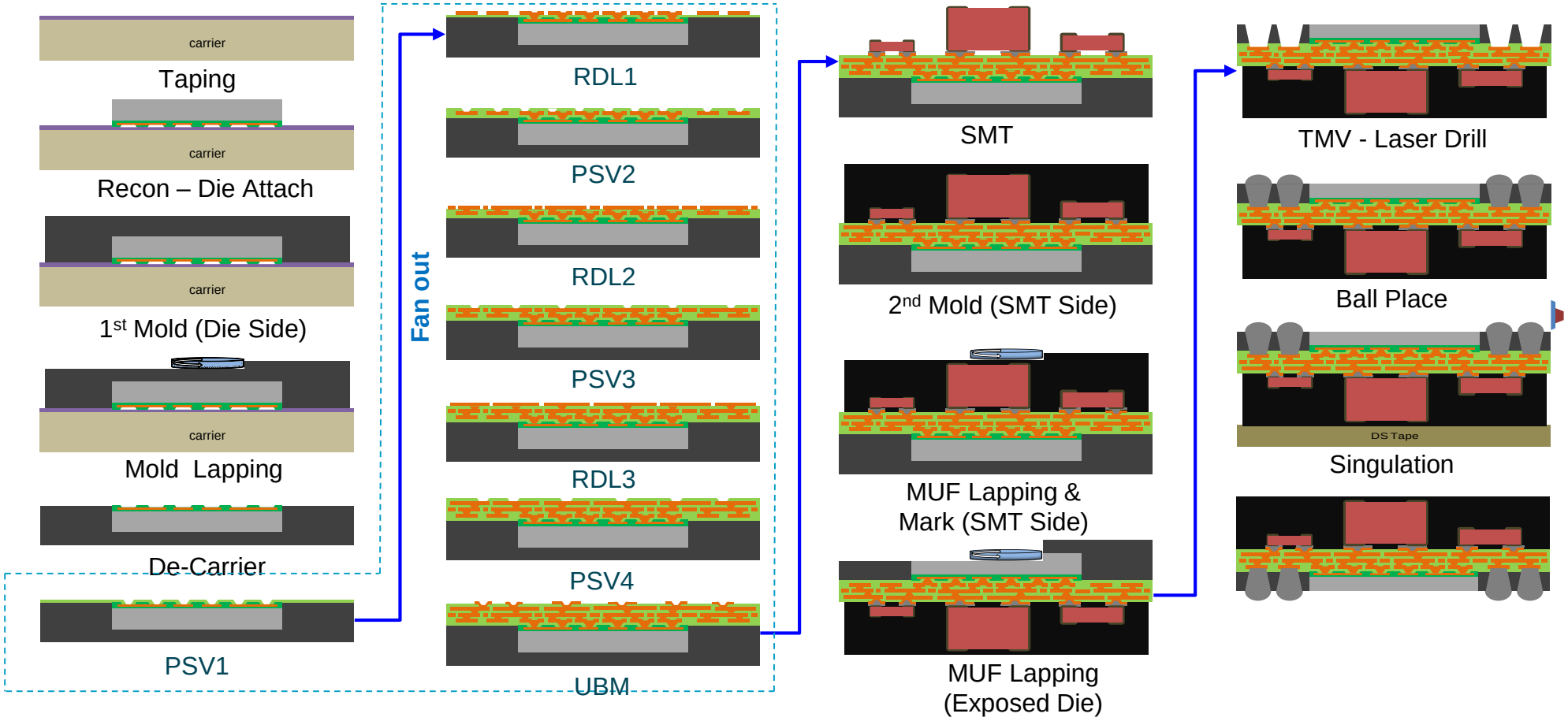
SMT – Top Side



Ball Footprint – Bottom Side



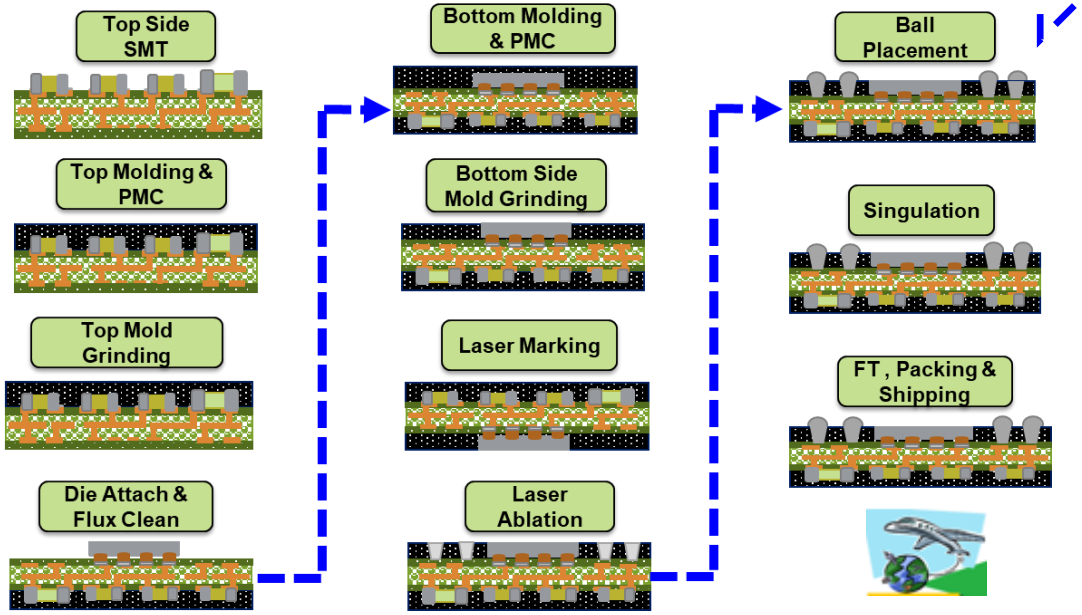
Dialog Concept Flow for Double Side Thin eWLP SIP Concept

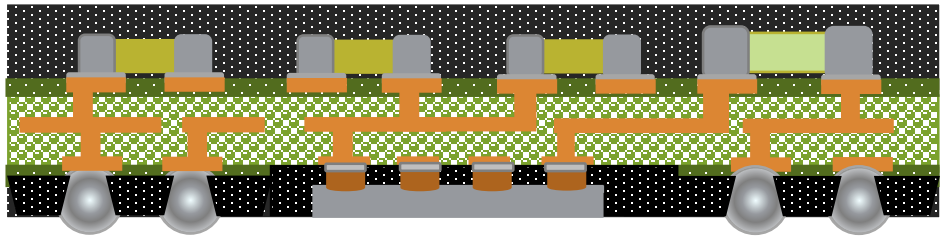


DLG SIP Technology Differentiator

SIP Concept Flow Differentiator

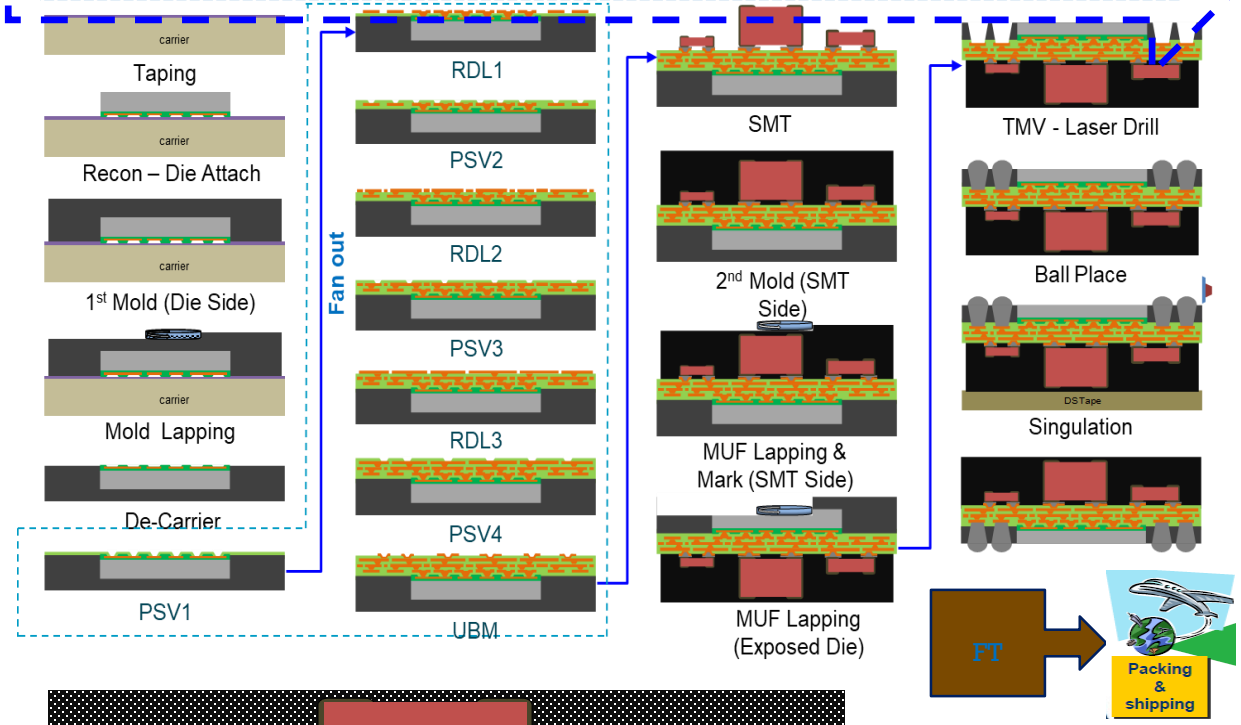
Total of approx 3 Weeks Process Cycle Time (Eng'g Stage)

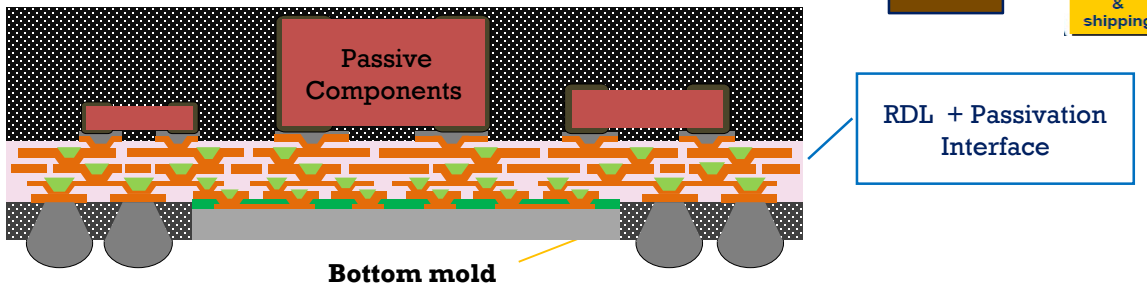




ETS SIP Technology

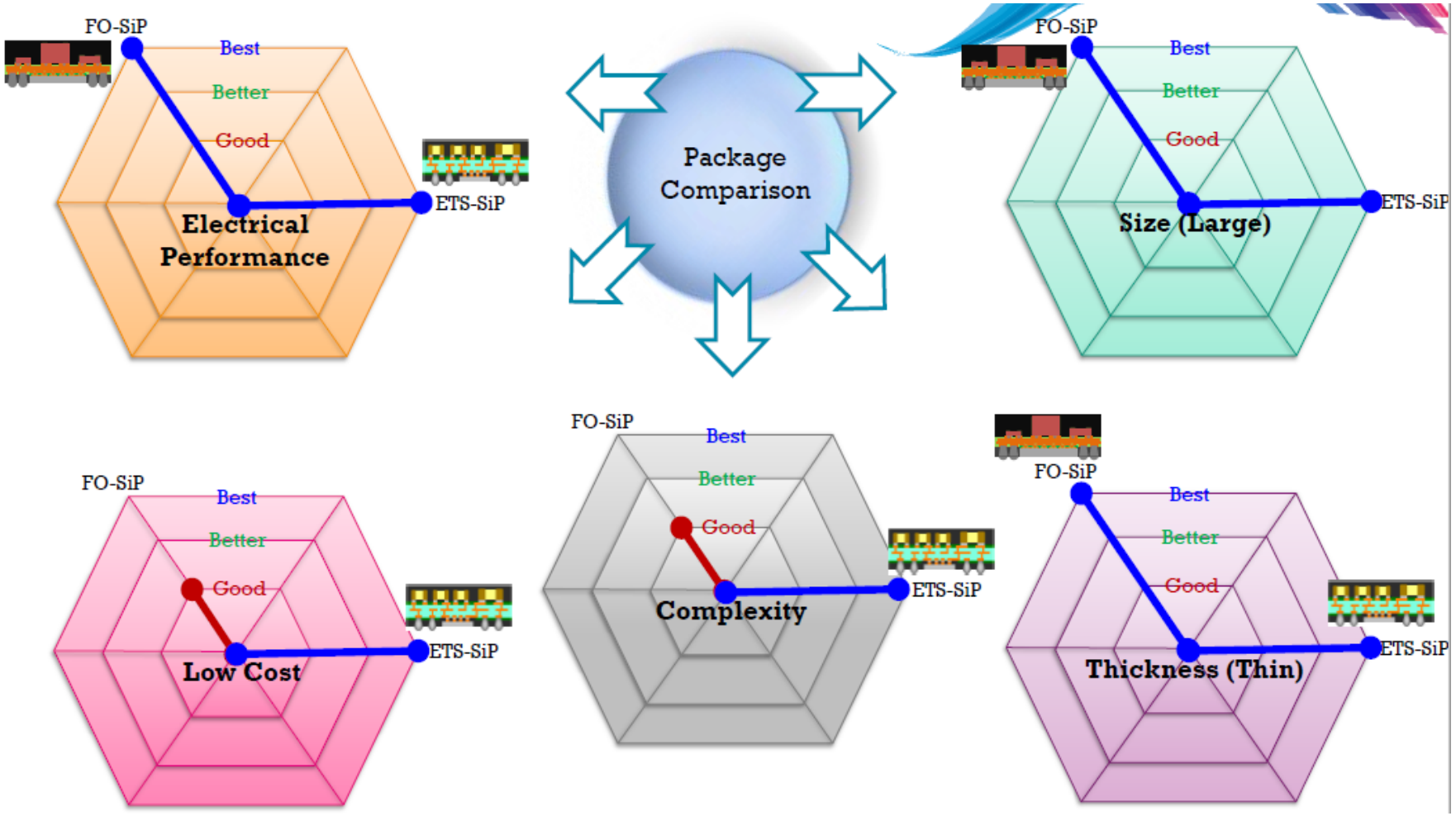
Total of approx 5 Weeks Process Cycle Time (Eng'g Stage)





FO – eWLP SIP Technology

SiP Type Package Technology assessment



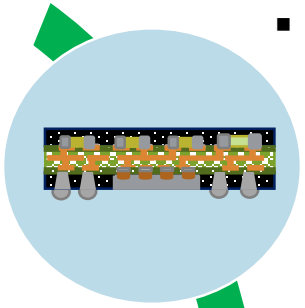
Short Notes :

- ❖ Package Technology Comparison by Dialog emphasized on 2.5 D addressing the needs to use and meets the needs of Wearable application requirements ;

- ✓ Package Foot Print
- ✓ Performance
- ✓ Complexity
- ✓ Cost

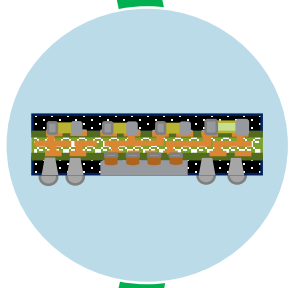
SIP Packaging Technology Differentiator (Cost & Industrialization)

+ Pros



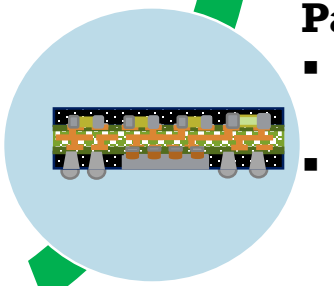
Complexity

- Using typical Prepreg Substrate material as Interconnect Carier/ interposer as Standard BGA Flow Concept



Industrialization

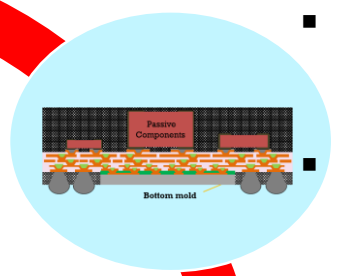
- Lower Cost of Equipment Investment
- Shorter Manufacturing Cycle time due to traditional substrate



Package Cost

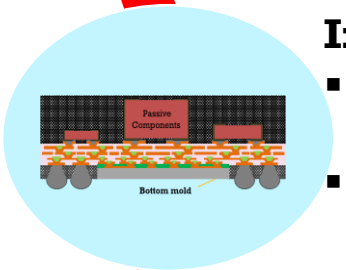
- No RDL Interconnect processes
- No use of additional BOM (ex. Liquid Compression Molding Material)

− Cons



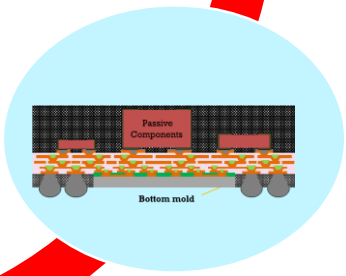
Complexity

- Compression Molding & 3 Layer RDL processes and structure .
- Warpage Behavior of Structure uncontrollable due to multi Layer RDL



Industrialization

- High Cost of Equipment Invest
- Longer Manufacturing Cycle time



Package Cost

- Multi Layer of RDL Bumping methodology
- Compression Molding using LCM Material

SIP Technology Achievement

Reliability Performance (PLR + BLR)

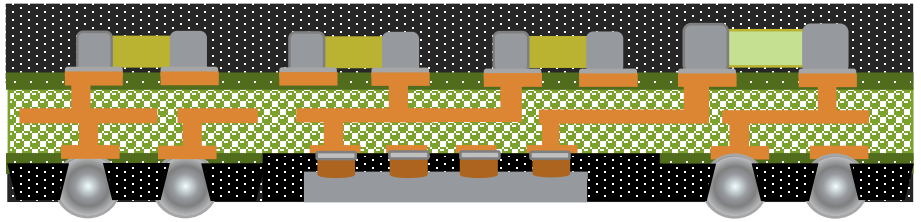
- ETS-SiP Structure passed all the PLR & BLR criteria

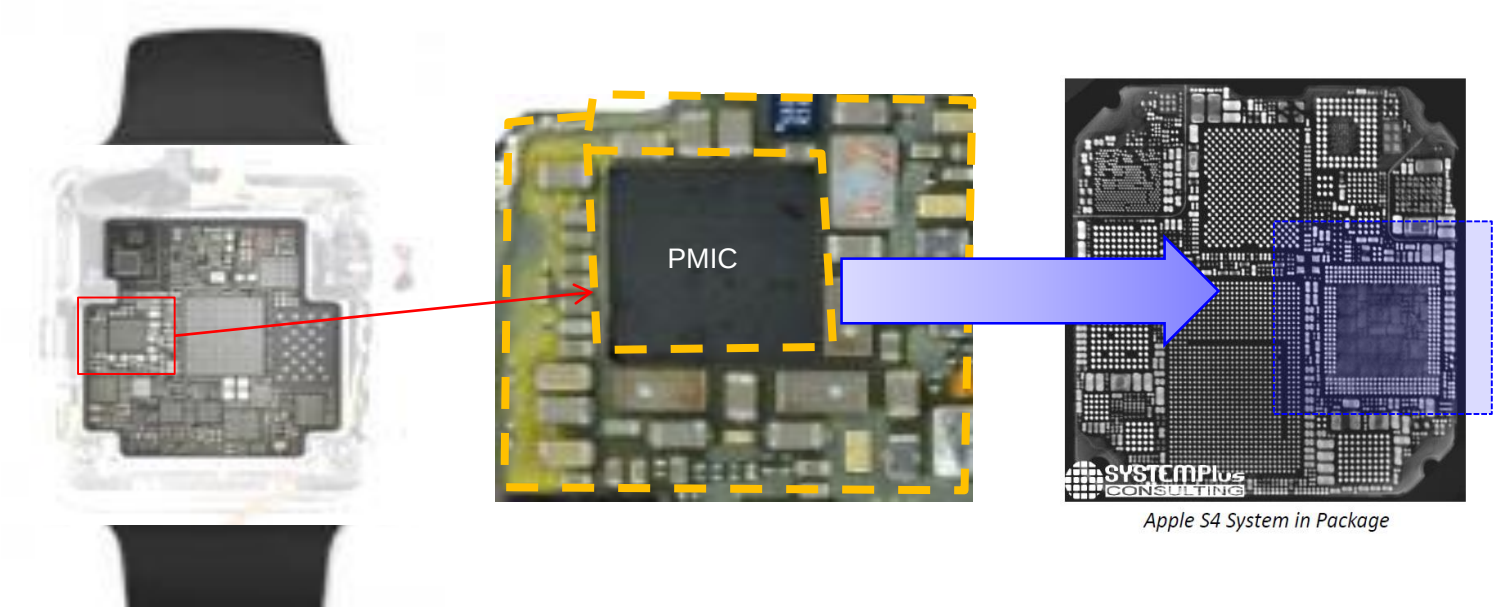
PLR Test Items	JEDEC Method + Customer Conditions	Result
Pre-conditioning MSL3	JESD22-A113	Passed
Temperature Cycling (TC)	1000Hrs, JESD22-A104	Passed
Unbiased HAST	JESD22-A118	Passed
High Temperature Storage Life (HTSL)	1000Hrs, JESD22-B115	Passed
Solder Ball Pull	JESD22-B115	Passed
Solderability	J-STD-002D	Passed
Reflow Sensitivity	Customer Conditions	Passed
BLR Test Items	**JEDEC Method + Customer Conditions**	
Drop	JESD22-B110	Passed
Random Vibration	JESD22-B103	Passed
Mechanical Shock	JESD22-B110	Passed
Altitude	ASTM D6653 (IEC60068-2-13)	Passed
Thermal Cycling	1000 cycles, JEDEC JESD22-A104A	Passed
Temperature and Humidity Dwell	1000 hours, JEDEC JESD22-A101C	Passed
Random Vibration	Customrt	Passed
Mechanical shock	JESD 22-B104 C	Passed
Monotonic Bending	IPC/JEDEC - 9702	Passed

Additional Technology Achievement

- ✓ Customer Awarded the technology of Choice vs other SIP Options.
- ✓ The invention is an innovative technical solution enabling unprecedented functionality in applications with challenging Form Factor ,Performance & Cost requirements, targeted initially for space constrained in wearable or smartwatch applications.

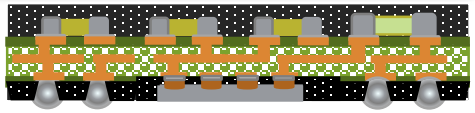
"Best Invention Award for 2017"with in DLG





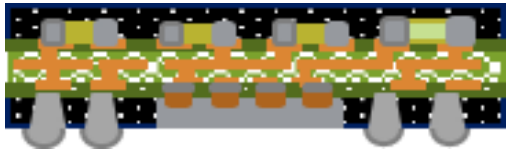
Apple S4 System in Package

DIALOG Double Side Molding
"ETS SiP Package



Double Side Mold SiP
- ✓ Ultra-thin 3D package
- ✓ Highly integration SiP
- ✓ High Performance
- ✓ Low Cost Approach

Summary & Takeaways for DLG ETS SIP -2.5D



- Advanced semiconductor packaging 2.5D SIP type, is seen as a way to increase the value of a semiconductor product functionality, maintaining/ increasing performance while lowering cost & package Size Footprint.
- More multi-die heterogeneous integration (SiP) and higher levels of package customization in the future. A variety of multi-die packaging (System-in-packages) is developing in both high and low end, for consumer, in specific applications like wearables . And Heterogeneous integration has created opportunities for both the substrate Type , WLP etc based SiP.
- So given the needs of COST , Area , Performance , Complexity and Cost for SIP Technology in Wearable and other applications with in needs of limited space , DLG SIP have the competitive edge vs other 2.5/3D technology in market today .
  - ✓ DLG Low Profile ETS SIP Technology ;
    - ✓ Offer less complexity in terms of assembly processes & manufacturing.
    - ✓ Technically flexible in integrating 3 to 4 layers of trace interconnect, dependent to application & electrical requirements.
    - ✓ Very Cost Effective Solutions & Technology vs eWLP SIP,TSV or other 3 to 4 layer interconnect structure.
    - ✓ Reliability robust & competitive vs 3or 4 RDL Layer Type vs eWLP Fan Out structure or other type .
    - ✓ DLG SIP technology showed Highly Integration of Passives (ex .82 ~110 pcs ..) vs other technology in the Market and this technology running in HVM since mid of 2018.

Thank You !

Any Questions ?

Slides Contributor Acknowledgement :

- **Dialog IC Packaging Team : *Ian Kent (Snr. Director IC Packaging)***
  - **Advance Package Development : *Jerry LI (Snr. Packaging Development Engineer)***
  - **Package Simulation : *Baltazar Canete (Manager Package Simulation)***

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