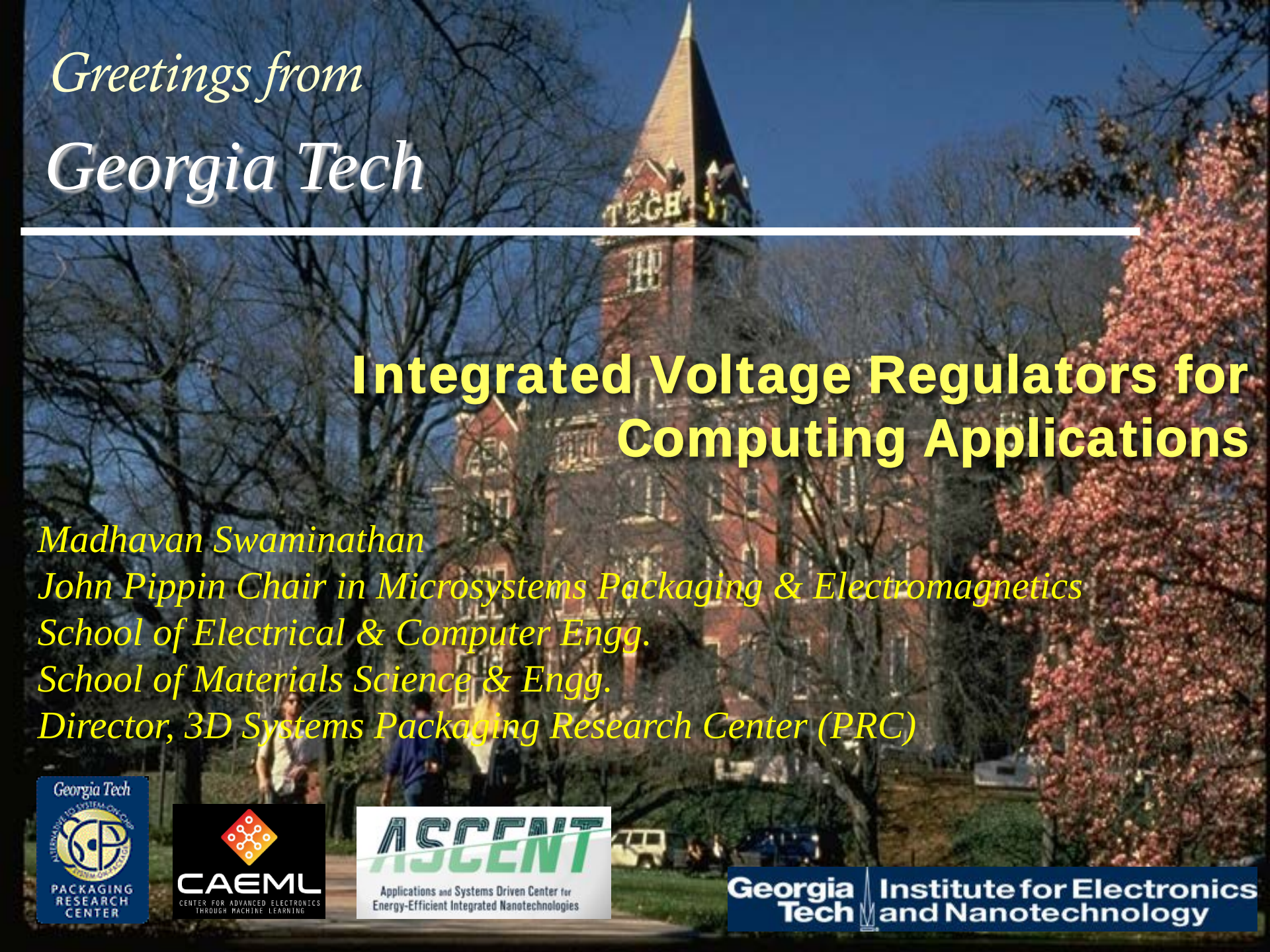
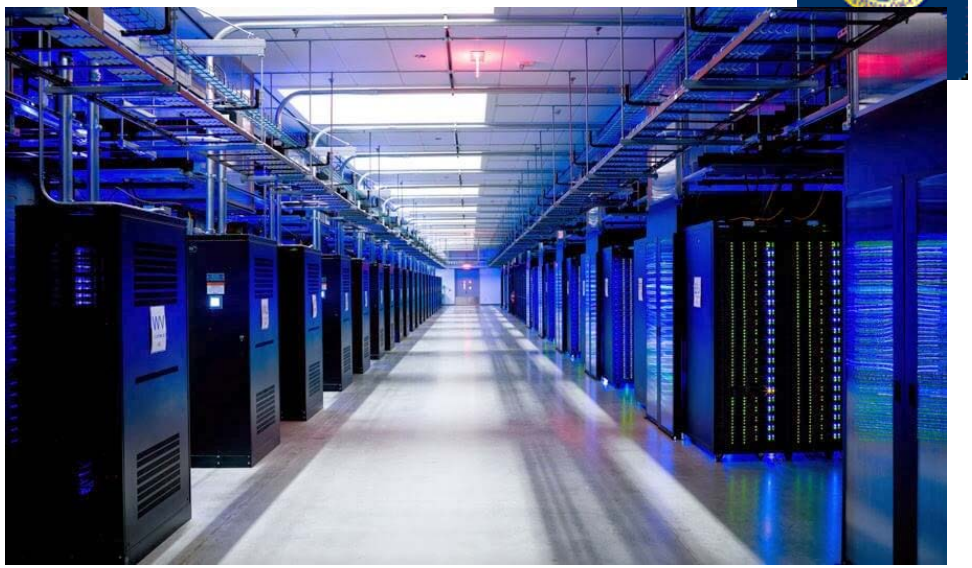
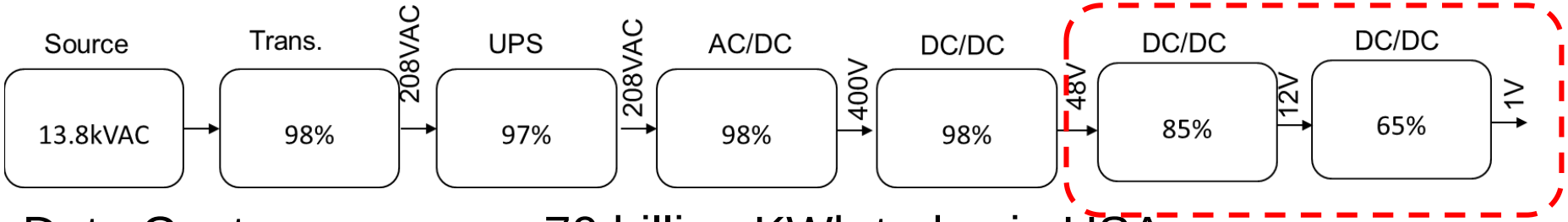

Greetings from
Georgia Tech
Integrated Voltage Regulators for Computing Applications
Madhavan Swaminathan
John Pippin Chair in Microsystems Packaging & Electromagnetics
School of Electrical & Computer Engg.
School of Materials Science & Engg.
Director, 3D Systems Packaging Research Center (PRC)
Georgia Tech
PACKAGING RESEARCH CENTER
CAEML
CENTER FOR ADVANCED ELECTRONICS THROUGH MACHINE LEARNING
ASCENT
Applications and Systems Driven Center for Energy-Efficient Integrated Nanotechnologies
Georgia Tech
Institute for Electronics and Nanotechnology

Outline

- ❑ Overview
- ❑ Low & High Voltage Converters
- ❑ Integrated Magnetics
- ❑ Summary

Data Centers & Energy

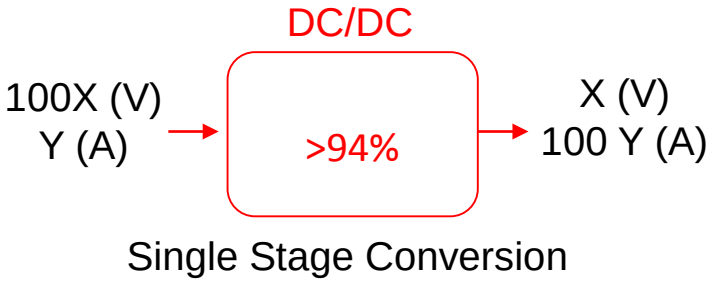


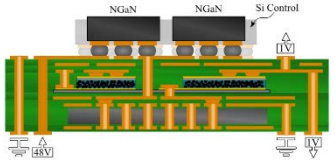


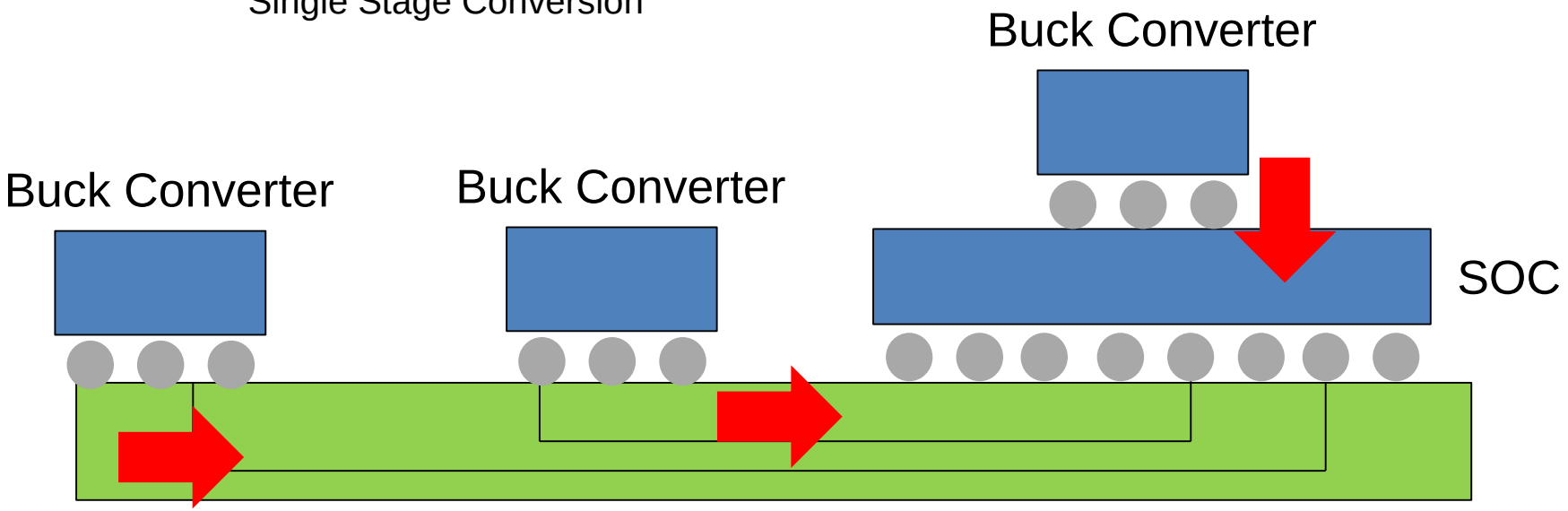
- Data Centers consume 70 billion KWh today in USA
- For every 2W drawn from the grid only 1W is used by the Data Center
- 20% improvement in efficiency can translate to 20% reduction in energy consumption

Source: Dept. of Energy, USA

Efficient Power Delivery in Microsystems

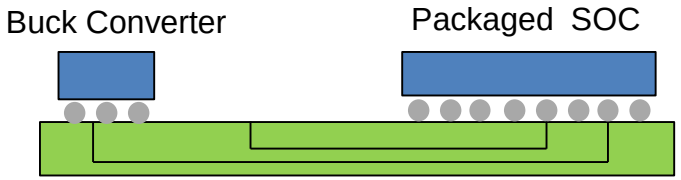




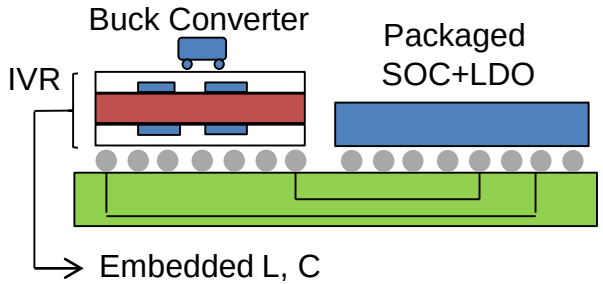


- Bring the converter (power source) in close proximity to SOC
  - Significantly reduce Cu losses due to shorter current paths
- Need: High Efficiency, Highly Integrated, Highly Miniaturized, High Conversion Ratio, Single Stage Converters
- Low energy circuits

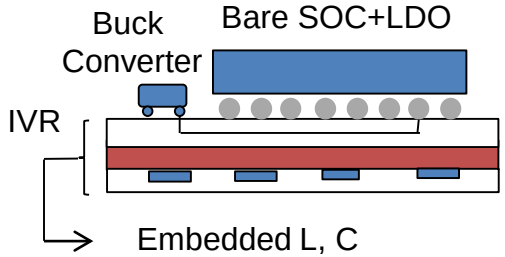
Voltage Regulation and Integration



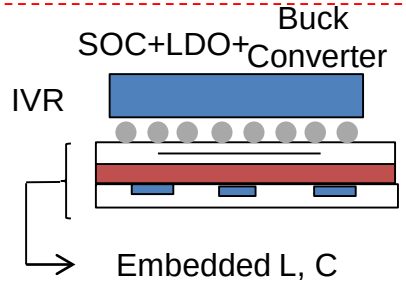
Business as usual
Advantages: Reasonable signal and power integrity
Integration: Low; Solution: Non-disruptive



New technology: SIP with embedded C & L, Buck Converter to SOC on board
Advantages: Slow/fast operation, Medium efficiency, Good Signal and Power Integrity,
Integration: Medium; Solution: Non-disruptive



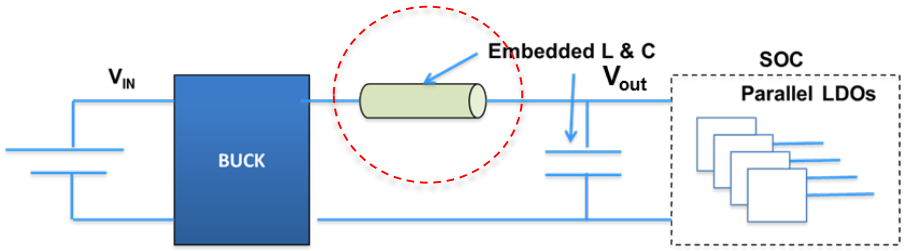
New technology: SIP with embedded C & L, Buck Converter, SOC in package
Advantages: High Performance, High Efficiency, Modular, Excellent Signal and Power Integrity, Cost effective, Thermal Mgmt.
Integration: Very High; Solution: Disruptive

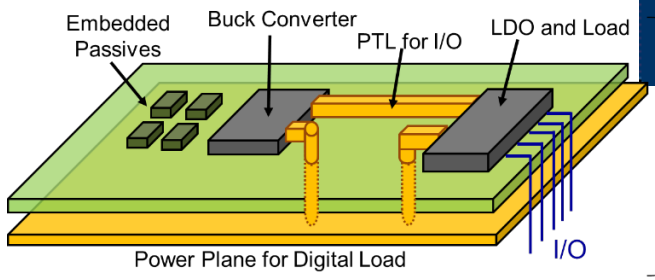


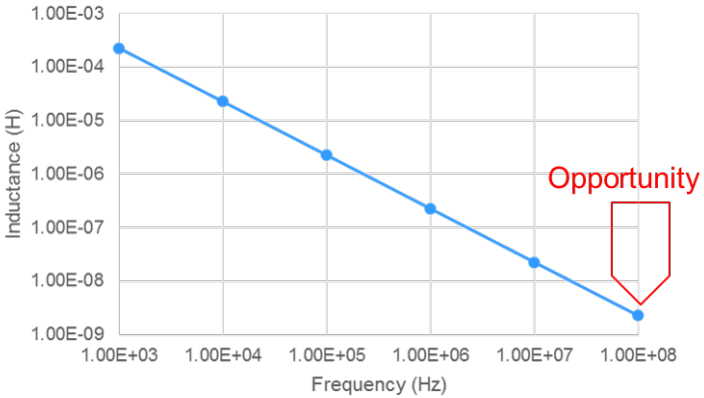
Intel FIVR

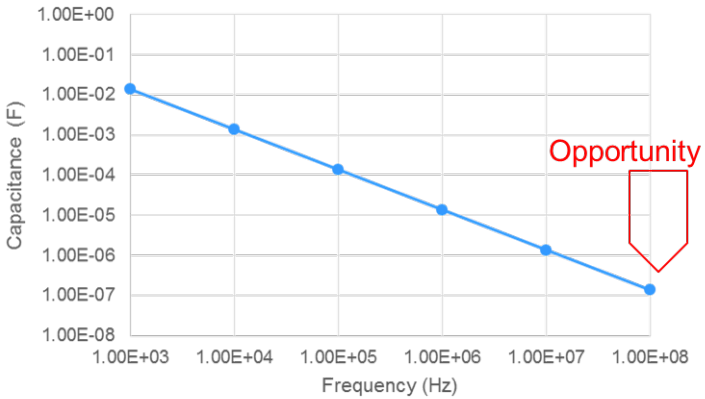
New technology: SOC with on-chip integrated IVR, embedded C & L in package
Advantages: Very High Performance
Challenges: Non-modular, Non-scalable, Thermal Mgmt.
Integration: Ultra-High; Solution: Disruptive

Integrated Voltage Regulators



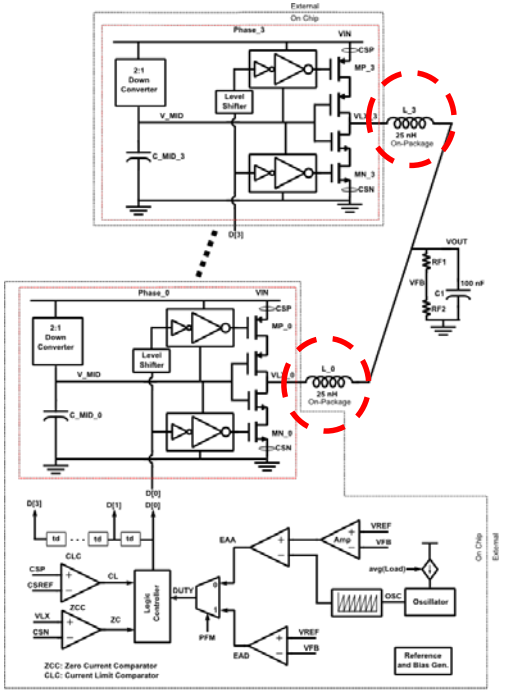


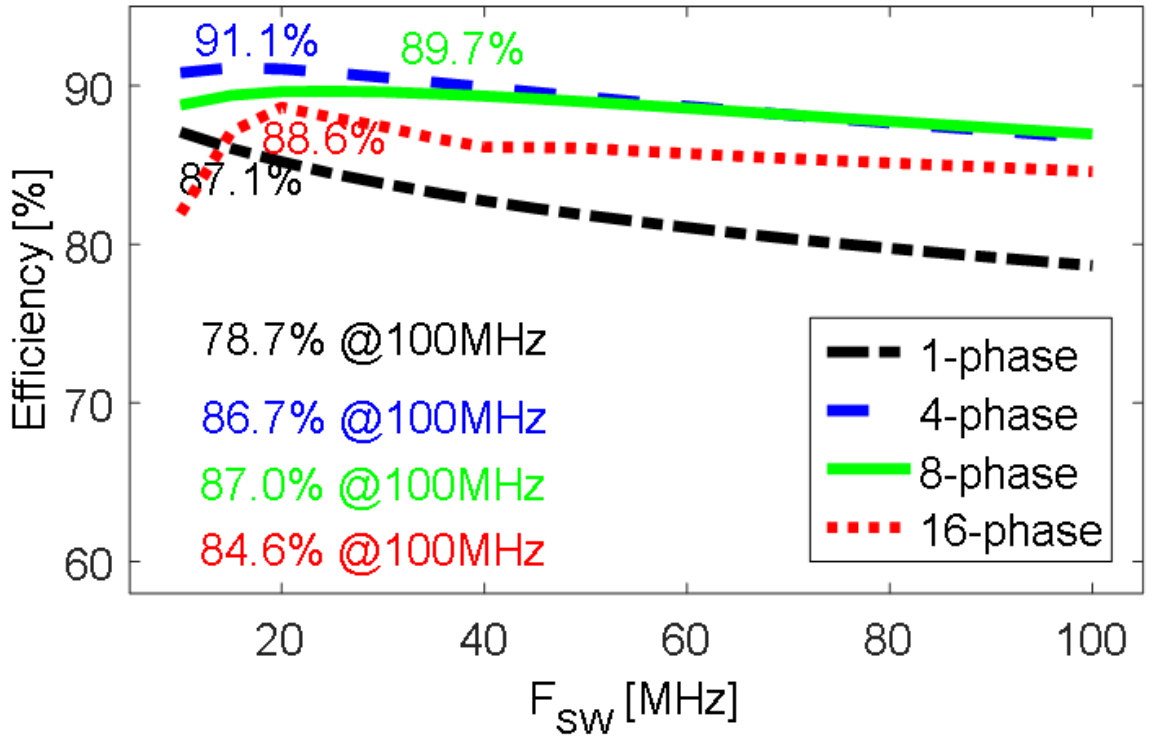




- L and C values reduced by increasing switching frequency
- Provides an opportunity for embedding and miniaturization in package (Reasonable values for L and C)
- However, losses increase as switching speed increases
  - Transistor losses
  - Inductor losses (DC, eddy current, skin, hysteresis and proximity effect)
- But tradeoff possible between speed, component size and technology

Design Space Exploration through Chip-Package Co-Design: 1.7V/1V



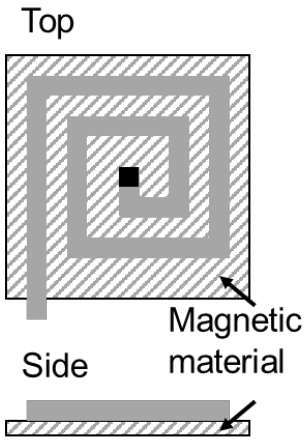


- ❑ Tradeoff Analysis Critical
- ❑ Number of phases? (4 phases w/100nH total inductance)
- ❑ Maximum power efficiency 91% @ 20MHz
- ❑ Power efficiency improves by ~2% with transistor scaling

Inductor Design Options

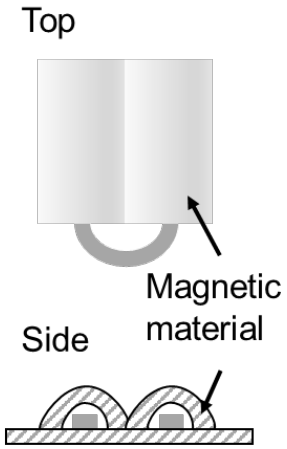
- Several inductor designs with magnetic material possible (published in literature)

Spiral inductor on or between magnetic material



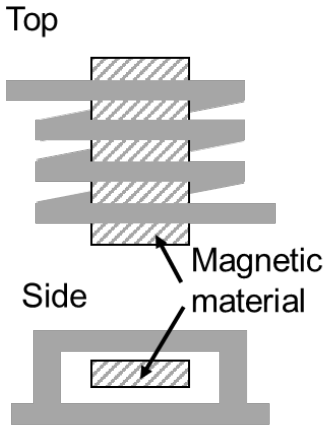
- **Advantage:** simple structure / simple fabrication
- **Disadvantage:** Inductances larger than a few nH require high permeability or large inductor area

Copper winding enclosed by a magnetic material



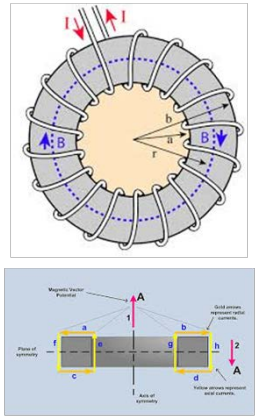
- **Advantage:** coupling between different inductor phases possible for DC field cancellation
- **Disadvantage:** inductor uses single winding – high permeability required

"Solenoidal" inductor enclosing a magnetic core



- **Advantage:** higher number of windings – higher inductance for a given permeability
- **Disadvantage:** "3D" structure – challenging fabrication

"Toroidal" inductor " Closed loop core

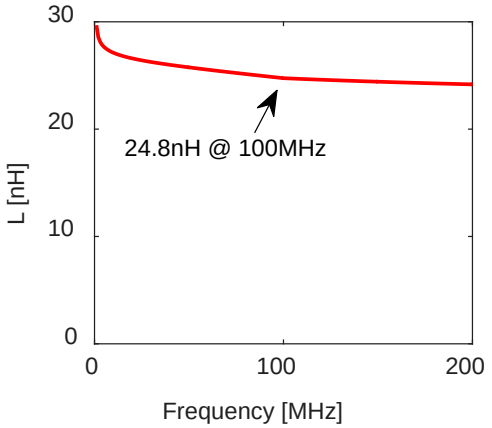


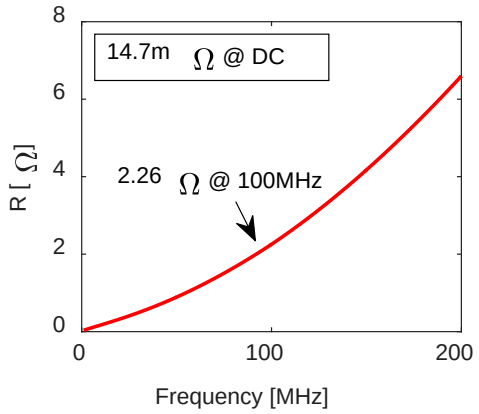
- **Advantage:** Higher inductance, Q & inductance density
- **Disadvantage:** "3D" structure – challenging fabrication

Inductor Design – An Example

- Final design: 4-phase design with 25nH inductance per phase
- Inductor properties as specified below:

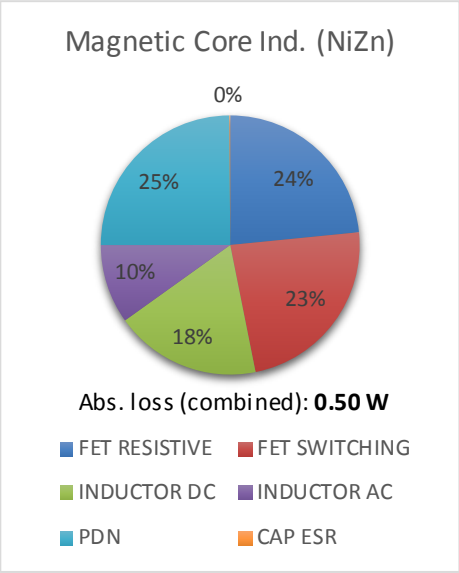
	Optimized inductor design
L [nH]	24.8
R_{DC} [mΩ]	**14.7**
R_{AC} [Ω]	2.26
C [pF]	1.9
Area [mm²]	11.6
L / $L_{Aircore}$	3.1
Peak eff. 5V:1V	79.4%
Peak eff. 3V:1V	88.5%
Peak eff. 1.7V:1.05V	91.1%

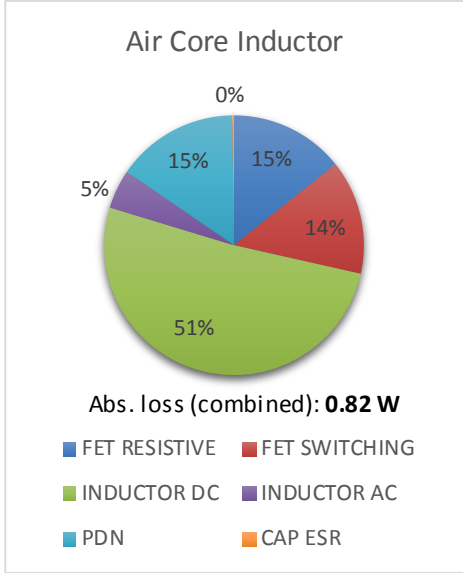




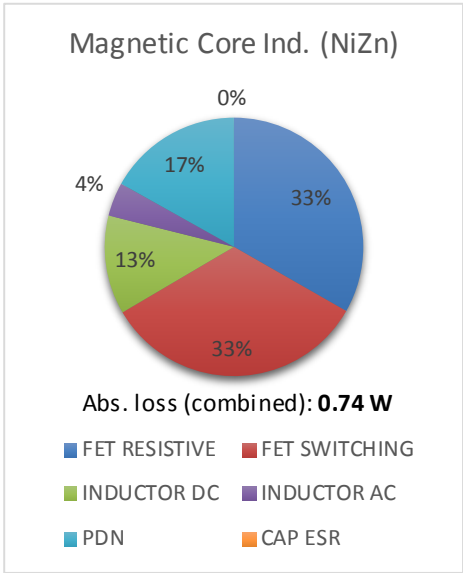
Power Losses

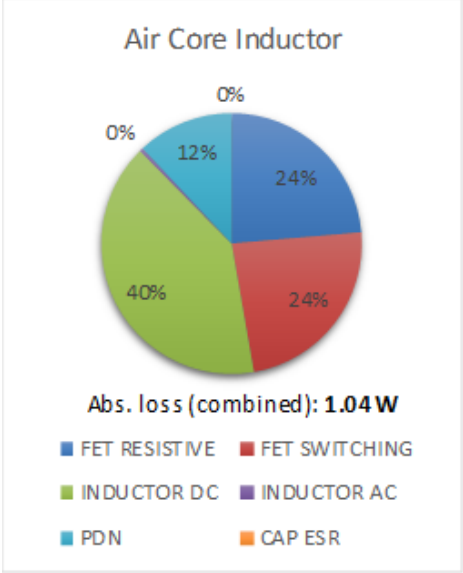
22 MHz





100 MHz





- ❑ 1.7/1V 5A Load Current (50% Load)
- ❑ 25nH inductance/phase
- ❑ 22MHz
  - Ferrite Core: 47% FET; 28% Inductor (DC: 18% AC: 10%); 25% PDN
  - Air Core: 29% FET; 56% Inductor (DC: 51% AC: 5%); 15% PDN

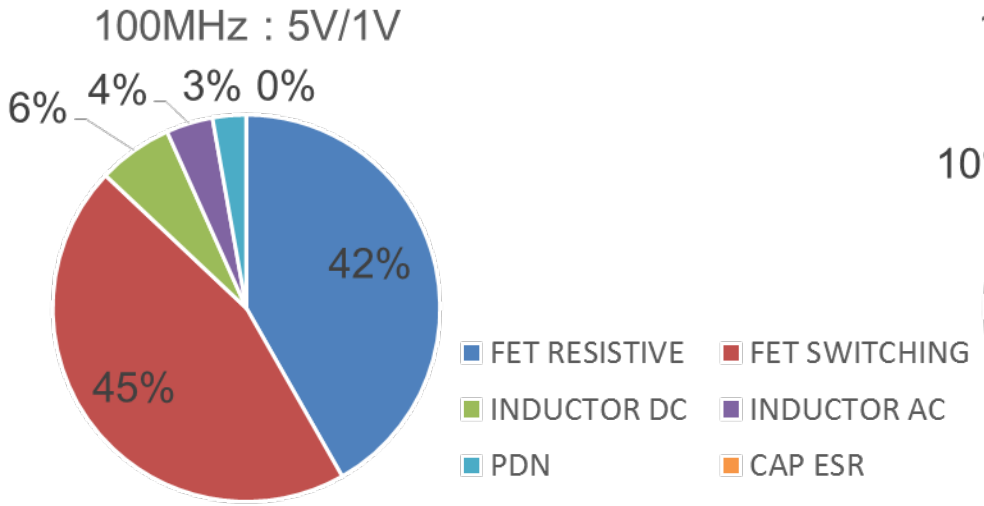
Magnetic core increases inductance density and lowers DC resistance

S. Mueller, Member, M.L. F. Bellaredj, A. K. Davis, P. A. Kohl, and M. Swaminathan, Design Exploration of Package-Embedded Inductors for High Efficiency Integrated Voltage Regulators", IEEE Trans. CPMT, Accepted, 2018.

Impact of Heating on DC Loss

- Impact of inductor heating on overall efficiency [6]:

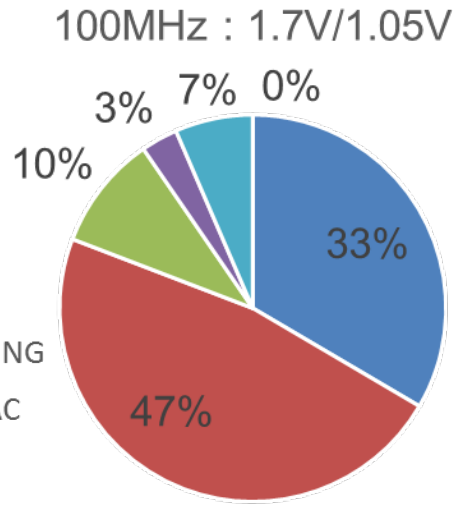
5V:1V conversion



→ 9% of overall loss related to resistance ("inductor DC" and "PDN")

→ **Inductor heating changes overall efficiency at 100 MHz from 70.5% to 70.2% (small)**

1.7V:1V conversion

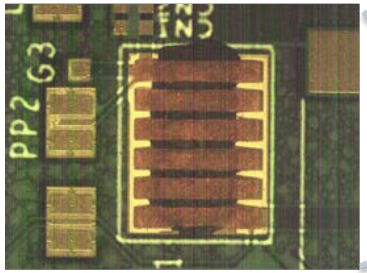


→ 17% of overall loss related to resistance ("inductor DC" and "PDN")

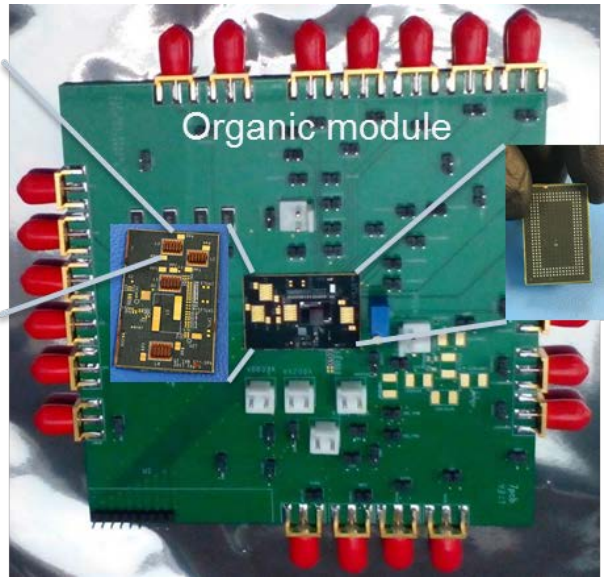
→ **Inductor heating changes overall efficiency at 100 MHz from 86.7% to 86.4% (small)**

[6] Modeling and Design of System-in-Package Integrated Voltage Regulator with Thermal Effects, S. Mueller, A. K. Davis, M. L. F. Bellaredj, A. Singh, K. Z. Ahmed, S. Mukhopadhyay, P. A. Kohl, M. Swaminathan, Y. Wang, J. Wong, S. Bharathi, Y. Mano, A. Beece, B. Fasano, H. Fathi Moghadam and D. Draper, To be presented at EPEPS, CA, Oct. 23-26, 2016

Recent Work



Screen printed inductor on Organic Substrate



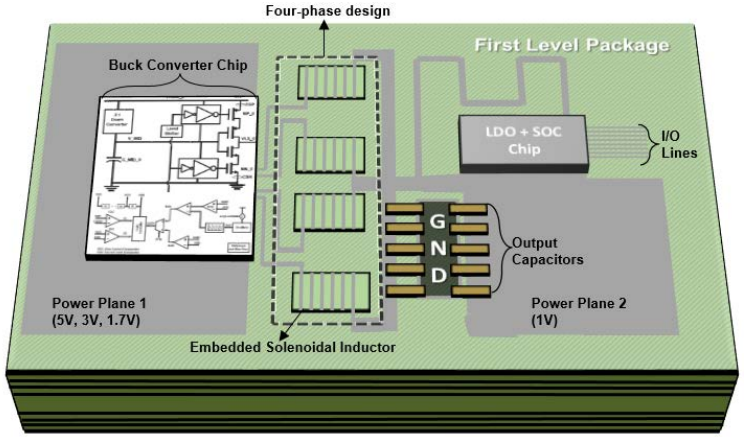
	[1]	[2]	[3]	[4]
Phases	4	Up to 16	8	8
Process node	130nm	22nm	45nm	45nm
Integration level	Package	Package	Silicon interposer	Die
Inductor type	Magnetic core	Air core	Magnetic core	Magnetic core
Inductance @100MHz	22.8nH	2.5nH	8nH	1.5nH
Peak eff. (1.7V:1V)	91.7%	90% (1.7:1.05)	82% (1.6:0.83)	84% (1.5:1.15)
Peak eff. (3V:1V)	89.6%	Not specified	Not specified	Not specified
Peak eff. (5V:1V)	81.3%	Not specified	Not specified	Not specified

[1] S. Mueller et al, Design Exploration of Package-Embedded Inductors for High Efficiency Integrated Voltage Regulators", IEEE Trans. CPMT, 2018.
[2] E. A. Burton et al., "FIVR - Fully integrated voltage regulators on 4th generation Intel(R) CoreTM SoCs," in 2014 Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2014.
[3] K. Tien et al., "An 82%-efficient multiphase voltage-regulator 3D interposer with on-chip magnetic inductors," in 2015 Symposium on VLSI Technology (VLSI Technology), 2015.
[4] H. K. Krishnamurthy et al., "20.1 A digitally controlled fully integrated voltage regulator with on-die solenoid inductor with planar magnetic core in 14nm tri-gate CMOS," in 2017 IEEE International Solid-State Circuits Conference (ISSCC), 2017.

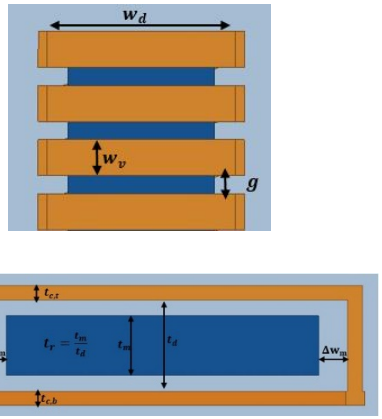
Courtesy: PDES, GT & JUMP-SRC (ASCENT)

Machine Learning for IVR Optimization

Overall SoP IVR Architecture



Embedded Solenoidal Inductor



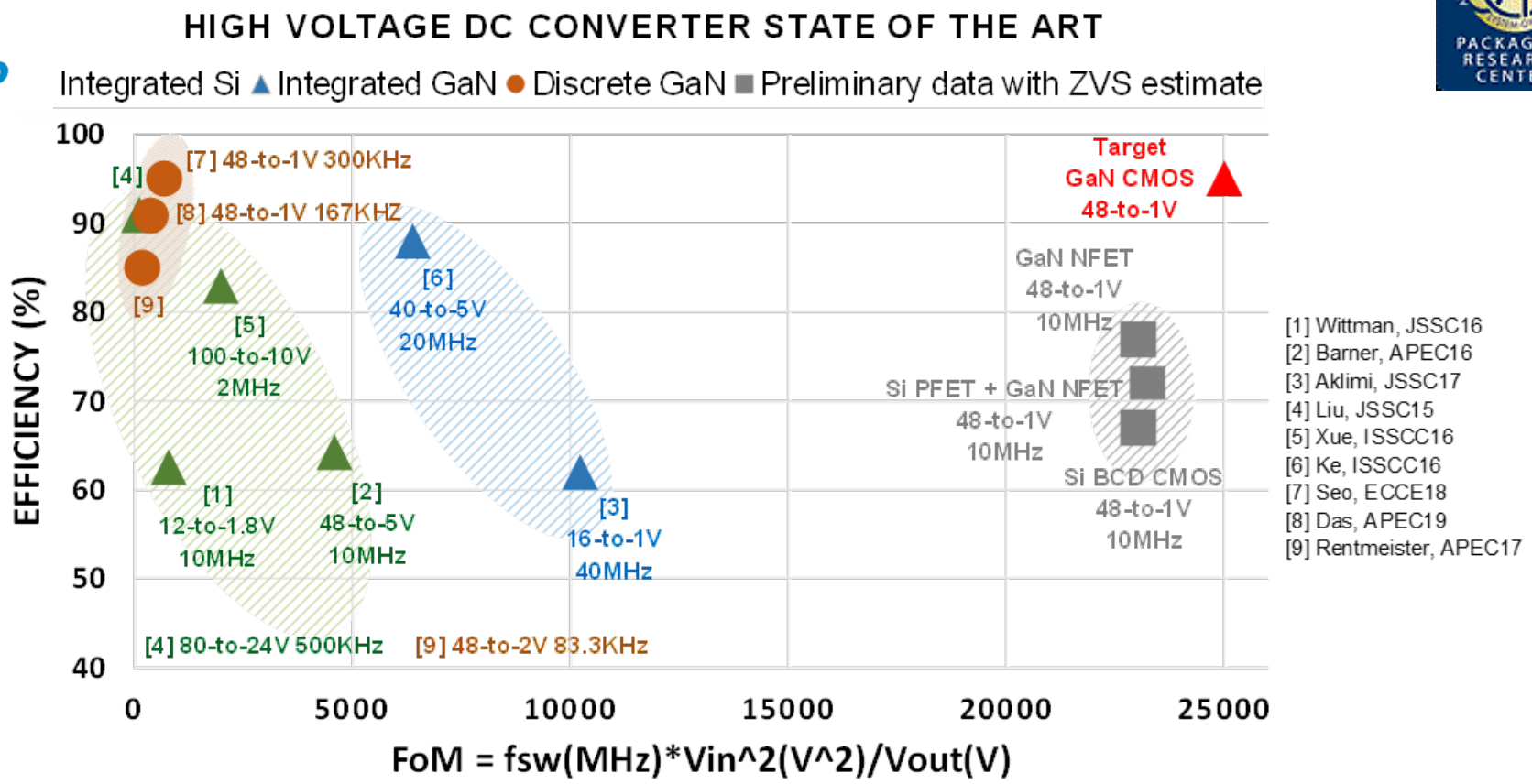
Control Parameters

Parameter		Unit	Min	Max
Gap between windings	g	mil	2	20
Number of windings	N		3	13
Size of via	s_v	μm	50	103
Copper Trace Width	w_c	mil	2	20
Copper Thickness Bottom	$t_{c,b}$	μm	35	170
Copper Thickness Top	$t_{c,t}$	μm	35	170
Dielectric Thickness	t_d	μm	50	650
Dielectric Width	w_d	μm	50	350
Magnetic Core Thickness Ratio	t_m		0.1	1
Magnetic Core Width offset	Δw_m	mil	0	100

	Hand Tuned	Non-Linear	GP-UCB	IMGPO	TSBO
Inductor Area	11.3 mm^2 (+56.1%)	25.19 mm2 (+79.6%)	5.18 mm2 (%0.4)	6.64 mm2 (%28.1)	**5.16 mm^2**
Peak Efficiency	79.4%	78.6%	84.9%	84.4%	**85.1%**
CPU Time	N/A	>185 min (+72.9%)	117.33 min (+57.4 %)	115.6 min (+56.7 %)	**50.1 min**

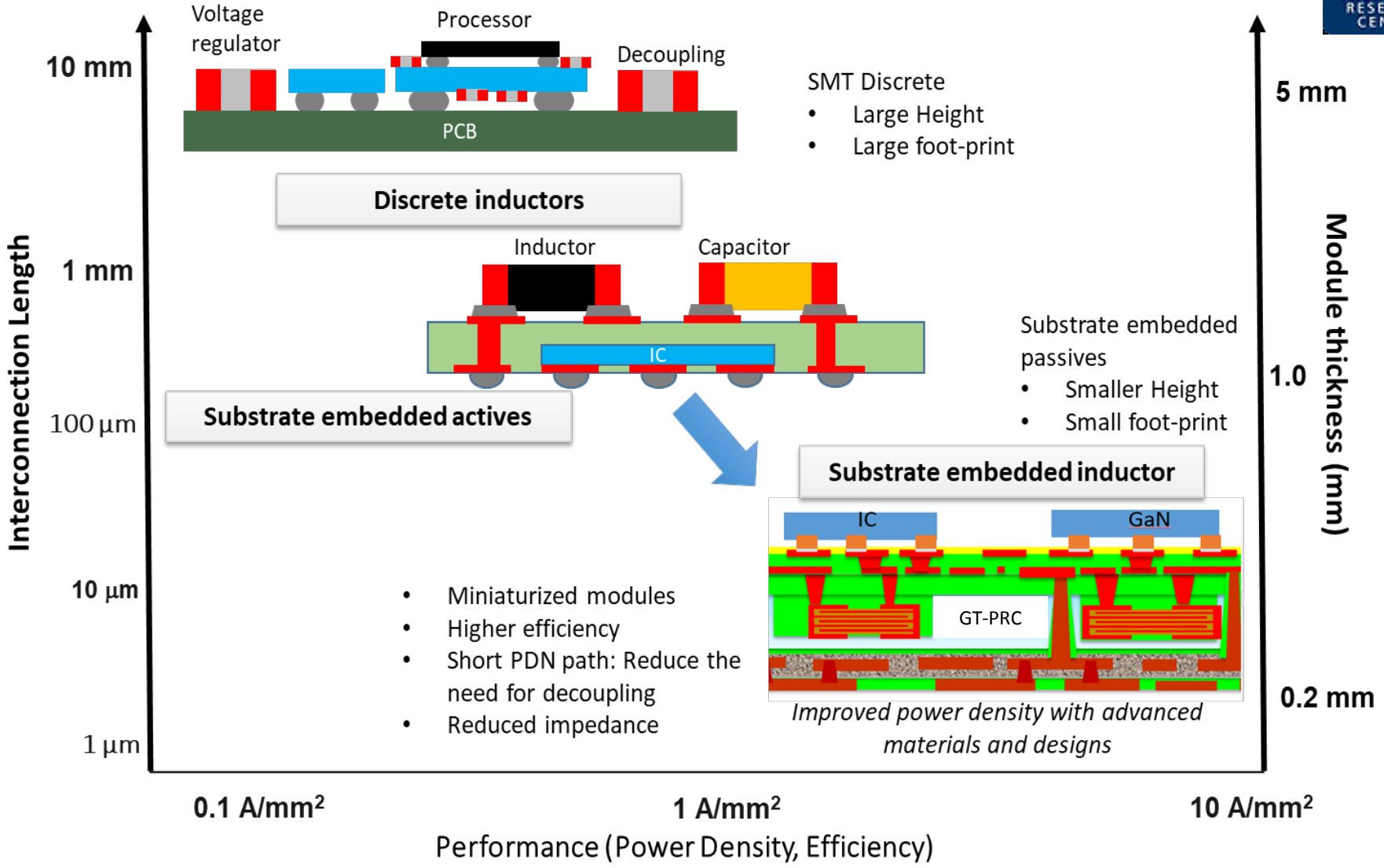
Hand Tuned: S. Mueller *et al.*, "Design of High Efficiency Integrated Voltage Regulators with Embedded Magnetic Core Inductors," ECTC'16**.**
Optimized: *H. M. Torun et al.* "A Machine Learning based Global Optimization Algorithm and its Application to Integrated Systems". TVLSI '18

Future Power Delivery Solutions



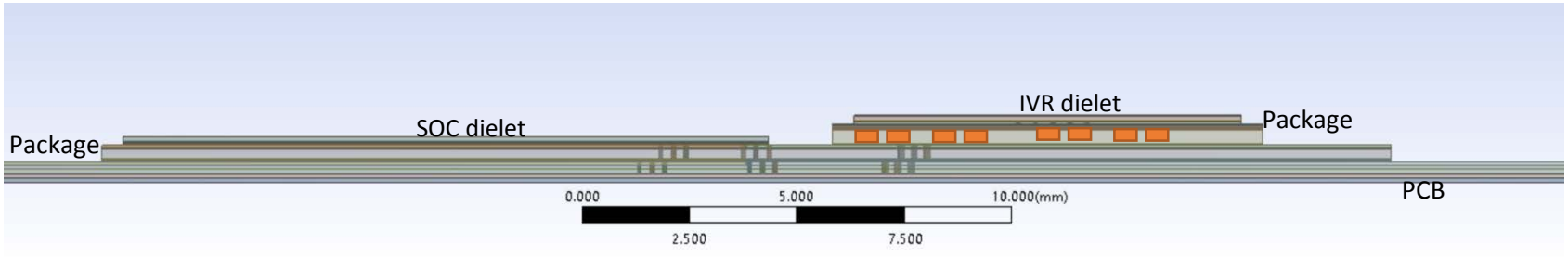
- GaN Converter: Up to 10x higher switching frequency at comparable efficiency
- Breakthrough in p-channel GaN FinFET with record on-current – a key enabler for GaN-CMOS
- Opportunity: GaN Buck Converters w/ Magnetics for 48V/1V Conversion

Integrated Voltage Regulators (revisited)

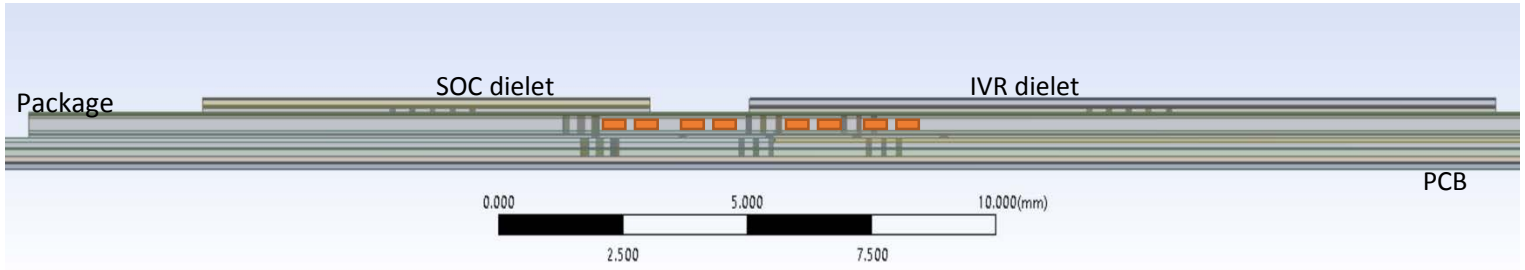


Thermal Management

- Two heterogeneous architectures being explored
- Inductors embedded either in a package or in the substrate of the multi-chip package



(a) Package on package (PoP)



(b) Multi-chip module (MCM)

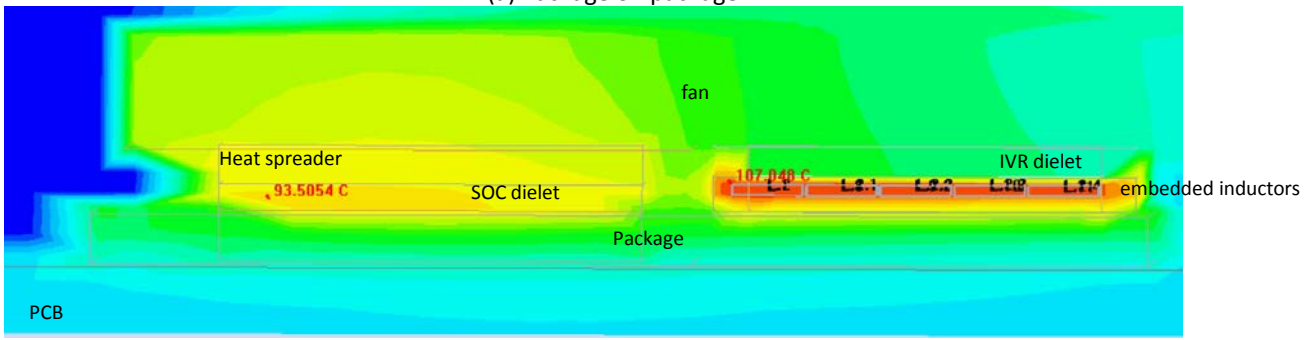
	SOC (12mmx12mmx.0.75mm)	**IVR** (10mmx10mmx0.75mm)	**Embedded inductor** (2mmx1mmx0.35mm)
TDP (W)	100	10	0.15

Thermal Coupling and Joule Heating major issues

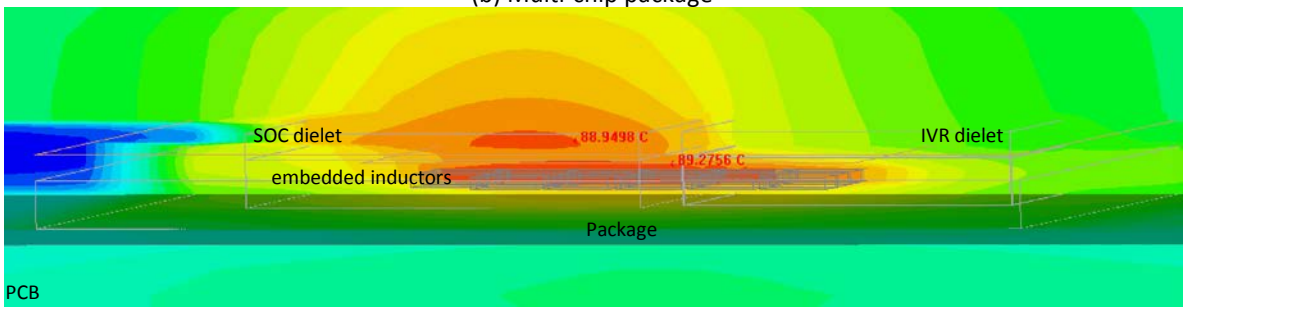
- Embedded inductors reach high temperatures in the range of 89-107C
- Joule heating <u>neglected</u> here. Inductor temperature expected to increase

Configuration	Fan flow (CFM)	$T_{ambient}$ (°C)	$T_{inductor}$ (°C)	$T_{cpu\_junction}$ (°C)
Package on package	30	42	107	93.5
Multi-chip package	30	42	89.2	88.9

(a) Package on package



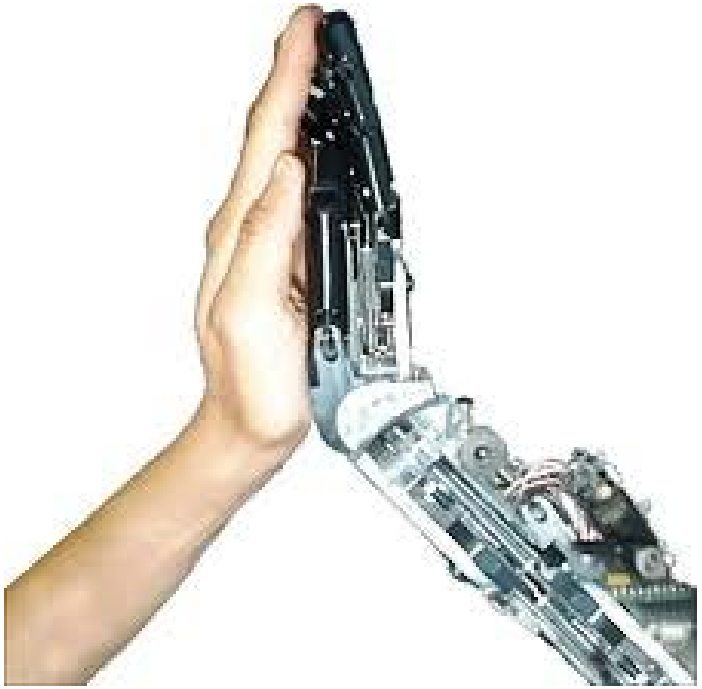
(b) Multi-chip package



Summary

- Integrated Voltage Regulators (IVR) can lead to significant energy savings
- Requires integrated integrated magnetics and dielectrics
- Thermal management critical
- Heterogeneous Integration is the way forward (for various reasons)!

Thank you



NAMASTÉ

www.prc.gatech.edu
www.c3ps.gatech.edu