High-Performance Controllers for Emerging Converter Topologies and Low-Power High-Frequency SMPS

Aleksandar Prodić

E-mail: prodic@ece.utoronto.ca

Laboratory for Power Management and Integrated SMPS

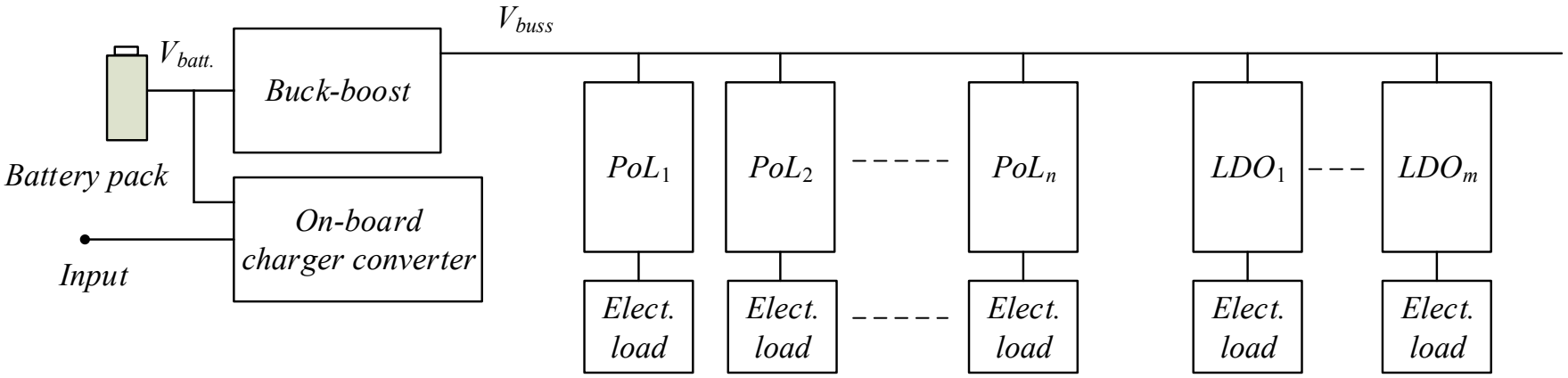
University of Toronto, E. Rogers ECE Department

http://www.ele.utoronto.ca/power_management/publications.html

Applications of Primary Interest, Challenges and Goals

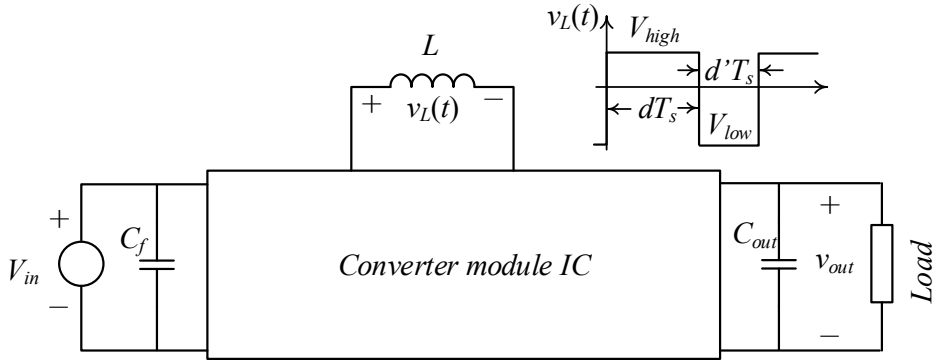
Primary Applications: Power Management Systems of Modern Electronic Devices (Space Constrained)

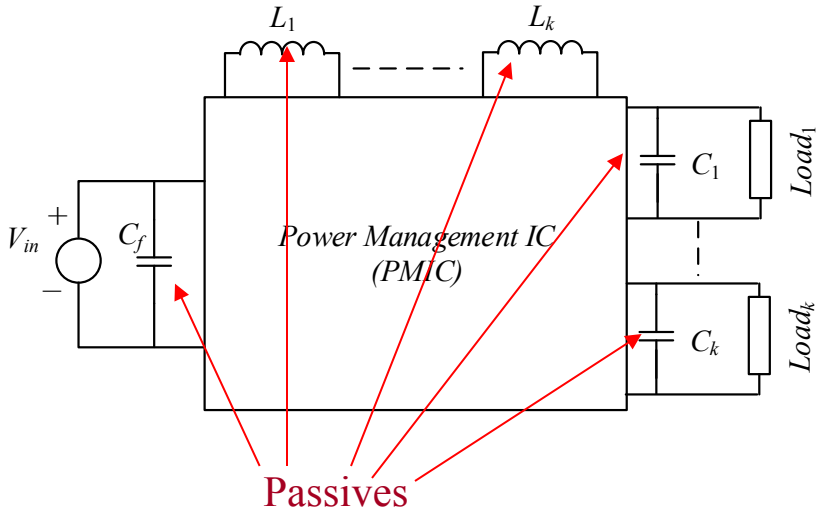
- Often consist of more than 30 switch mode power supplies (SMPS) and low-drop out regulators (LDOs)
- Power processing is usually done in two stages
- Converters process power from a fraction of watt to few hundreds of watts



Power management system of a mobile device

Low Power SMPS: Ongoing Situation & Requirements





- Passives often occupy up to 80 % of total PCB area and are a large contributor to the overall weight and cost, **often area by Cs and height/weight by Ls**
- Bottle neck in extension of functionality and operating time
- Increasing power and conversion ratio and, at the same time, smaller height < 1 mm of power SMPS are required
- Highly cost sensitive applications

SMPS in Low Power Applications – General Challenges

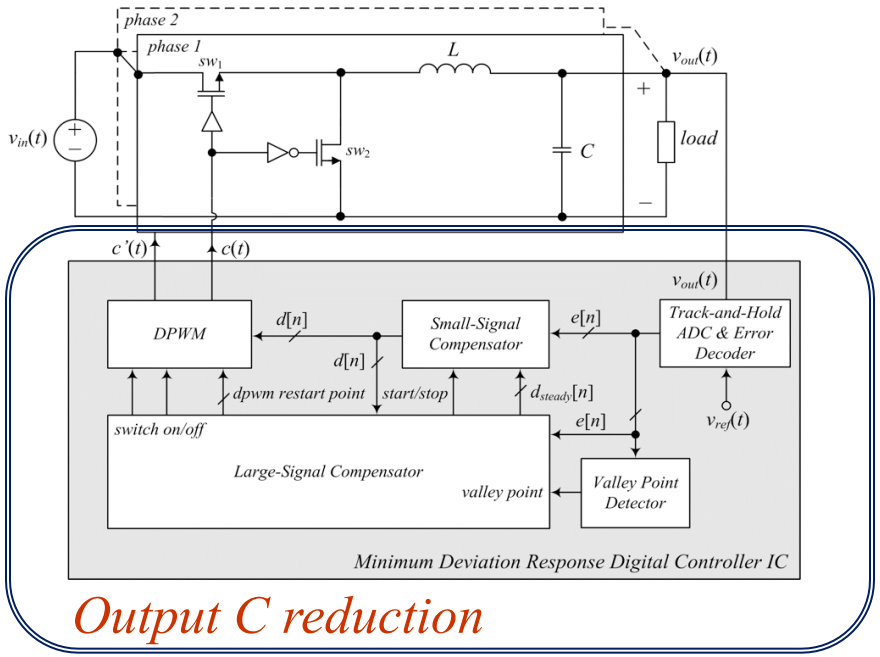
- Existing solutions cannot keep with requirements of emerging applications, due to increasing power consumption (driven by increasing functionality)
- Design requirements practically ask for **larger output power and smaller passive components while improving efficiency.** Due to thermal (safety and cooling constrains).
- Related, voltage requirements are changing, higher step down required
- Custom topological/control solutions for a given application might be needed to maximize efficiency and minimize the volume.

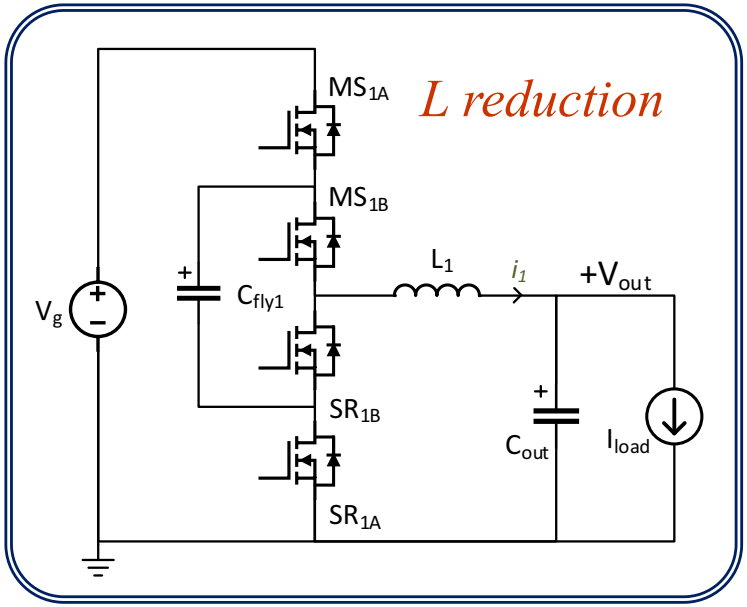
- Solutions based on novel devices and technologies, i.e. operation at higher switching frequencies
- ***Solutions based on novel controller design and power stage architectures => Focus of this talk***

Main Requirement for new solutions => Need to be more efficient and smaller at the same time

Fundamental Volume Reduction Principles for Passive Components

Control and Topological Solutions for C and L Reductions

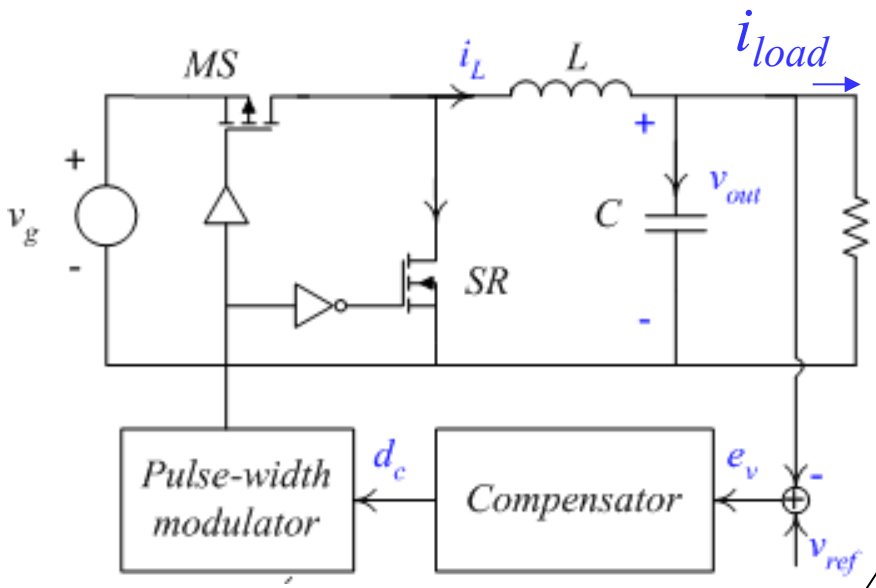


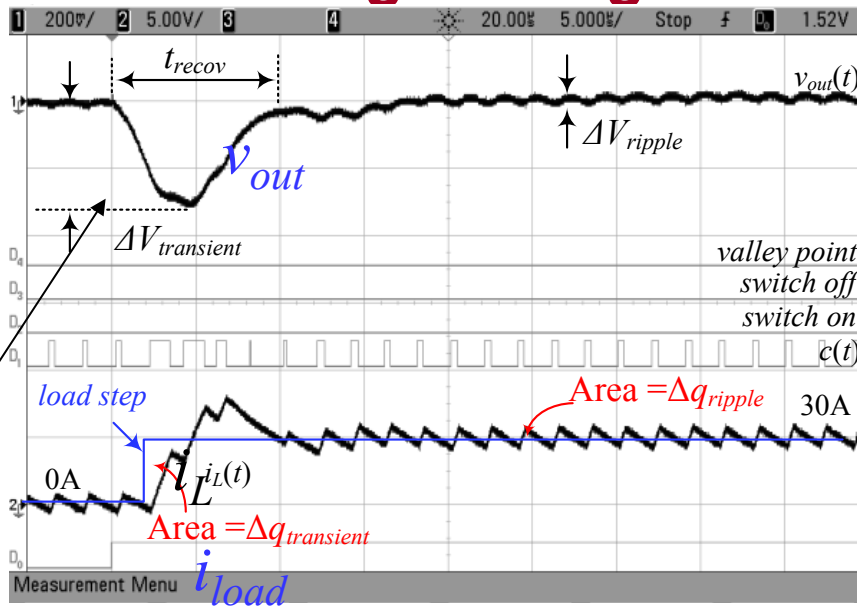


- *C reduction through improvement of dynamics performances of controllers (min. deviation control)*
- *L (and C) reduction through minimization topological solutions– reduced voltage swing converter topologies*

Single Mode Minimum Deviation Controller

Sizing of the Output Capacitor and Charge Swing





Design parameter: voltage deviation during transients => ultimate goal to reduce this deviation

Key converter waveforms during steady state and a transient

Our ultimate goal is to minimize $\Delta V_{transient}$ – so lets see how, in traditional design, we go there…

Frequency Domain (s-Domain) Based Controller Design (Conventional Control Theory Based)

Wide-bandwidth loop

Frequency → time

Fast Controller Action

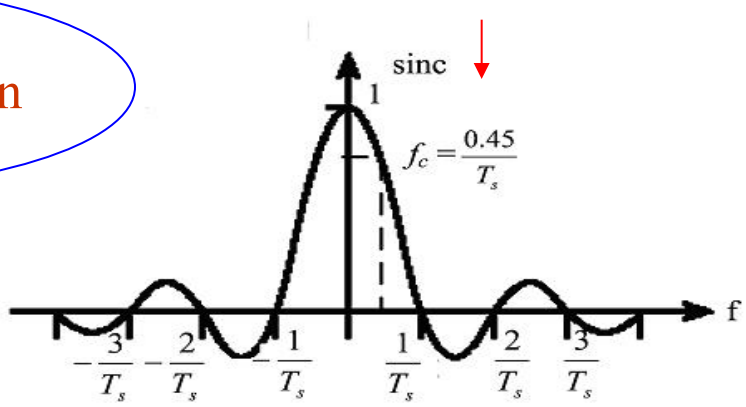
Time → deviation = size

Reduced C Volume with a Small Output Deviation

Ultimate Goal

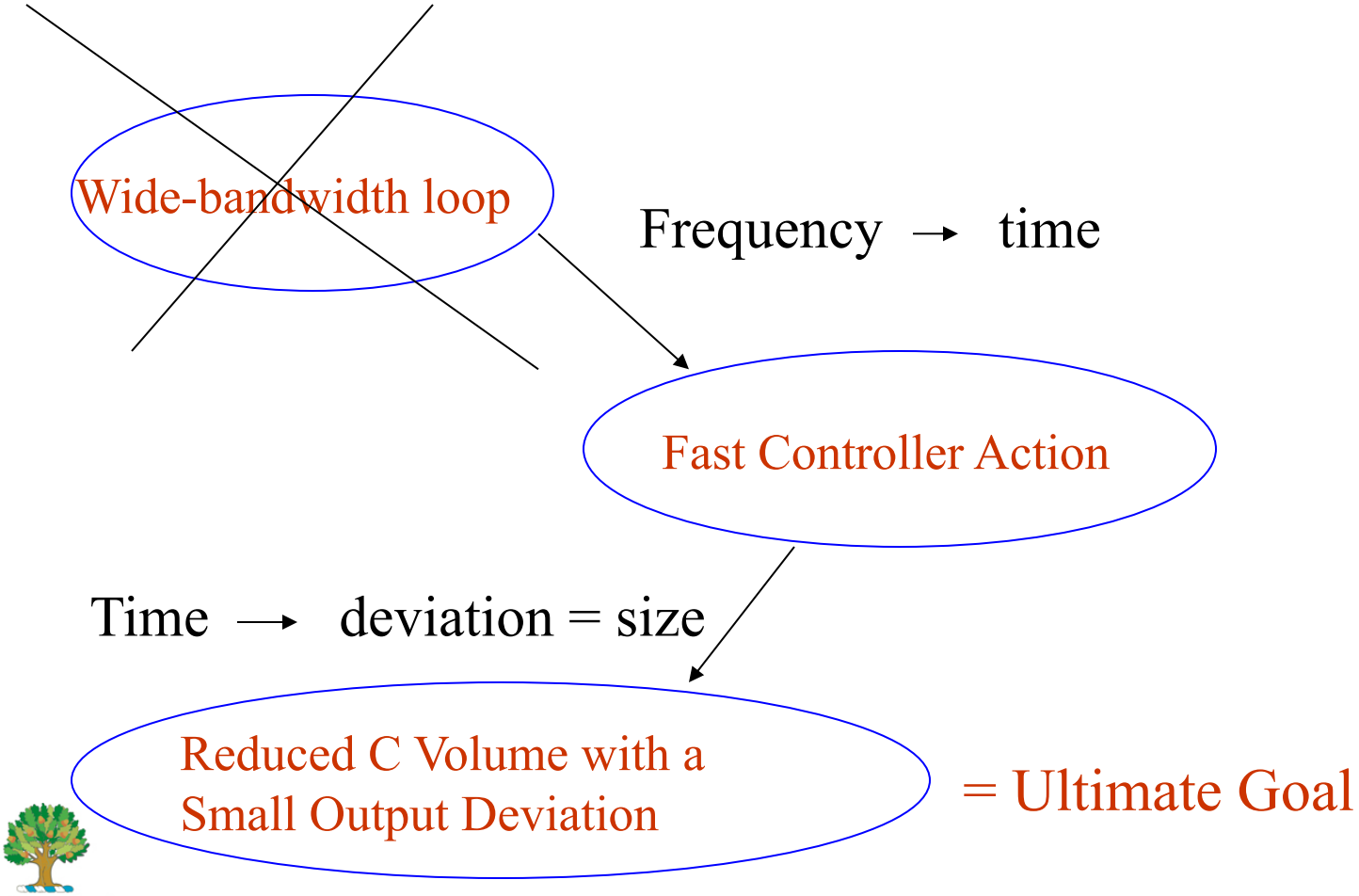
$$\langle i_L(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{T_s} i_L(t)dt$$

$$\langle v(t)\rangle_{Ts} = \frac{1}{T_s}\int_0^{T_s} v(t)dt$$

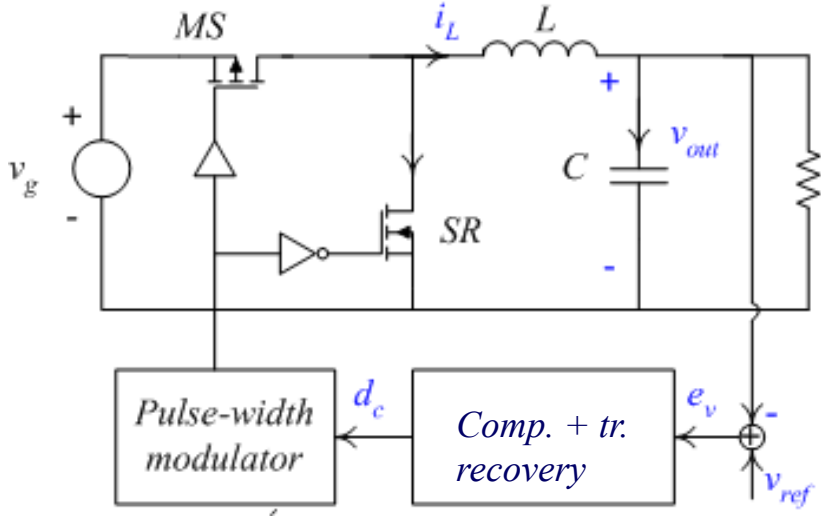


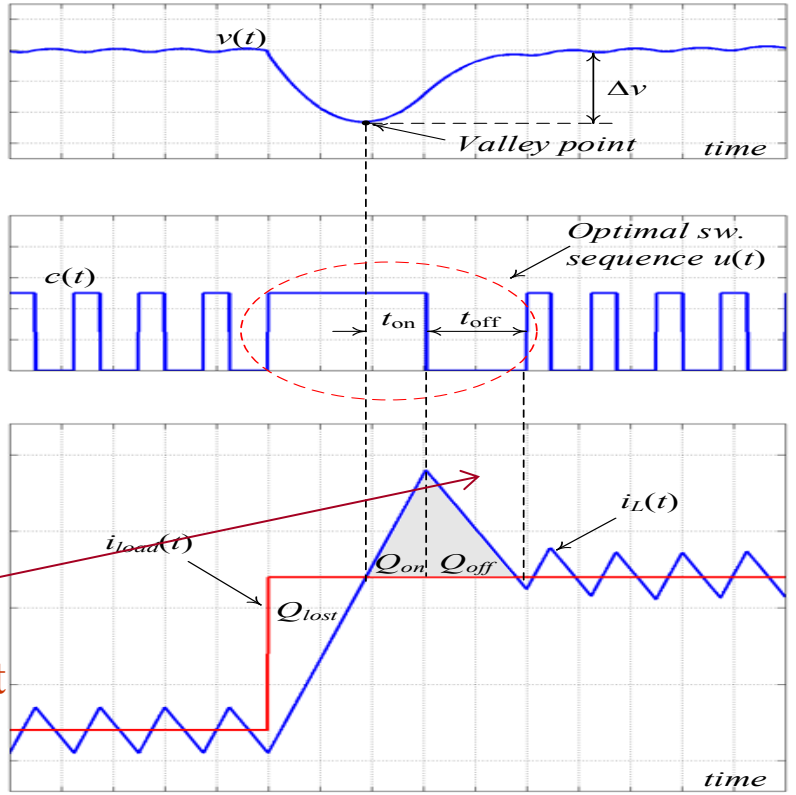
Model valid for $f << f_{sw}$ and The analysis is applicable for small variations around a steady state operating point

Frequency vs. Optimum-Time Control



Charge Based (Mixed-Signal) Time-Optimal Response





$$Q_{lost} = Qon + Qoff$$

$$Q = C\Delta V$$

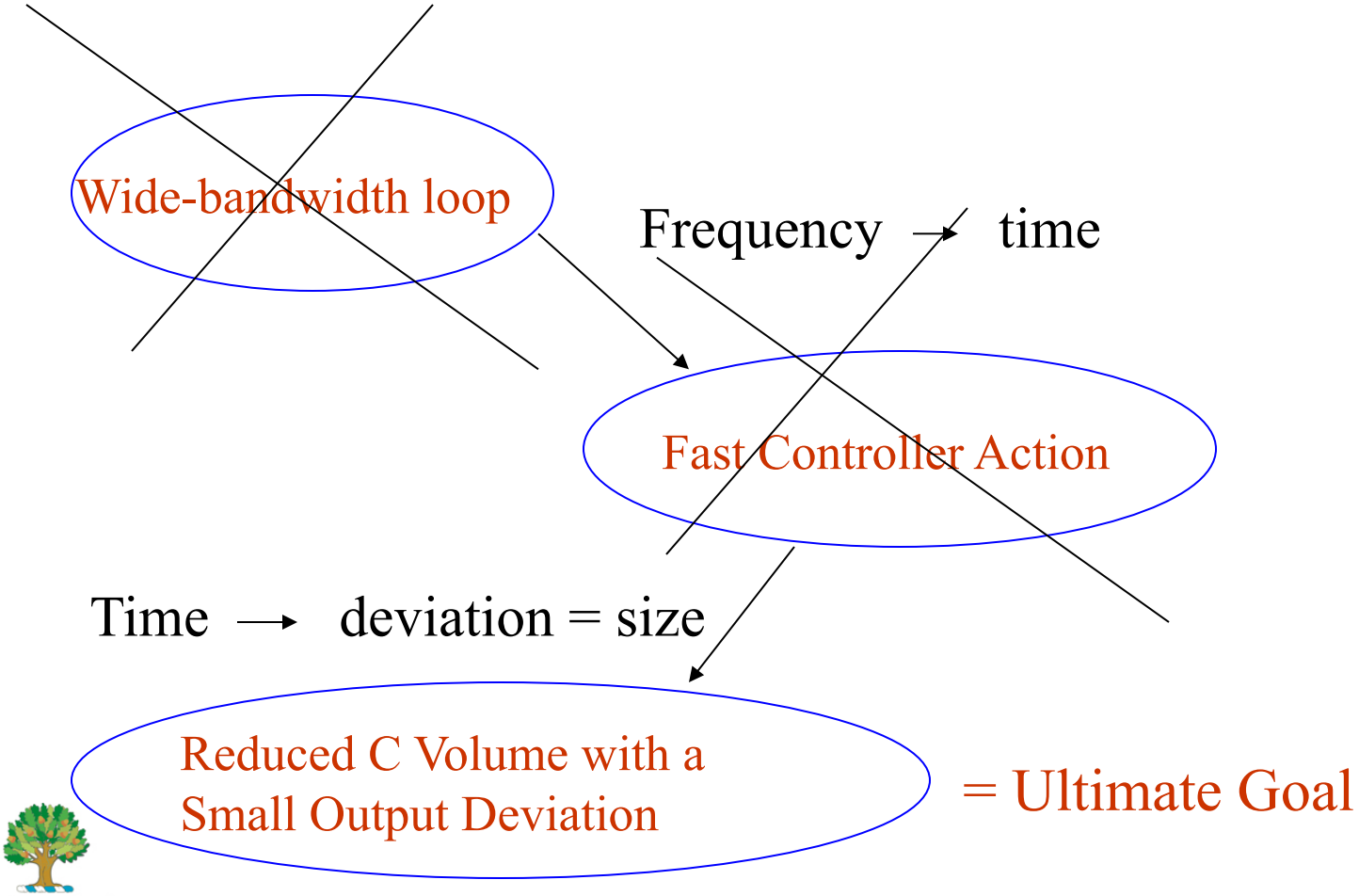
High peak current

- Capacitor reduced but the peak current results in a larger inductor, not a favorable tradeoff.
- For indirect energy transfer converter the fastest speed does not even guarantee the minimum deviation.

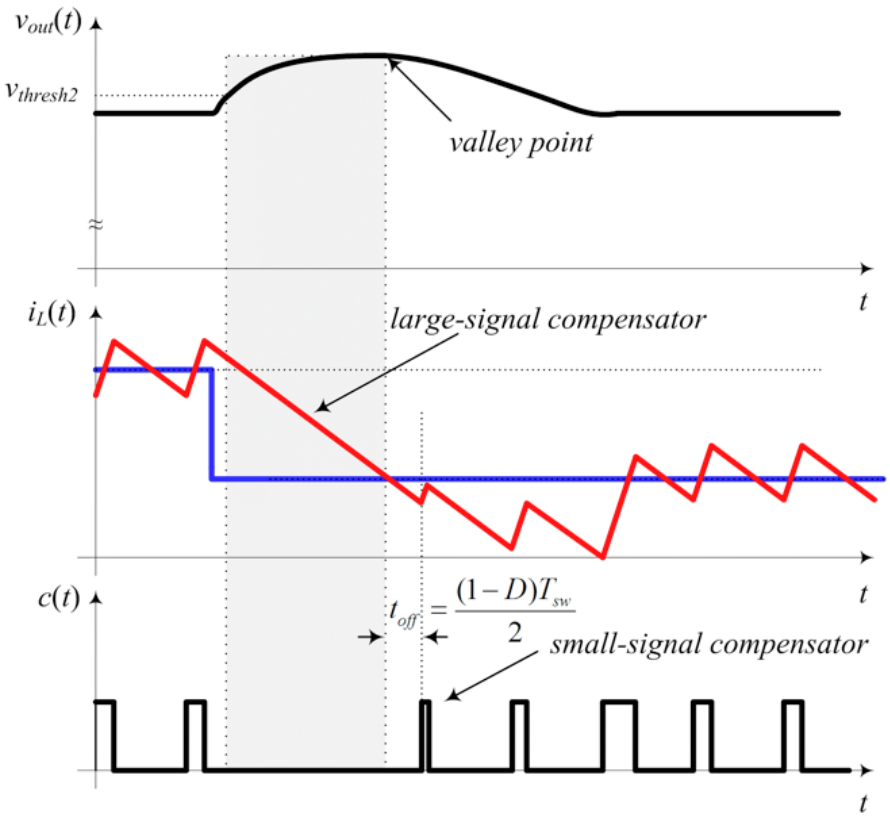
[1] W. Burns, T. Wilson "A State-Trajectory Control Law for DC-to-DC Converters", IEEE Transactions on Aerospace and Electronic Systems, January, 1978.

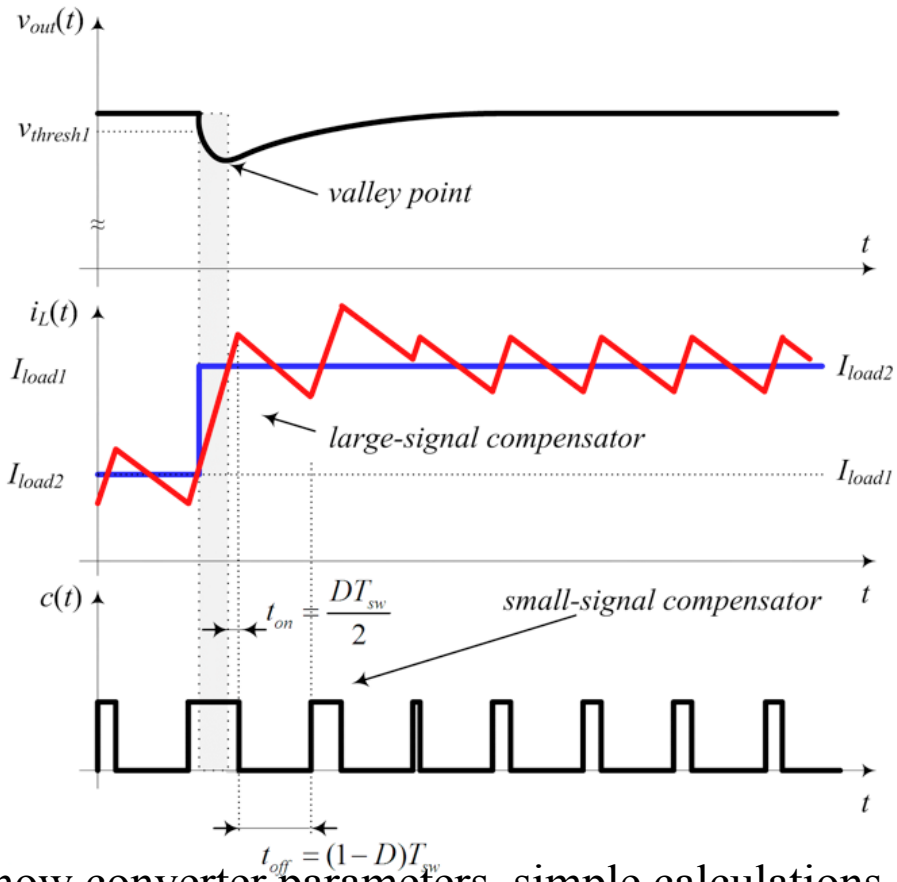
[2] F. Guang, E. Meyer, Y.-F. Liu, "A New Digital Control Algorithm to Achieve Optimal Dynamic Performance in DC-to-DC Converters," Power Electronics, IEEE Transactions on , vol.22, no.4, pp.1489-1498, July 2007.

Minimum Deviation Controller



Minimum (Optimum) Deviation Dual-Mode Controller

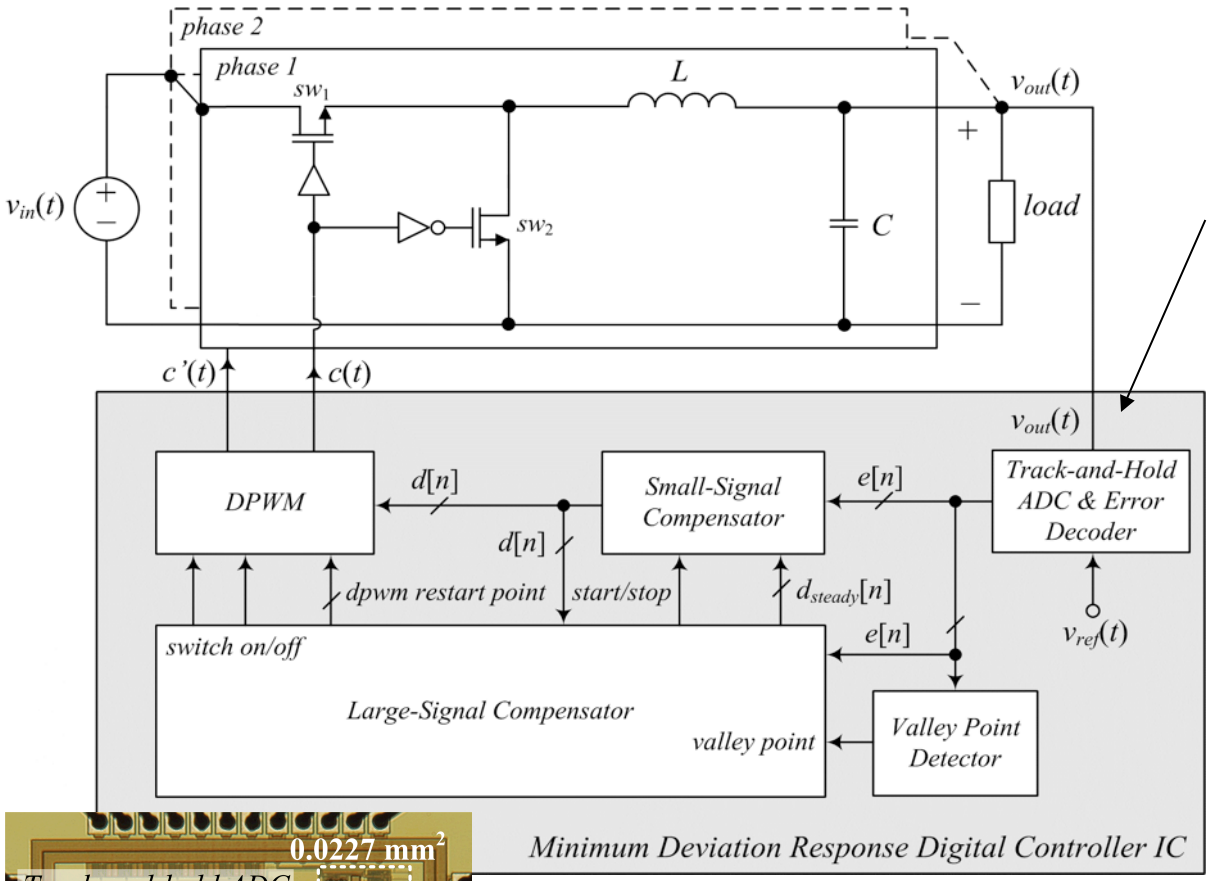




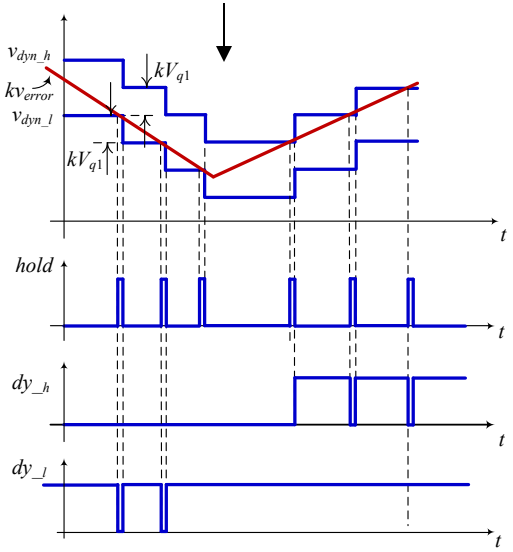
- No current overshoot, no need to know converter parameters, simple calculations

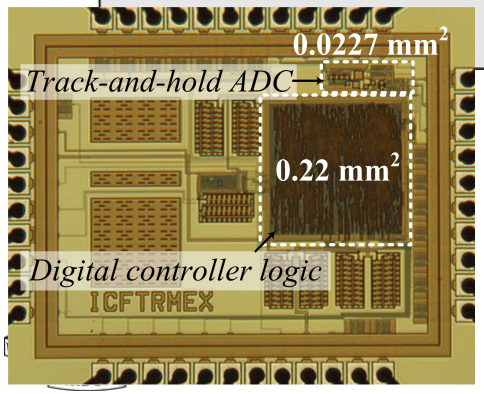
[1] A. Radić, Z. Lukić, S.M. Ahsanuzzaman, A. Prodić, and R. de Nie, "Minimum Deviation Digital Controller IC for Dc-Dc Switch-Mode Power Supplies," IEEE Trans. on Power Electronics, Sept. 2013,Vol.28.

Minimum (Optimum) Deviation Dual-Mode Controller



Track and hold asynchronous ADC with peak/valley detection operation

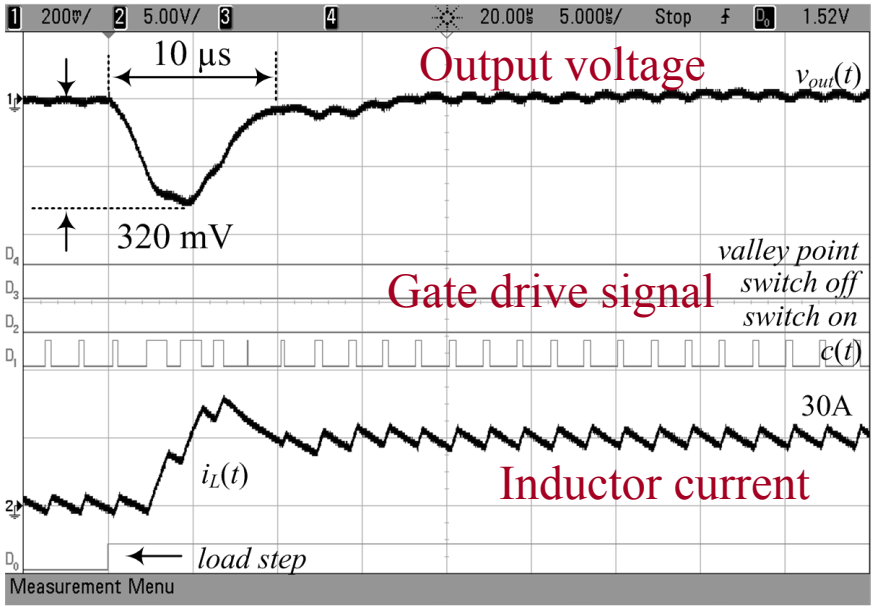


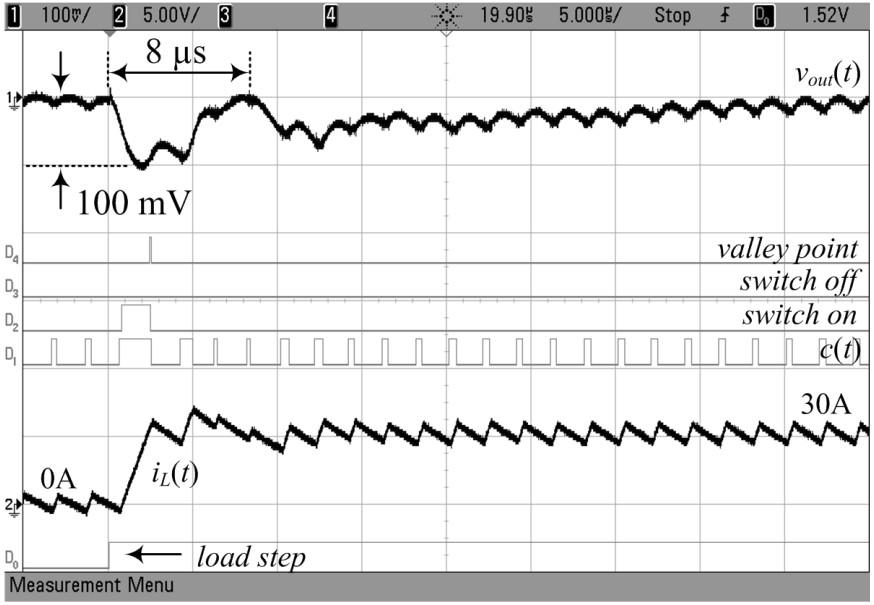


Only needs to remember D before transient no need to know the converter parameters

[1] A. Radić, Z. Lukić, S.M. Ahsanuzzaman, A. Prodić, and R. de Nie, "Minimum Deviation Digital Controller IC for Dc-Dc Switch-Mode Power Supplies," IEEE Trans. on Power Electronics, Sept. 2013,Vol.28.

Experimental Results (500 kHz VRM)





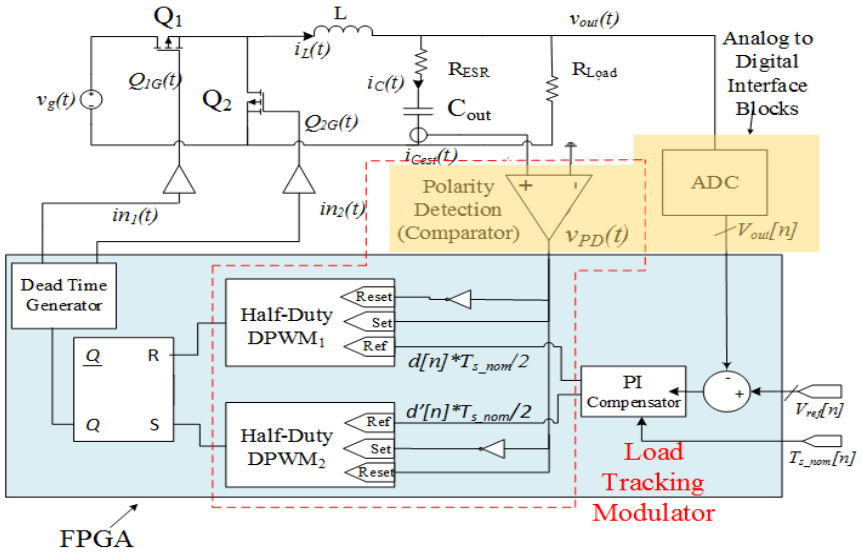
Fast PID

Optimum Deviation

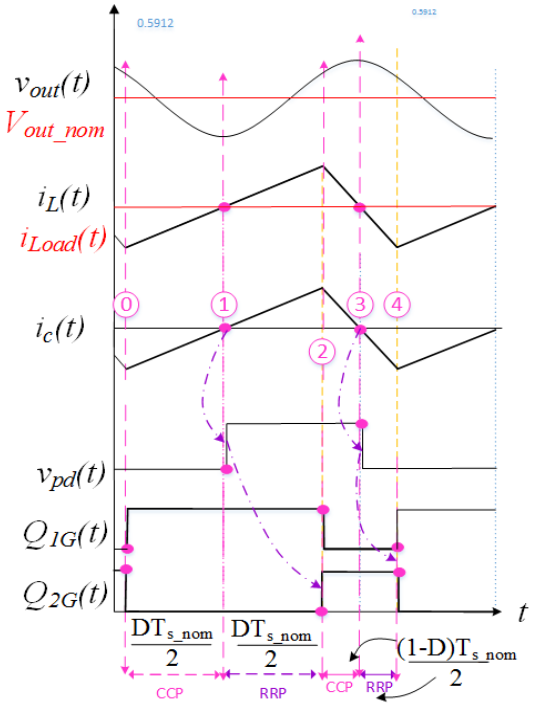
Low peak current, minimum deviation but two control modes could present a challenge and are often not desirable

[1] A. Radić, Z. Lukić, S.M. Ahsanuzzaman, A. Prodić, and R. de Nie, "Minimum Deviation Digital Controller IC for Dc-Dc Switch-Mode Power Supplies," IEEE Trans. on Power Electronics, Sept. 2013,Vol.28.

Single Mode Min. Deviation Controller



Simple modification of a conventional PWM controller



Steady state operation

- Only detect zero crossings of the outpt capacitor current and keeps transistor on/off for D/2 (positive zero crossing) or D'/2 (negative zero crossing)
- Has two PWM modulators, producing D/2 and D'/2

[1] T. Moinaoau, A. Radić, and A. Prodić, "A single mode minimum deviation controller …," IEEE APEC 2018.

Single Mode Min. Deviation Controller

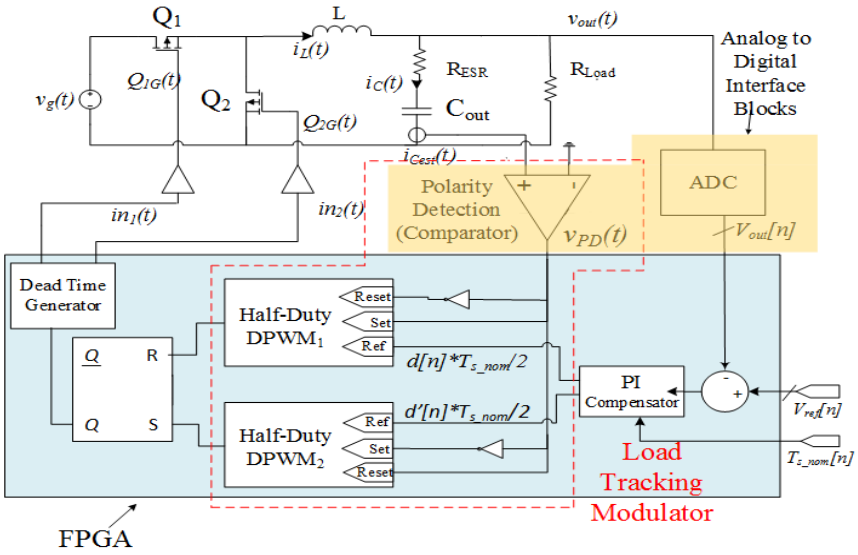
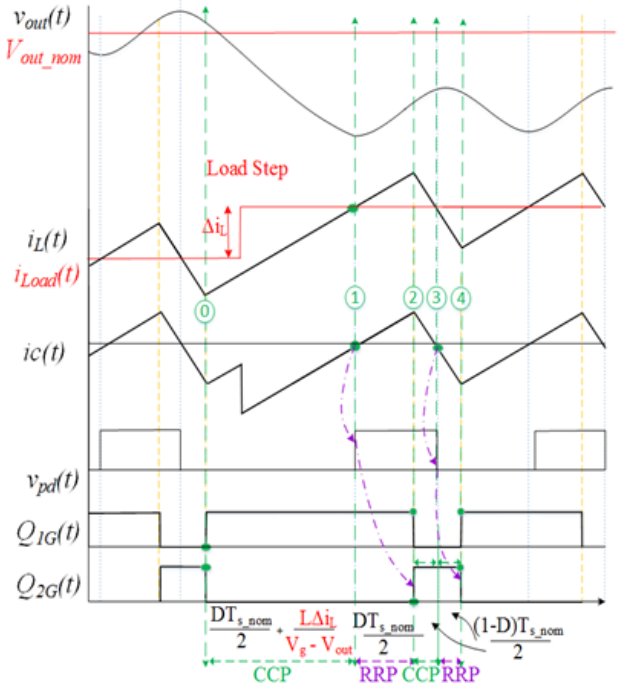


Fig. 1 A buck converter regulated by a single mode load tracking minimum deviation controller.

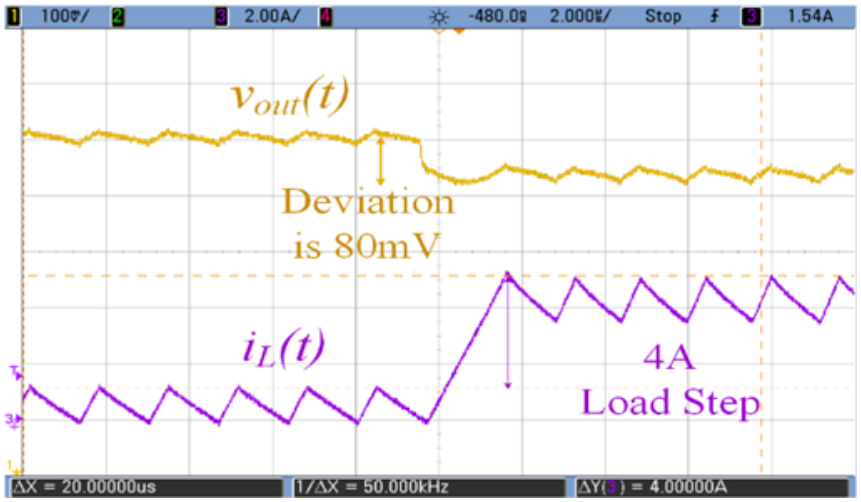


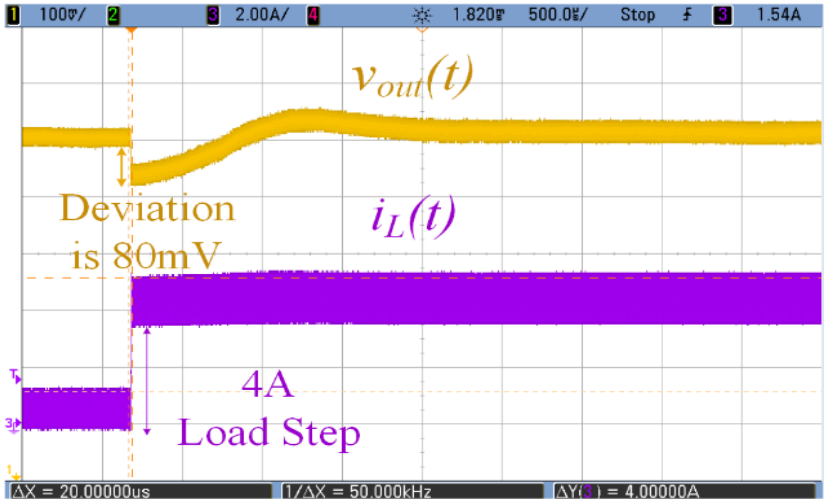
Load transient

- Only detect zero crossings of the outpt capacitor current and keeps transistor on/off for D/2 (positive zero crossing) or D'/2 (negative zero crossing)

[1] T. Moinaoau, A. Radić, and A. Prodić, "A single mode minimum deviation controller …," IEEE APEC 2018.

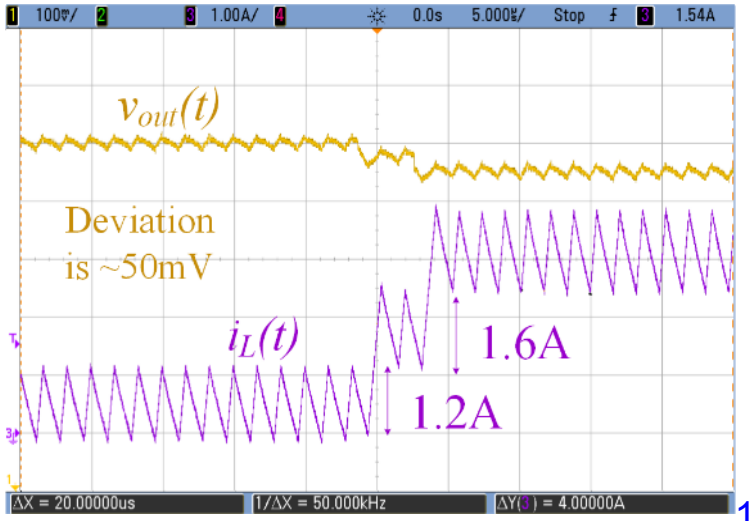
Single Mode Min. Deviation Controller – Exp. Results





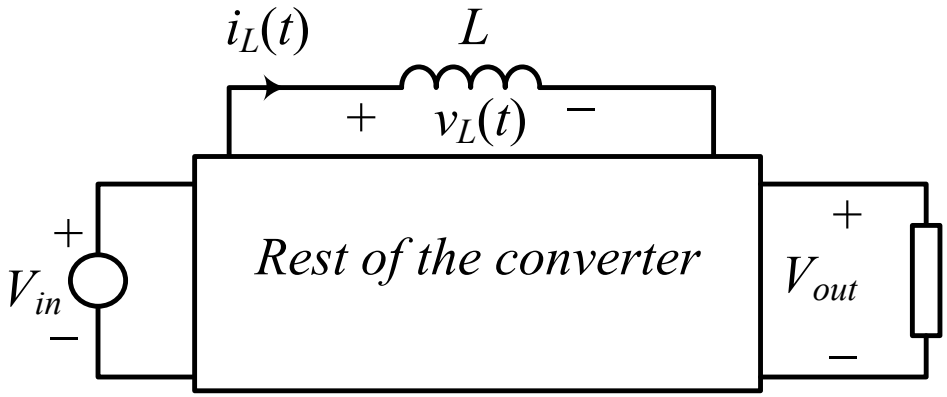
A 10% o 90% load step (0.5 A to 4.5 A)

Reacts on multiple transients without any mode-transition problems



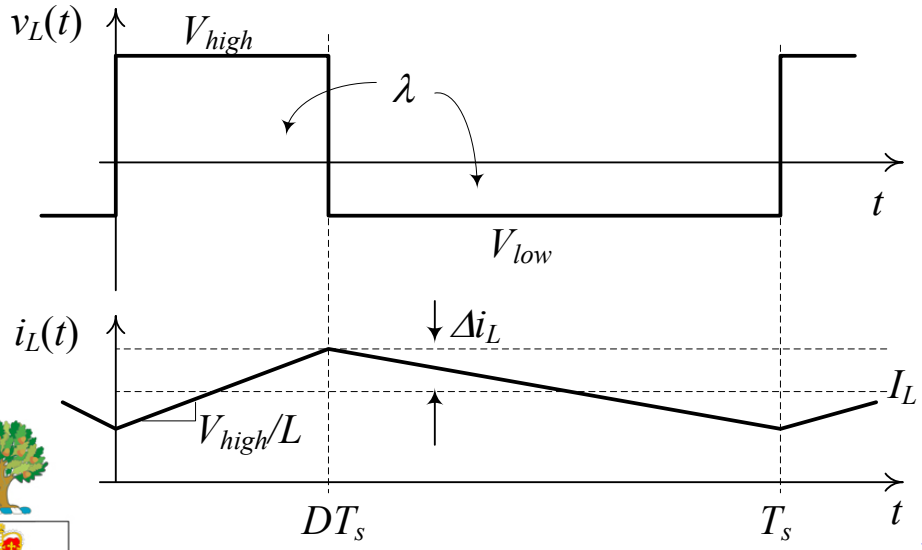
Inductor Volt-Swing Reduction Based Topologies

Voltage Swing Reduction- Fundamental Principle



- Inductor volume directly proportional to the flux linkage

$$\lambda = LI$$



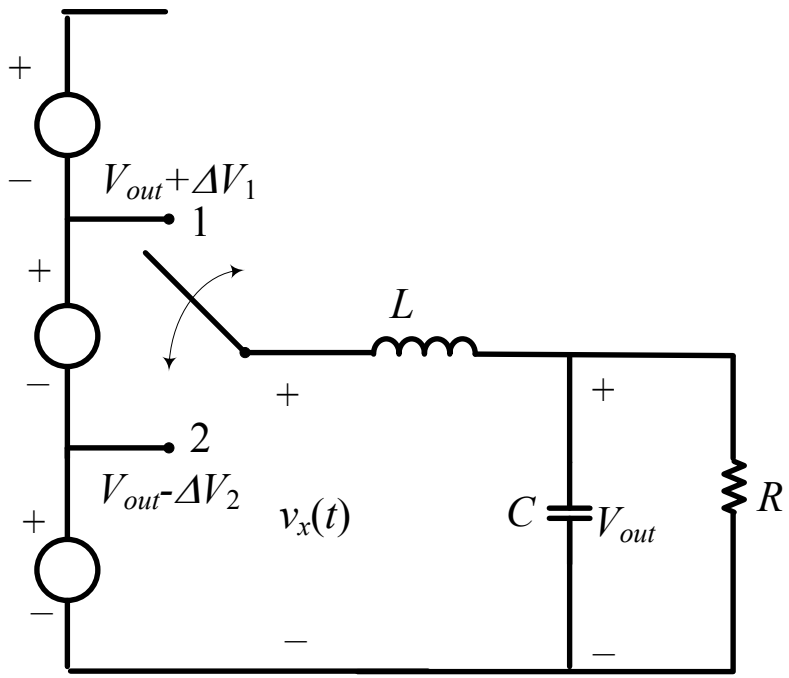
-λ usually reduced by reducing T (increasing the sw. frequency) => penalties in efficiency (we need both smaller volume and better efficiency)

- *Alternatively, λ can be reduced by minimizing voltage swing, i.e. V_{high}-V_{low}*

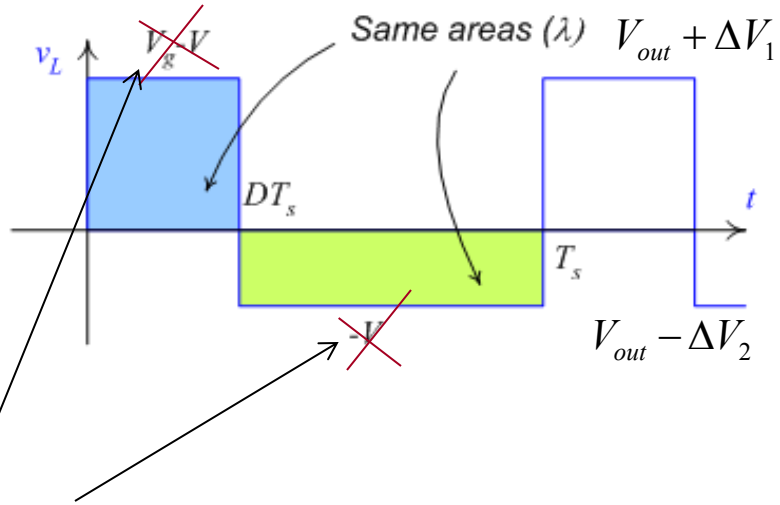
Voltage swing reduction principle

Voltage-Swing Reduction (Differential Buck Principle)

By reducing the voltage swing the inductor size (inductance value) can be drastically reduced



$$\Delta i_L = \frac{V_{L\_1}\cdot D}{2\cdot L\cdot f_{sw}} = \frac{V_{L\_2}\cdot(1-D)}{2\cdot L\cdot f_{sw}}$$

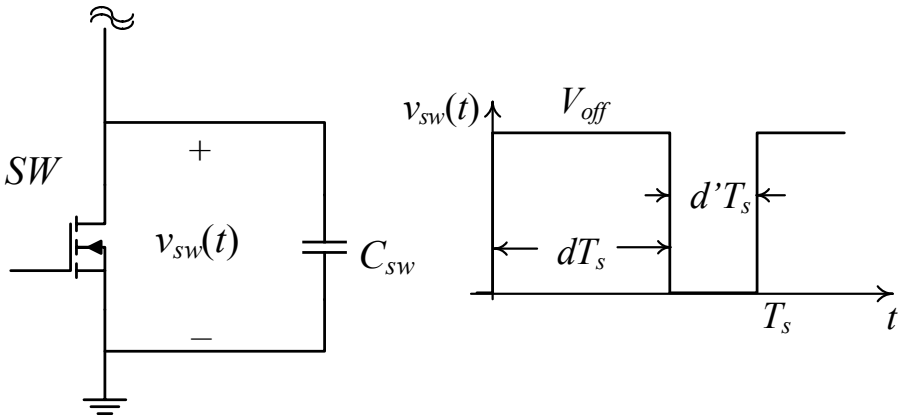


Two values of the switch node voltages can be set closer to the output voltage value. We don't need to have two dc references (of v_x) at 0 and Vg.

Voltage Swing Reduction: Switching and Conduction Losses

Side benefits (byproducts): Reduction of voltage stress of the components allowing for power processing efficiency improvements and **cost-effective** implementation with components **having a better figure of merit (FOM)**

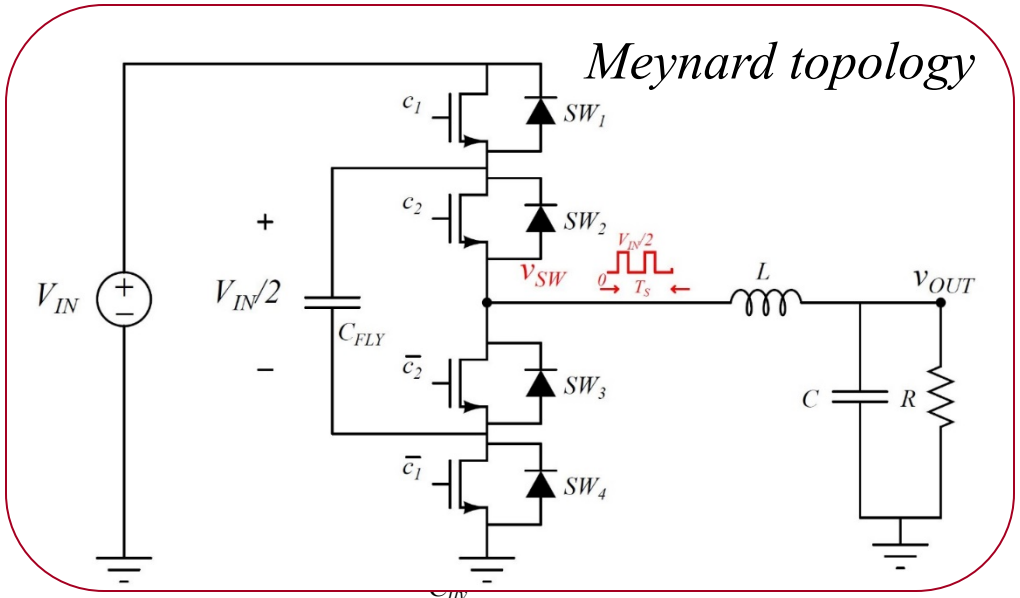
$$Psw \approx f\left(\frac{1}{2}CVoff^2\right)$$



Conduction losses: transistor on resistances and the resistance of the inductor can be lower

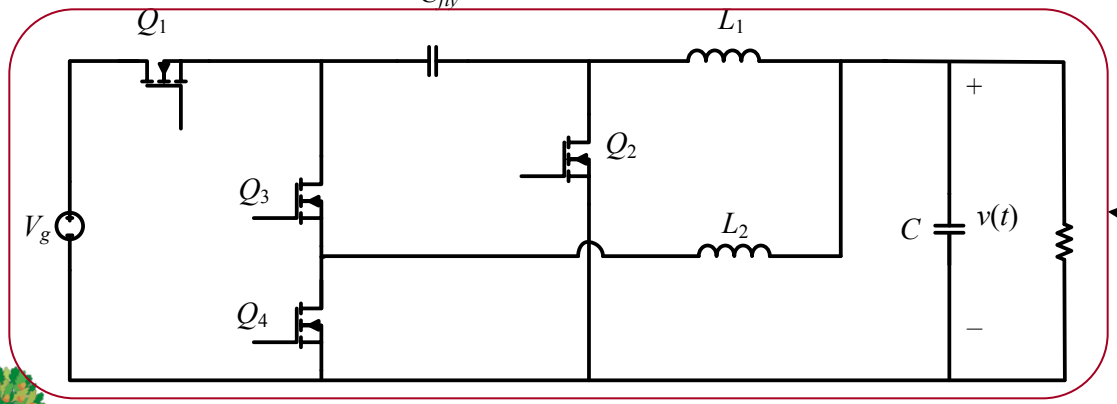
Indication that by reducing voltage swing we can actually gain both reduced volume and improved power processing efficiency.

Three (Multi) Level Flying Capacitor Topologies



Provide voltage swing reduction and lower braking voltage through utilization of a flying capacitor, which value is kept at Vin/2

Balancing of FC needed for some control methods



Naturally balanced but Q_4 rated for the full input voltage

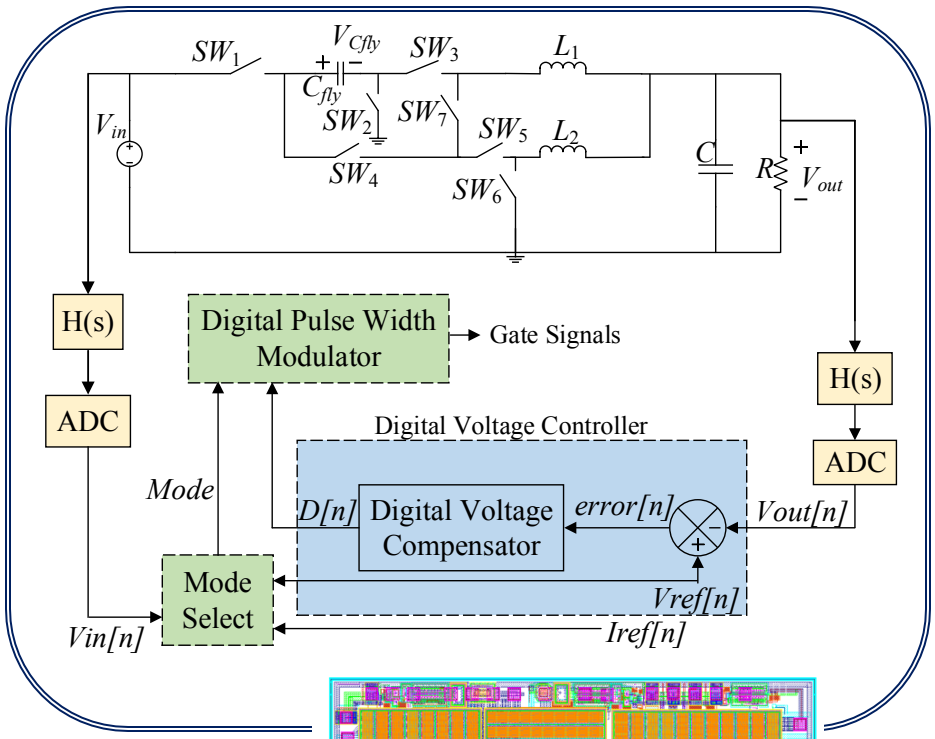
$$V_{out} < V_g / 4$$

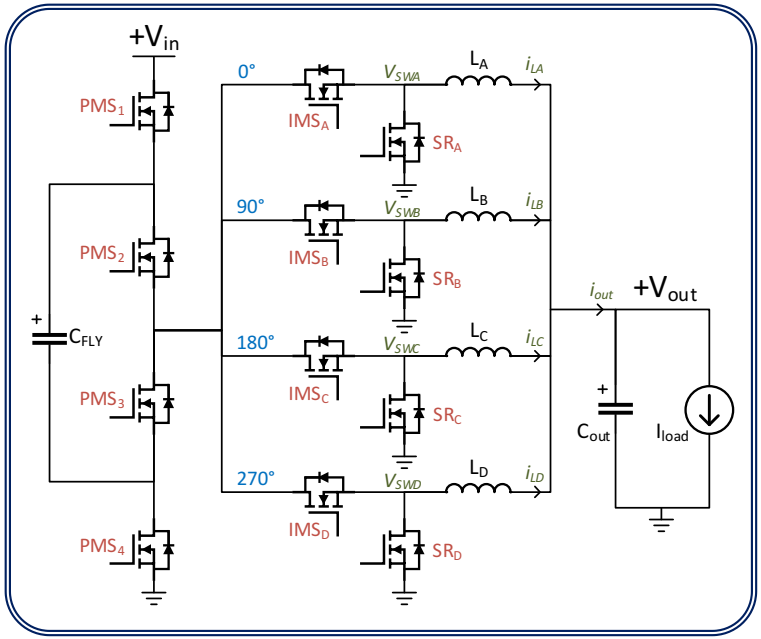
Nishijima – Series Cap Buck

[1] T.A. Meynard, H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," *in Proc. IEEE PESC* '92, vol. 1. pp.397-403 July 1992.

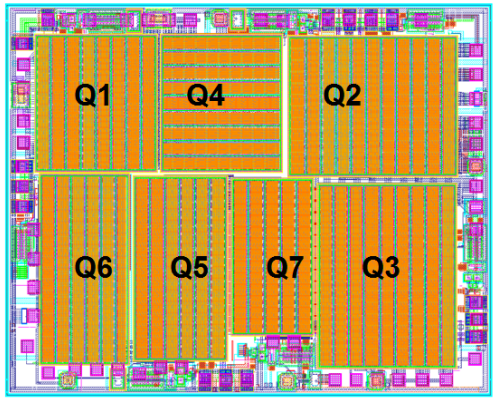
[2] K. Nishijima,K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "Analysis of Double Step-Down Two-Phase Buck Converter for VRM," *Telecommunications Conference, 2005. INTELEC '05. Twenty-Seventh International* , pp.497,502, Sept. 2005

Three (Multi) Level Flying Capacitor Topologies





24 V to 1 V, 120 A, 93% efficient topology with single loop cap balancing



[1] P. Jain, A, Prodić, and A. Gerfer, "Wide-Input High Power Density Flexible Converter Topology for Dc-Dc Applications," *in Proc. IEEE Applied Power Electronics Conference (APEC)*, 2016.

[2] G Roberts, N Vukadinović, A Prodić, "A multi-level, multi-phase buck converter with shared flying capacitor for VRM applications," *in Proc. IEEE Applied Power Electronics Conference (APEC)*, 2018.

Control of Hybrid Multi-Level FC Topologies

Reasons for not Using FC Converters
(Sceptics Guide on Trashing FC Converters Idea)

- *Flying capacitor instability problems in:*
  - *PWM voltage mode*
  - *Peak current programmed mode*
  - *Average current programmed mode*
- *Challenges of operating at light loads*
- *Start-up and input load transient challenges [1]*
- *Different failure mechanisms compared to conventional structures*
- *Not fully understood/explored system dynamics*
- *Pin count (pad ring) increase for IC implementation*
- *Losses of flying capacitor esr…*

[1] M. Halamicek, T. Moiannou, N. Vukadinović, and A. Prodić "Capacitive divider based passive start-up methods for flying capacitor step-down dc-dc converter topologies," *in Proc. IEEE ECCE-Asia/IPEC*, 2018.

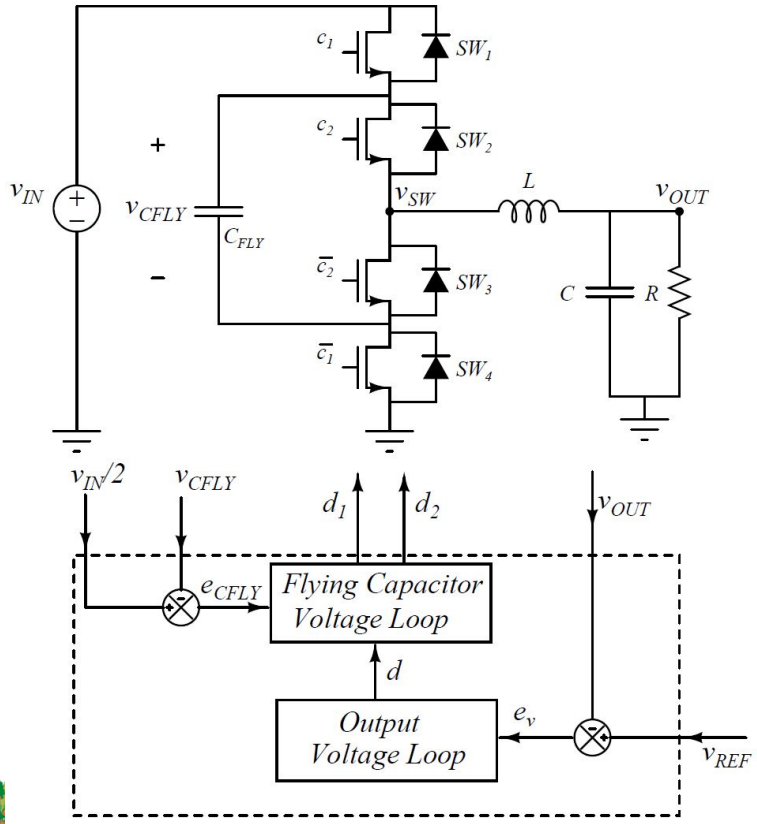
There are Some Good Control News as Well

- *Further improvement of transient response performance (further reduction of the output capacitor)* ☺
- *Opening possibilities for on-line efficiency improvement* ☺
- *Create opportunities for new (digital) control methods to make them even smaller and/or more efficient* ☺

Potential benefits are just too good to quit on the idea and, again, the existing solutions just cannot keep on with some emerging requirements (increased conversion ratio and power ratings)

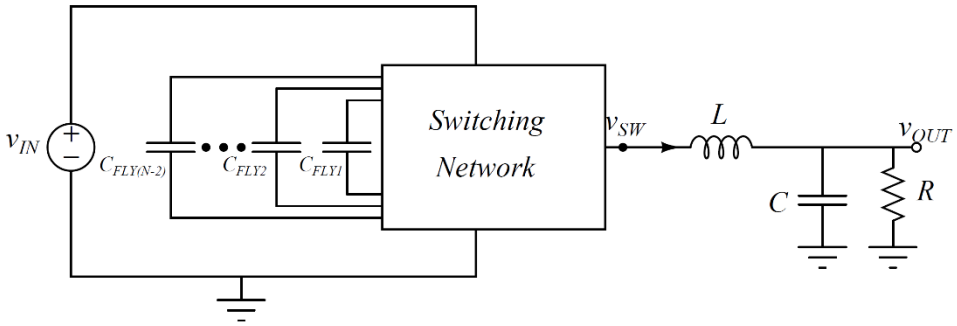
PWM Voltage Mode Flying Capacitor Balancing Challenges and Solutions

Flying Capacitor Voltage Balancing



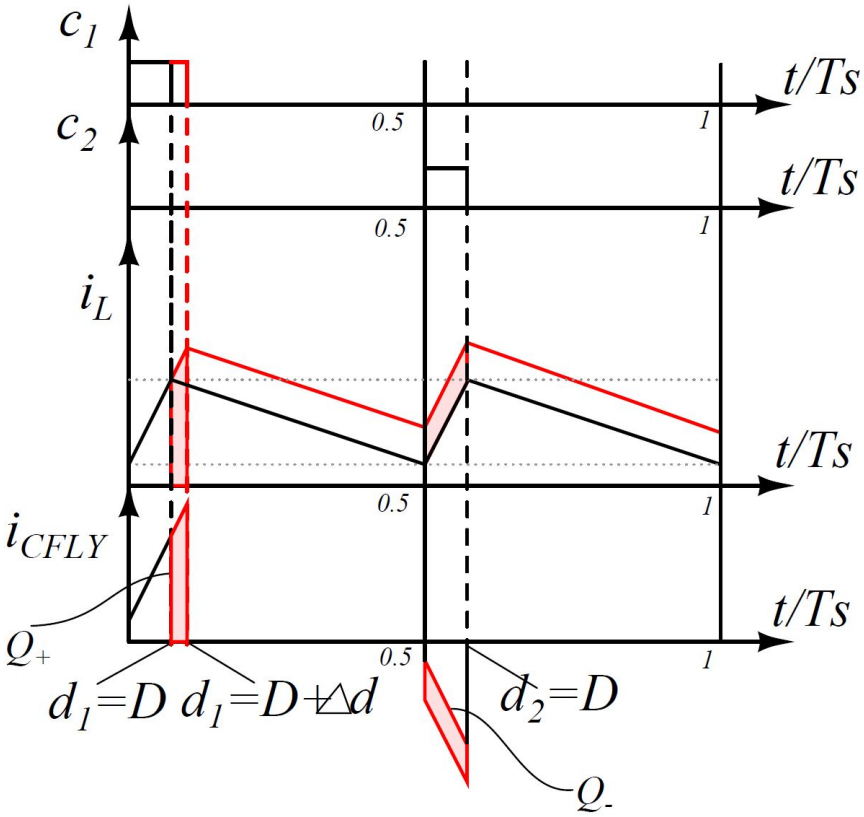
Ideally the flying capacitor is at Vg/2, in practice, due to circuit imperfections and tolerances the value is constant but not at Vg/2.

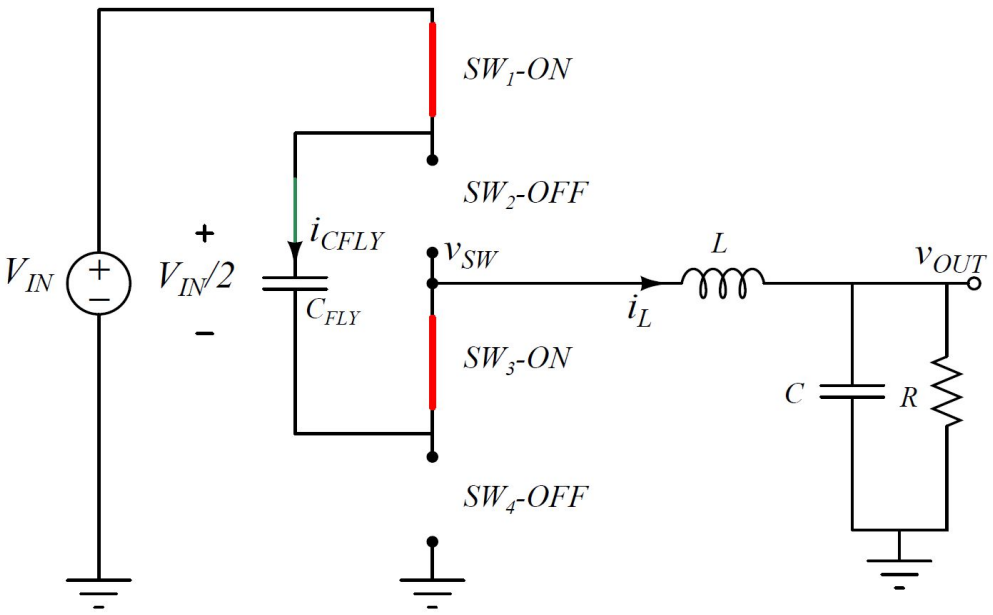
However, problems occur for non-negligible current ripple (Positive feedback)



Higher order FC multi-level converter

Flying Capacitor Voltage Balancing

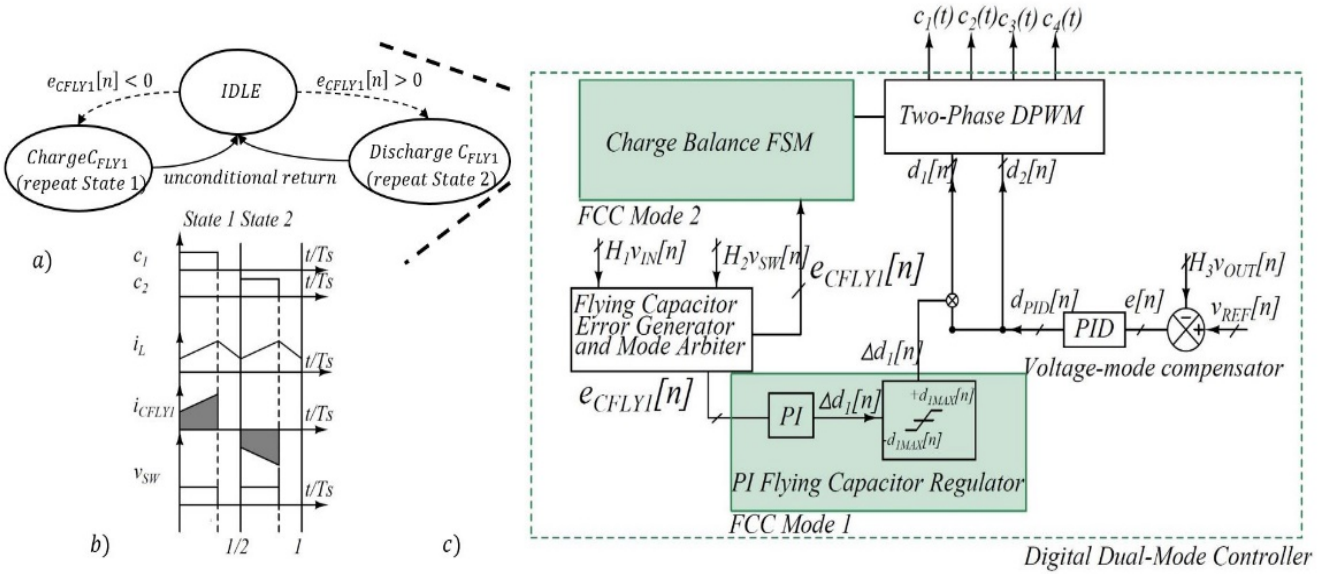




For example, when $V_{fly}<V_{in}/2$ increase in d_1 can cause more charge to be taken than put in the flying cap (positive feedback), due to the ripple.

[1] Nenad Vukadinović, Aleksandar Prodić, Brett A Miwa, Cory B Arnold, Michael W Baker, "Extended wide-load range model for multi-level Dc-Dc converters and a practical dual-mode digital controller," IEEE APEC 2016.
[2] N Vukadinovic, A Prodic, BA Miwa, CB Arnold, MW Baker, "Discontinuous conduction mode of multi-level flying capacitor DC-DC converters and light-load digital controller," IEEE COMPEL 2017

Two-Mode Controller for The FC Loop



- *Two mode controller, at lighter load repeats charging or discharging state when deviation of flying cap voltage is detected and at heavier changes duty ratio.*
- *Single mode impractical due to large variations in flying cap value for heavy load*

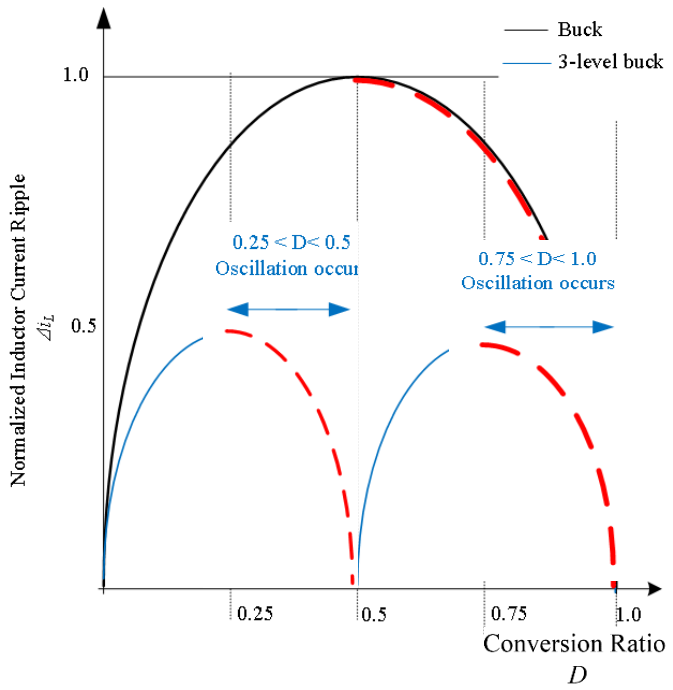
[1] Nenad Vukadinović, Aleksandar Prodić, Brett A Miwa, Cory B Arnold, Michael W Baker, "Extended wide-load range model for multi-level Dc-Dc converters and a practical dual-mode digital controller," IEEE APEC 2016.
[2] N Vukadinovic, A Prodic, BA Miwa, CB Arnold, MW Baker, "Discontinuous conduction mode of multi-level flying capacitor DC-DC converters and light-load digital controller," IEEE COMPEL 2017

CPM Control Challenges

And Solutions

Multiple Period Doubling Oscillation Regions and a Zero Ripple Region for Peak CPM

v_{Cfly} runaway condition worse than voltage mode control as the duty-cycle varies with a fixed peak command [1].FC goes unstable by itself.



Control Challenges:

1. *Peak CPM controller without slope compensation is inherently unstable for* ***0.25 < D < 0.5***

and

0.75 < D < 1.0

for three-slope converters.

2.Around M(D) = 0.5, there is near zero ripple, so Peak/Valley CPM, relying on ripple, cannot work directly.

[1] L Lu, SM Ahsanuzzaman, A Prodic, G Calabrese, G Frattini, M Granato, "Peak offsetting based CPM controller for multi-level flying capacitor converters IEEE APEC 2018

Other CPM Methods

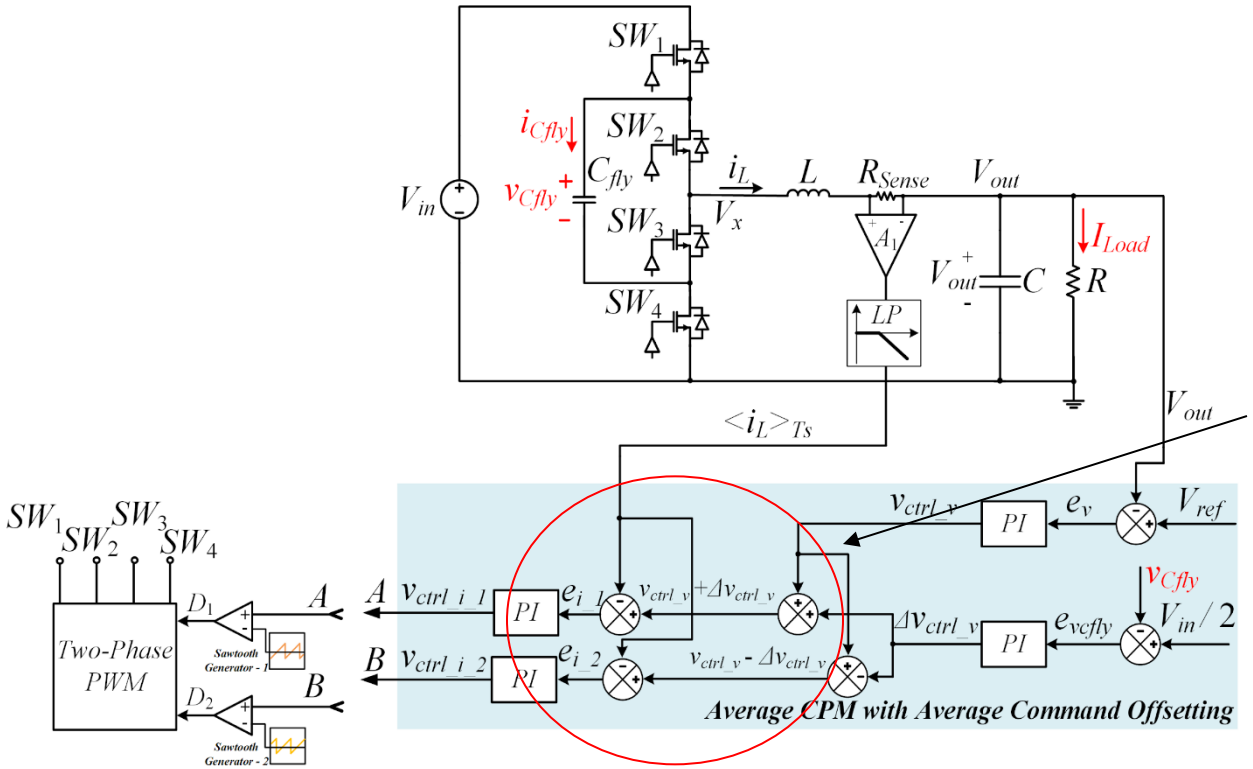
CPM Type/ FC Oscillations	*Stable Duty-Cycle Operating Range*
Peak CPM/ Yes	*0 < D < 0.25* *0.5 < D < 0.75*
Valley CPM/ No	*0.25 < D < 0.5* *0.75 < D < 1.00*
Average CPM/ Yes	*0 < D < 1.00*

Valley CPM provides FC stability [1] but does not provide inherent current protection of main (direct energy transfer) switches

[1] JS Rentmeister, C Schaef, BX Foo, JT Stauth, "A flying capacitor multilevel converter with sampled valley-current detection for multi-mode operation and capacitor voltage balancing," IEEE ECCE 2016,

[2] L. Lu, S. M. Ahsanuzzaman, A. Prodic, G. Calabrese, G. Frattini, and M. Granato. "Digital Average CPM Conrol for Multi-level Flying Capacitor Converters ". *IEEE COMPEL 2018*.

Peak Offsetting CPM Controller

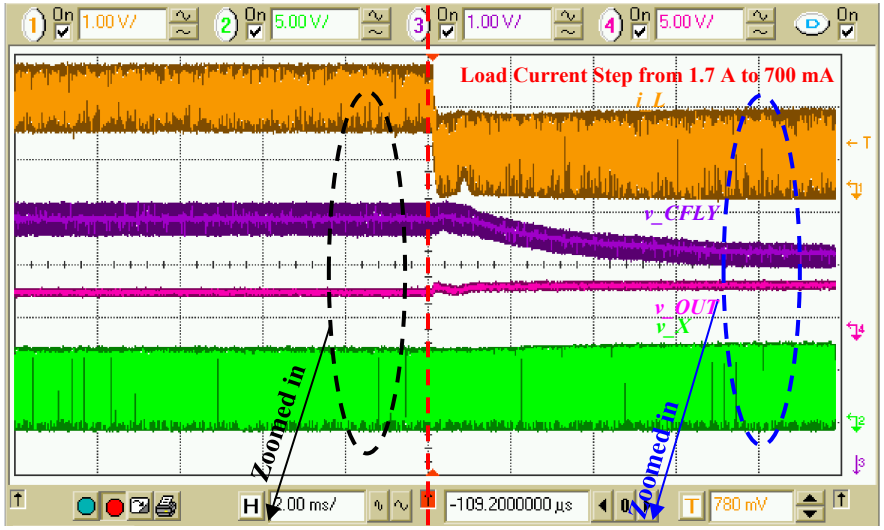


Based on voltage difference between v_{cfly} and Vg/2 brings positive and negative offsets to two consecutive current reference signals

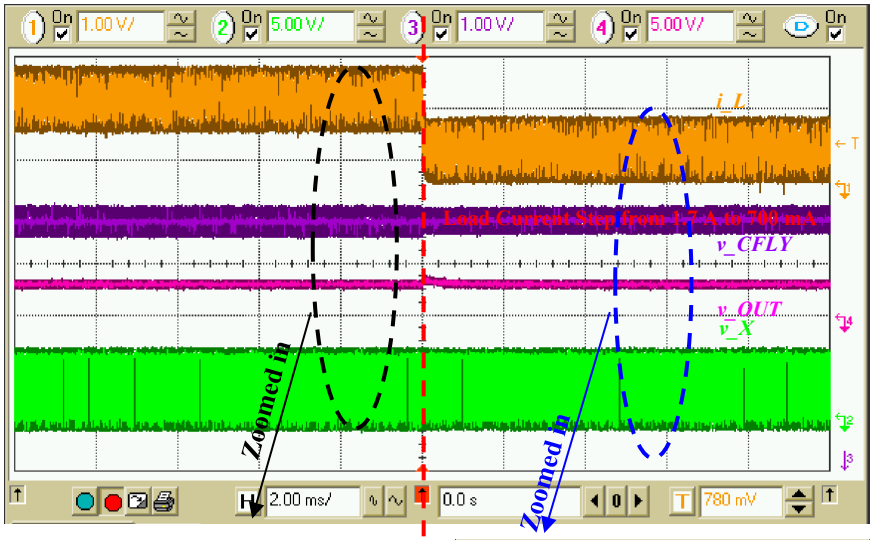
[1] L Lu, SM Ahsanuzzaman, A Prodic, G Calabrese, G Frattini, M Granato, "Peak offsetting based CPM controller for multi-level flying capacitor converters IEEE APEC 2018

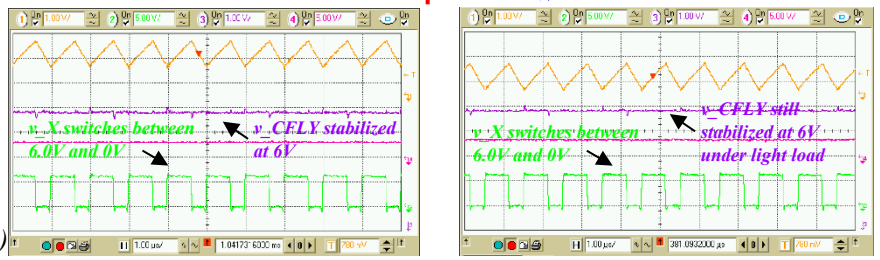
[2] L. Lu, S. M. Ahsanuzzaman, A. Prodic, G. Calabrese, G. Frattini, and M. Granato. "Digital Average CPM Conrol for Multi-level Flying Capacitor Converters ". *IEEE COMPEL 2018*.

Experimental Results



(a)

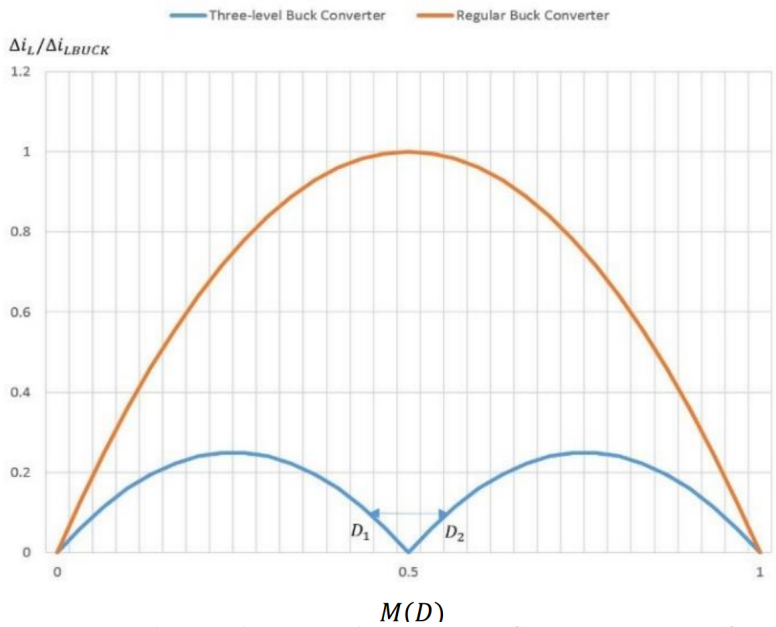




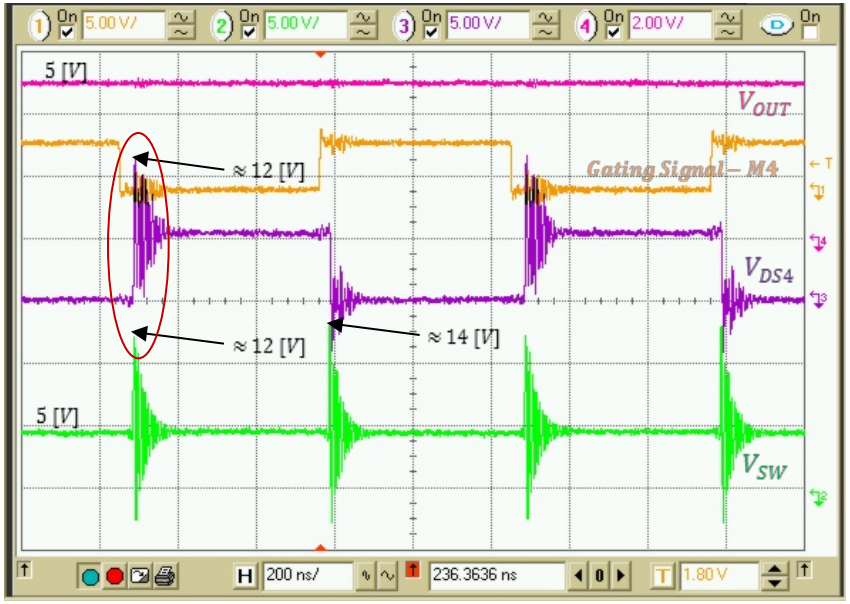
(b)

Failure Mechanisms: Voltage Spikes at Zero Ripple Operating Points

Voltage Spikes for Zero-Ripple Operating Points



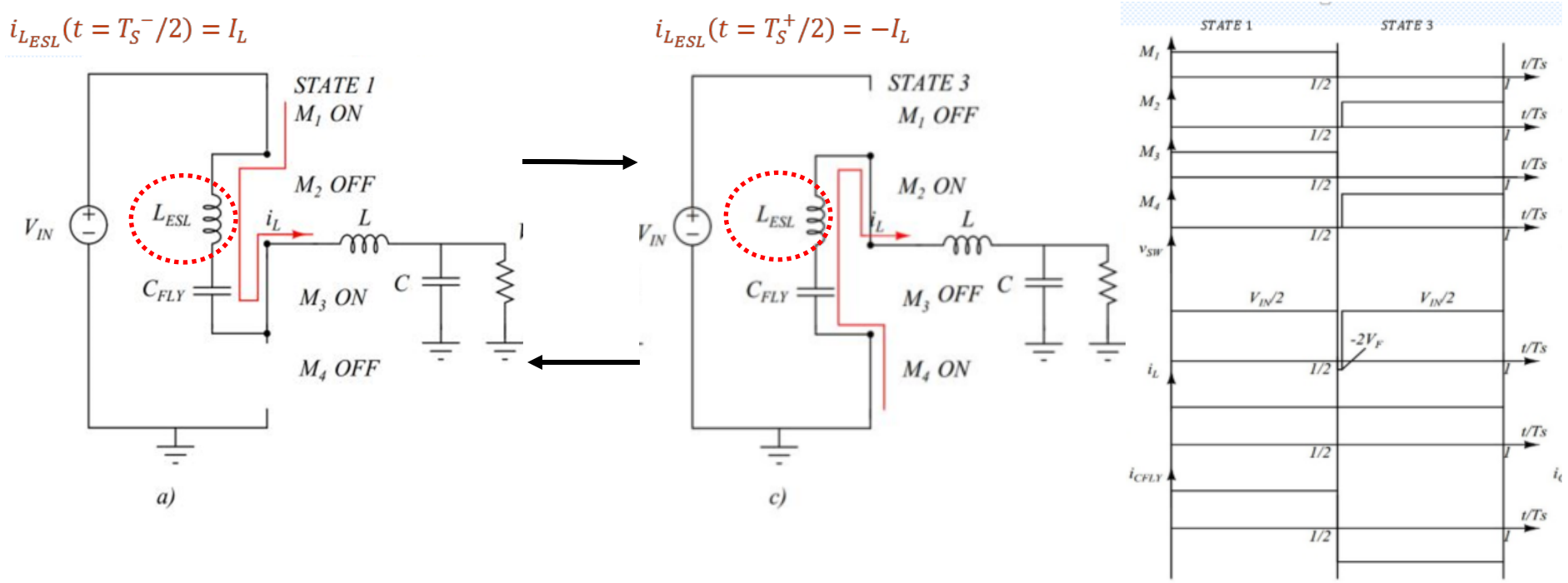
Normalized ripple as a function of M(D)



At zero ripple points (M(D)=0.5 for 3-level buck) high voltage spikes that can destroy components can be noticed.

Potential advantages of the low voltage rating transistors could be lost.

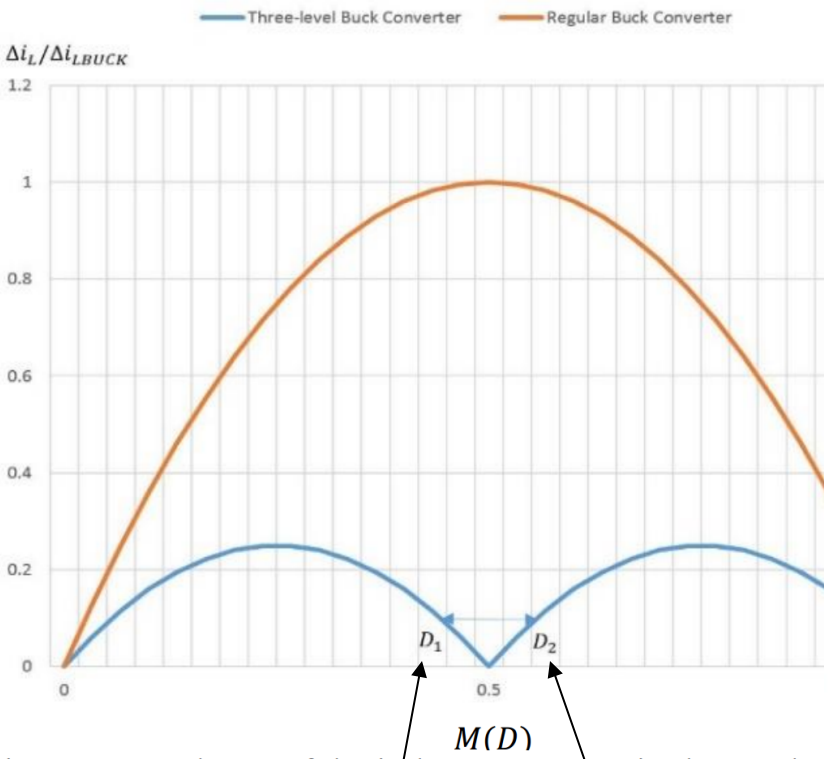
Operation For M(D) = 0.5 and Voltage Spikes

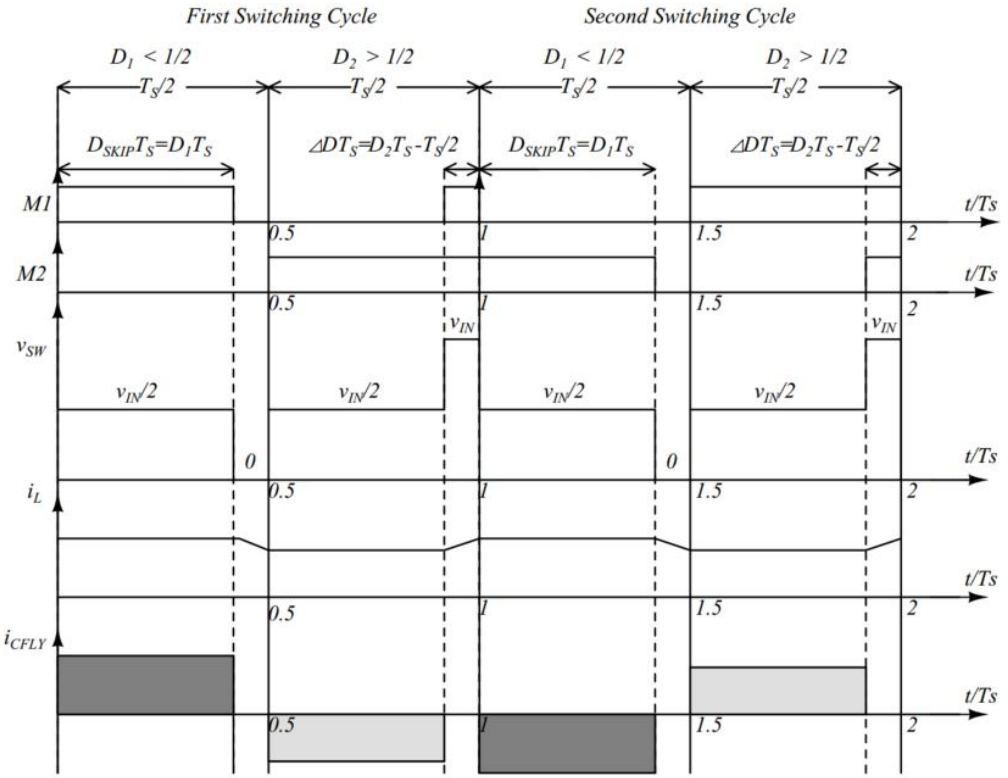


- *Current of the FC parasitic inductance is forced to move between +/- I causing high voltage spikes (di/dt)*

[1] Nenad Vukadinović, Aleksandar Prodić, Brett A Miwa, Cory B Arnold, Michael W Baker, "Skip-duty control method for minimizing switching stress in low-power multi-level Dc-Dc converters," IEEE COMPEL 2015,

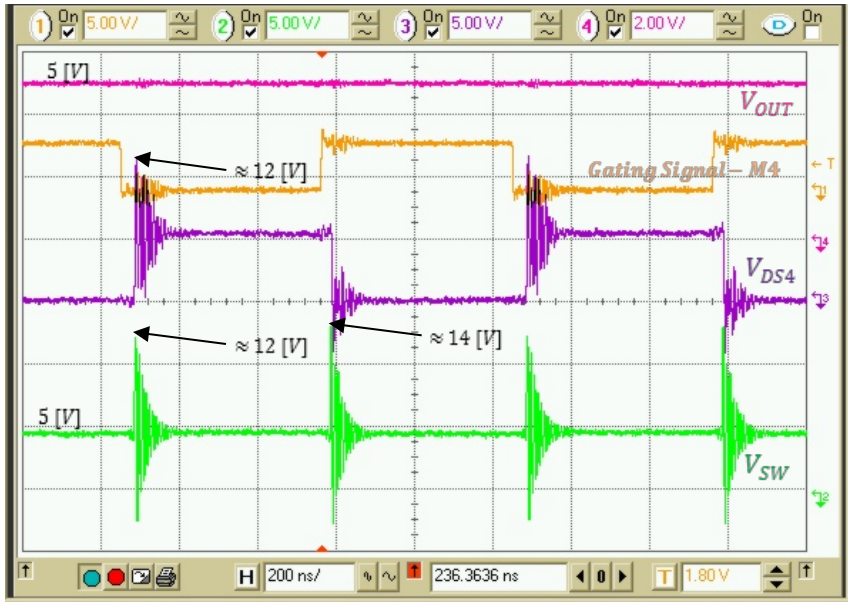
Elimination Through Skip-Duty & Sequencing





For M(D) required to be 0.5 "jumping" between two values resulting in 0.5 average and sequencing is applied. Sequencing needed to maintain symmetric current ripple.

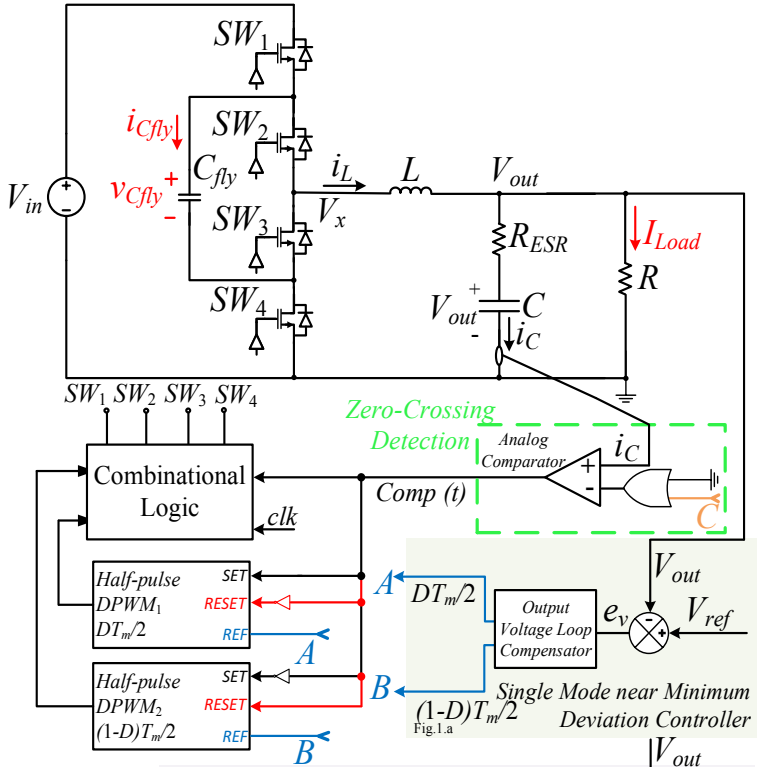
Experimental Results

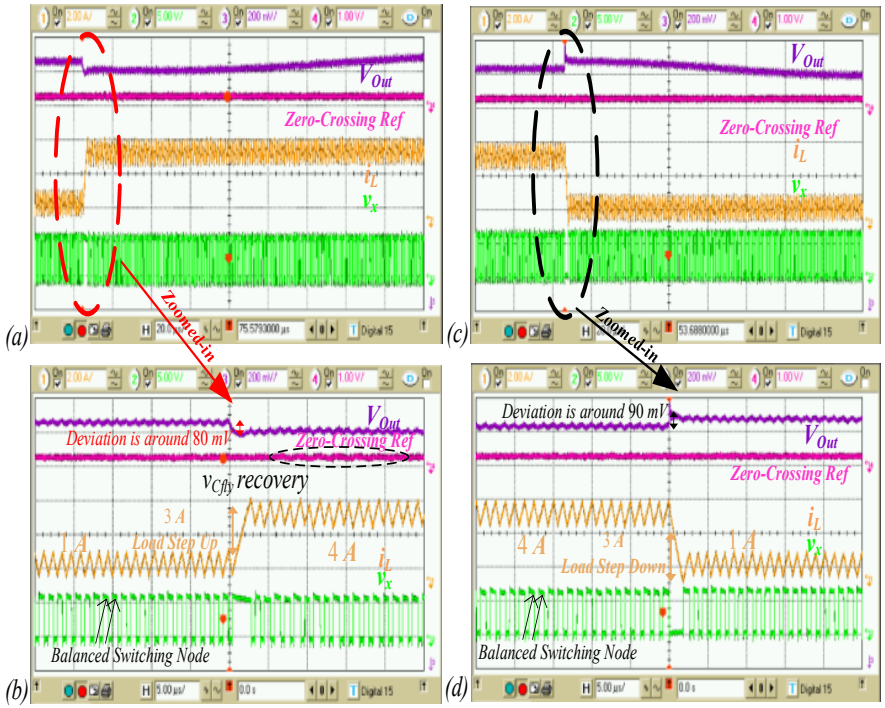


Comparison of the steady state operation of 3-level buck converter for M(D) = 0.5. a) Conventional controller (left) and b) Skip-duty controller (right). For both waveforms: Ch1. - 5 [V]/div: digital control signal of the low side M4 switch (Fig 1.), Ch2. – 5[V]/div: $V_{SW,}$ switching node voltage, Ch3. – 5[V]/div: $V_{DS4,}$ Drain-source voltage of the low side M4 switch (Fig 1.), Ch4. – 2[V]/div: $V_{OUT,}$ output voltage of the converter.

Some Good News: Transient Response Improvement and On-Line Efficiency Optimization

Transient Response Improvement (with Single Mode Minimum Deviation Controller)

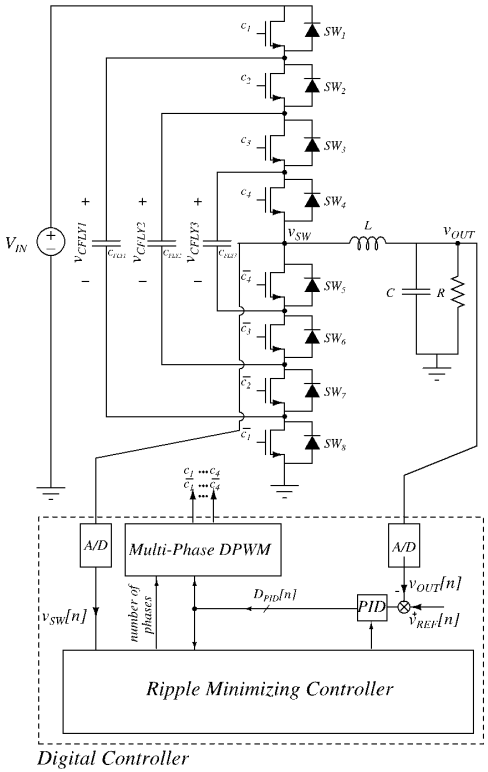




For two top switches on provide faster response than that of conventional converters (smaller)

[1] L. Liu, A Prodić, G. Calabrese, M. Granato, and G. Frattini, "Single-Mode Minimum Deviation Controller for Multi-Level Dc-Dc Converters", to be presented at IEEE APEC 2019.

On-Line Efficiency (Ripple) Optimization Through Adaptive 3-4 Level Mode Operation



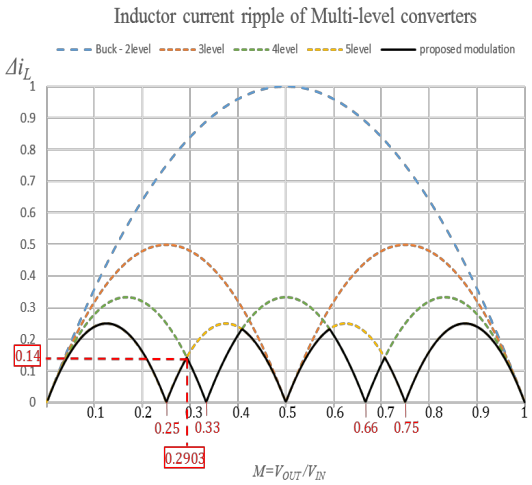
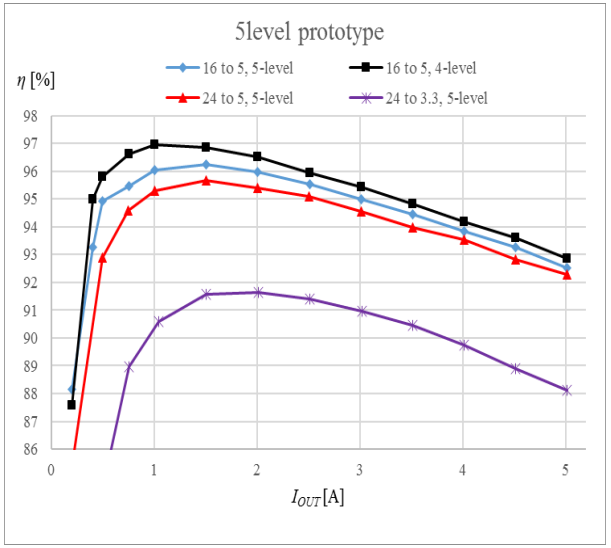


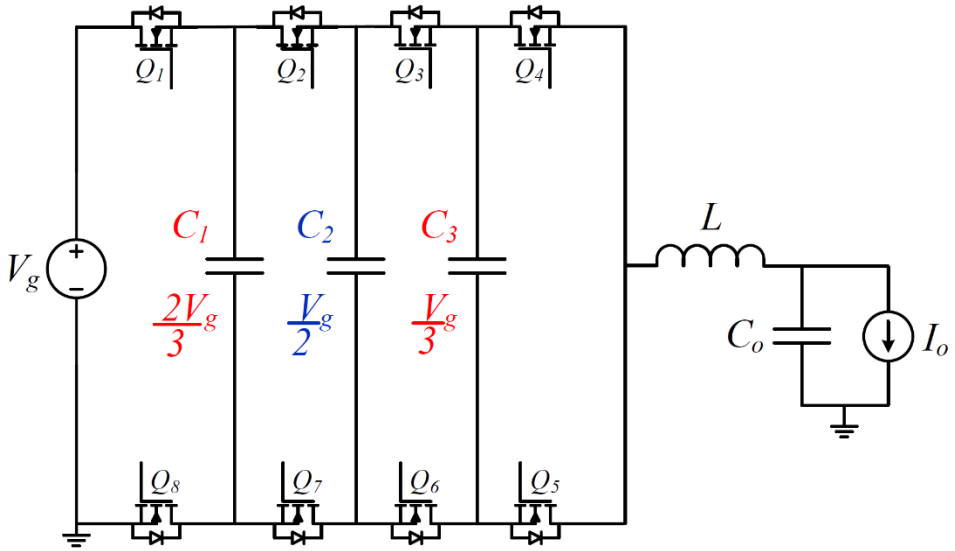
Fig. 3. Normalized inductor current ripple for the buck, 3,4 and 5 level converters.



On-line change of the number of levels to minimize the ripple (losses), could be useful for wide input dc-dc and rectifiers.

[1] N Vukadinović, A Prodić, BA Miwa, CB Arnold, MW Baker, "Ripple minimizing digital controller for flying capacitor dc-dc converters based on dynamic mode levels switching", IEEE APEC 2017.

Control-Based Increase of the Effective Number of Levels for FC Converters (further L reduction)

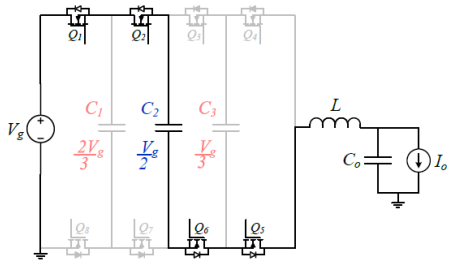


Conventional Modulation	Asymmetric Modulation
5	7
7	13
9	21
11	31
13	43
15	57

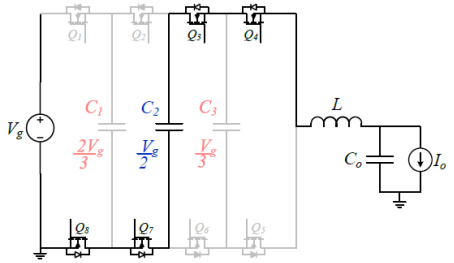
Depending on conditions, can be driven as a conventional 5-level converter producing 0, $V_g/4$, $2V_g/4$, $3V_g/4$, and V_g at the switching node and/or as a combination of a 3-level and 4-level converter producing additional two levels Vg/3 and 2Vg/3 => we can get 7 levels from a 5-level topology

[1] M. Halamicek, T. McRae, and A Prodić, "Asymmetric Voltage Splitting Modulation for Multi-Level FC Converters", to be presented at IEEE APEC 2019.

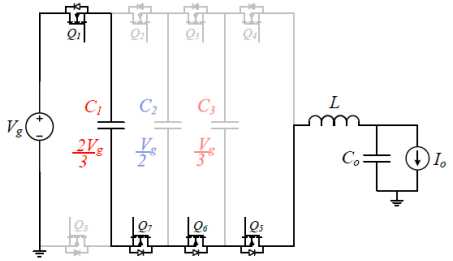
Control-Based Increase of the Effective Number of Levels for FC Converters (further L reduction)



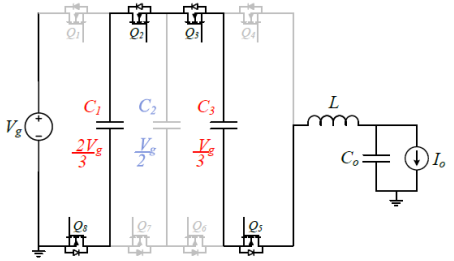
(a) MS_A



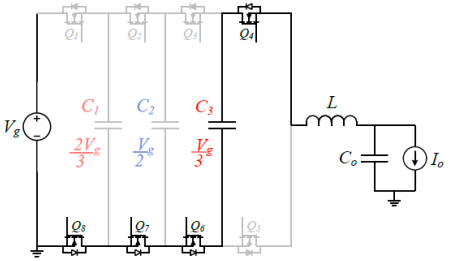
(b) MS_B



(c) SR_A



(d) SR_B



(e) SR_C

Example for 5-level structure operating with 0, Vg/3, Vg/2, 2Vg/3 and Vg levels. Can obtain automatic cap balancing.

[1] M. Halamicek, T. McRae, and A Prodić, "Asymmetric Voltage Splitting Modulation for Multi-Level FC Converters", to be presented at IEEE APEC 2019.

Control-Based Increase of the Effective Number of Levels for FC Converters (further L reduction)

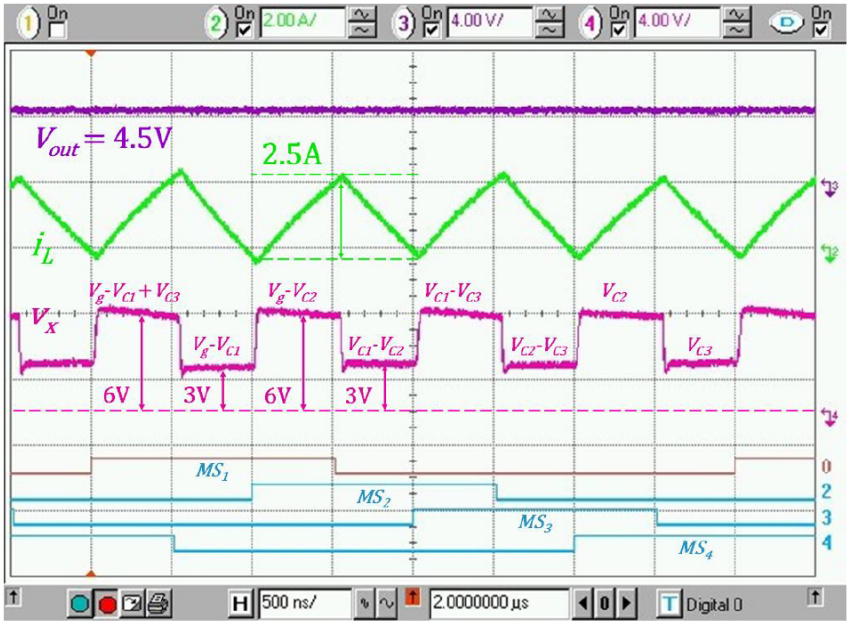


Fig. 6: Experimental waveforms of 5L-FC converter with conventional modulation.

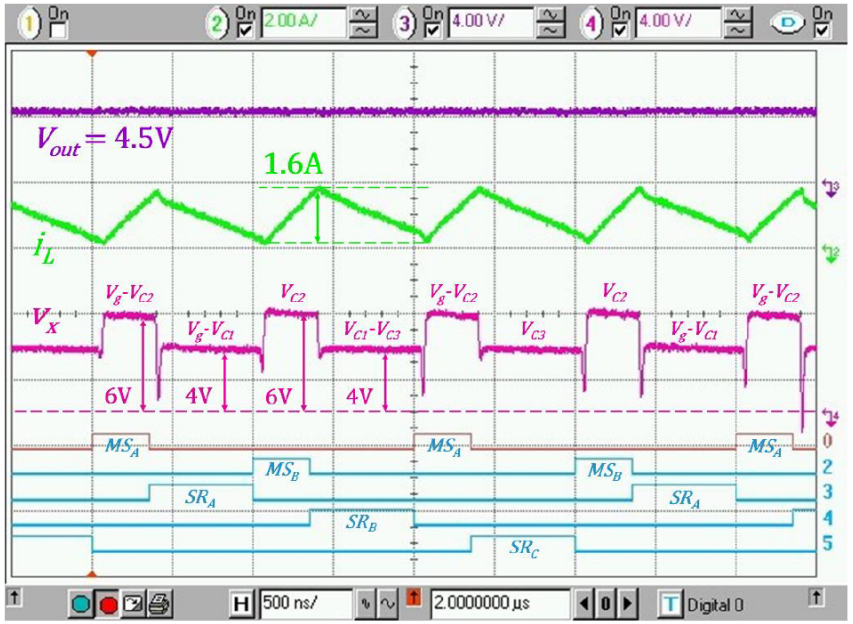


Fig. 7: Experimental waveforms of 5L-FC converter with asymmetric voltage splitting modulation.

Ripple (inductor) reduction – for a 5 level about a 40% smaller inductor

[1] M. Halamicek, T. McRae, and A Prodić, "Asymmetric Voltage Splitting Modulation for Multi-Level FC Converters", to be presented at IEEE APEC 2019.

Conclusions and Future Challenges

- *By utilizing reduced voltage and current swing principles new control and topological solutions can be found*
- *Single-mode minimum deviation controller provides virtually minimum voltage deviation resulting in the minimum size of output cap for direct energy transfer converters*
- *FC converter topologies bring advantages of lower size, improved efficiency (at the same time) with potentially lower cost of implementation, but also bring (solvable) challenges related to their control*
- *FC converters also open possibility for developing new control methods that could significantly improve their efficiency and further reduce the size*

Thank You.