Embedded Power Management for Automotive Microcontroller Units (MCUs) and its Challenges

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AGENDA

1. Infineon µC Automotive Applications
2. Power Managements: Evolution
3. Power Management: Present Development
4. Power Management: Challenges

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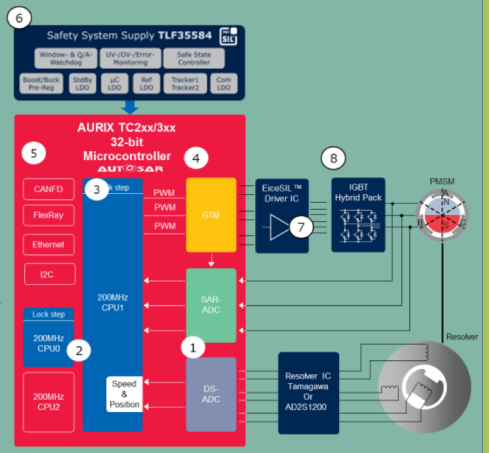
Infineon µC Automotive Applications

Strategy: Chassis, Safety and ADAS/ Connectivity

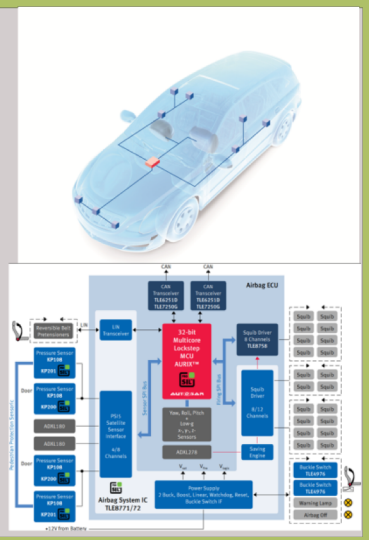
Hybrid Electric Vehicle (H)EV Inverter

1. ***DS-ADC (resolver)***
   Motor position sensing
2. ***Triple core***
   Real time app.
3. ***Safety, ISO26262***
   Lock step, IOM…
4. ***GTM timer***
   Motor control & tuning
5. ***CAN FD***
   Fast communication
6. ***Single voltage supply***
   Incl. safety features
7. ***EICE SIL driver:***
   Safety function
8. ***next IGBT module:***
   Efficiency ↓30%



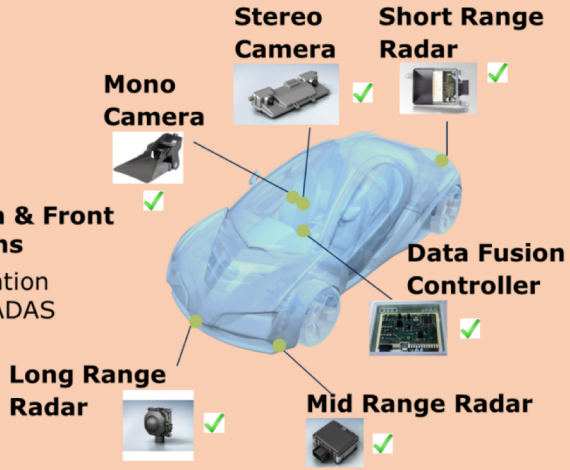
Airbag ECU Overview

- **Scope for µC:** central airbag ECU
- **Airbag tasks**:
  - **Evaluate** information from crash sensors and decide to trigger the squibs for bags, belts, pedals, battery, etc;
  - **Crash** data recording (LV37):
  - **Emergency** call
  - **Ensure** power supply during and short after an event (crash) is a key element of airbag applications



Advanced Driving-Assistance System; ADAS;

- **Radar, Data Fusion & Front Camera applications**
  - AURIX™ 2nd generation portfolio supports ADAS applications



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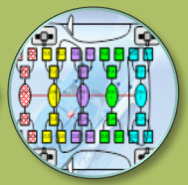
Infineon µC Automotive Applications

SoC **P**ower **M**anagement **S**ystem (**PMS**) constraints

Performance & Power Reduction		**PMS Performance** providing supply for up to 6 main cores
Scalability and Backward Compatibility		**PMS Concepts** supporting backward compatibility (HW/SW reuse)
Functional Safety		**PMS Concepts** following **ISO26262** standard, enabling **ASIL-D** level
Security		**PMS Concepts** supporting security functions,
Networking		**PMS supporting** peripherals to address the growing demands of **in-vehicle networking**

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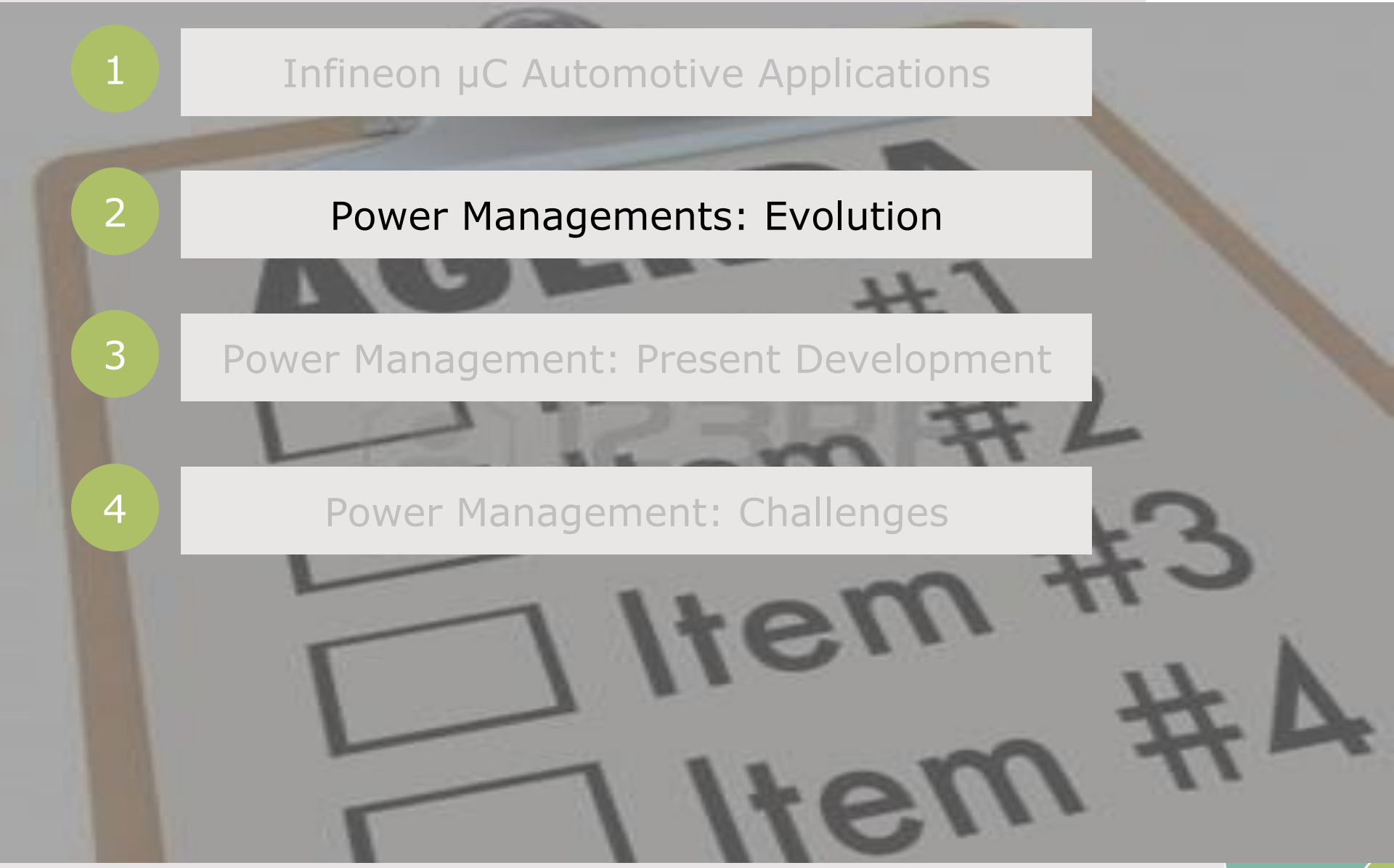

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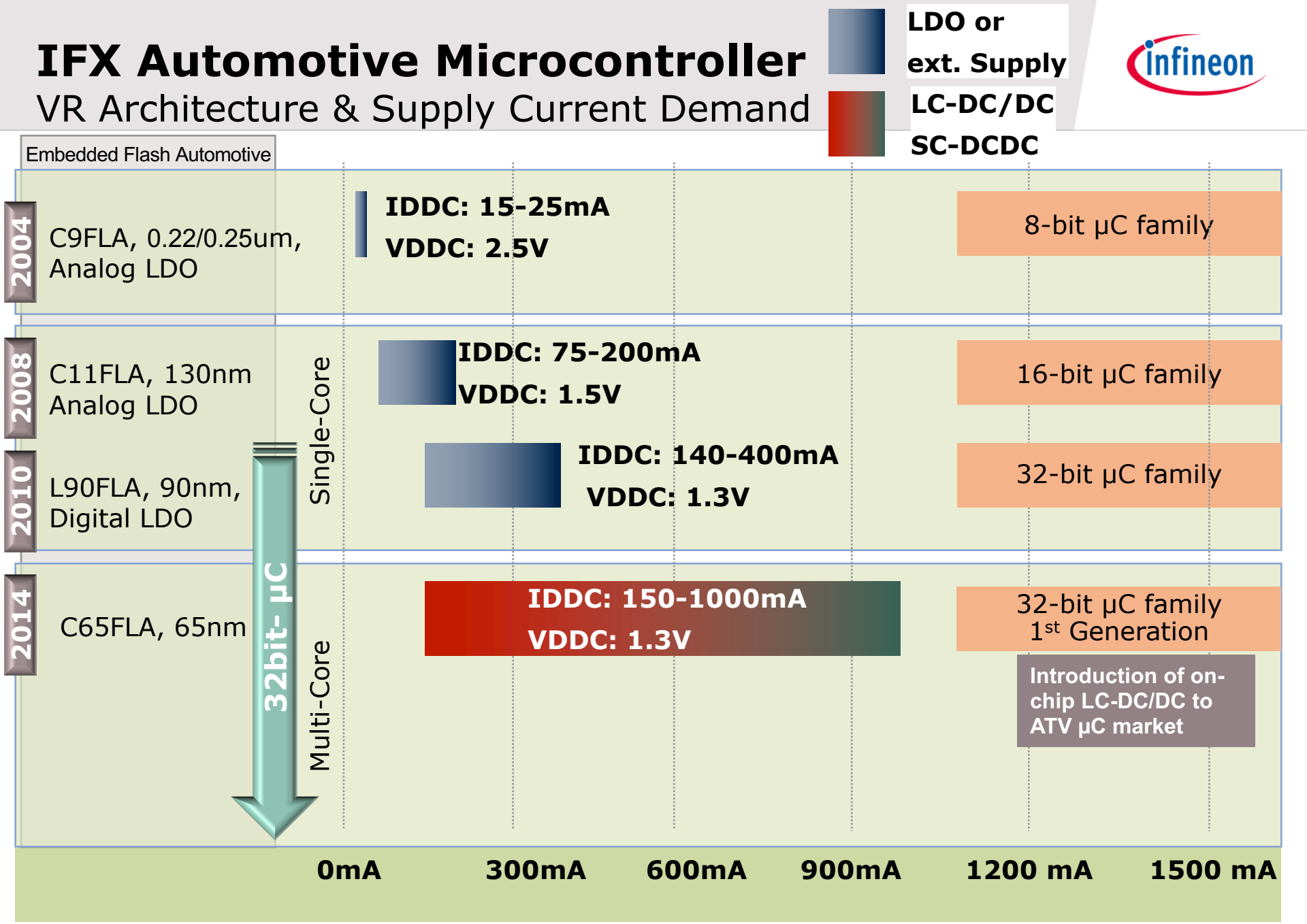
IFX Automotive Microcontroller

VR Architecture & Supply Current Demand



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IFX Automotive Microcontroller

PMS-CE to make µC ready for on-chip DCDC (LC & SC)

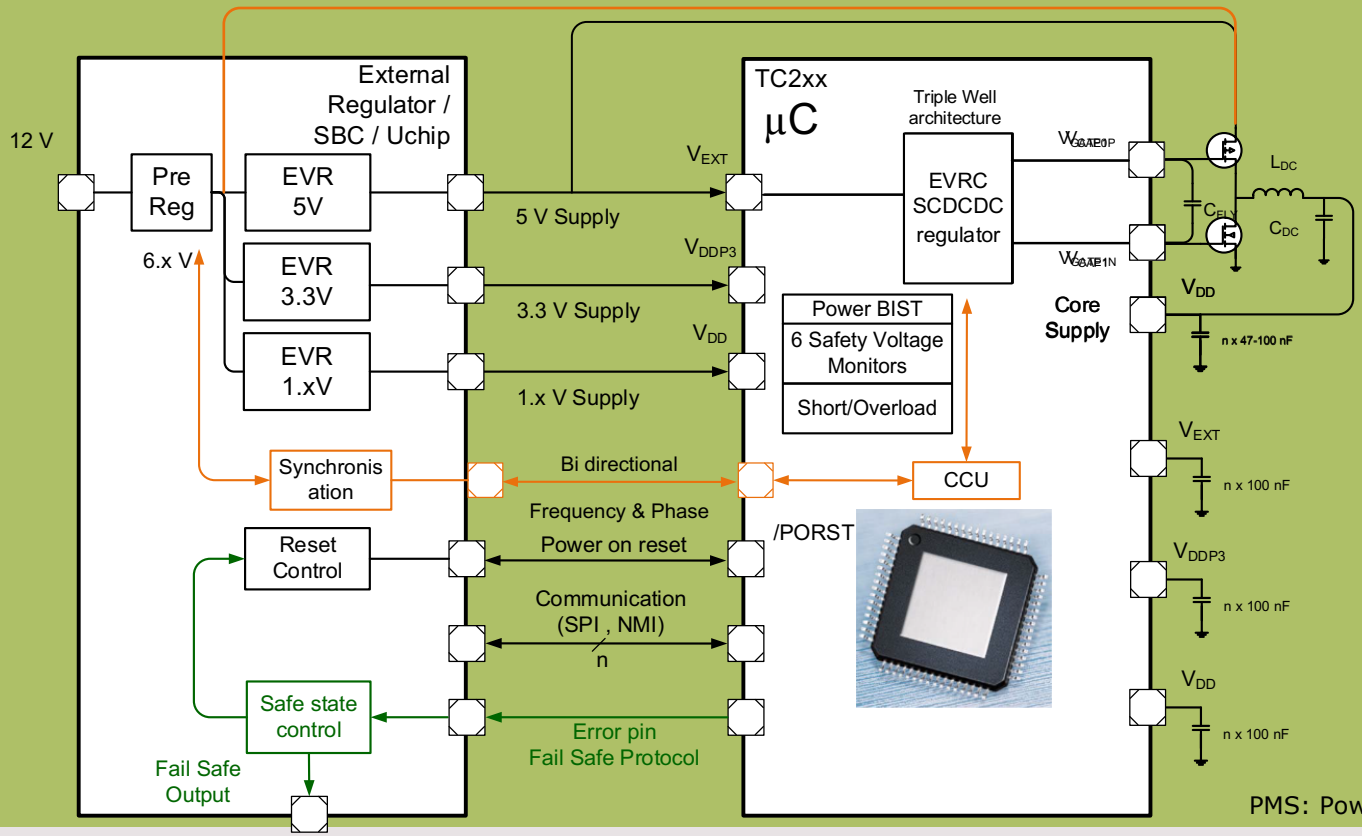
1. Triple supply to Single Supply with integrated DCDC regulators devoid of power sequencing

- ~ 50 % reduction of power supply pins and E-pad introduction

2. Safety compliant architecture : Error pin, Bi-directional reset and power fail, Power BIST, 6 Independent monitors..

3. DCDC Synchronization, Direct Pre-regulator drive

- Switch capacitor distributed regulators for LE devices



PMS: Power Management System

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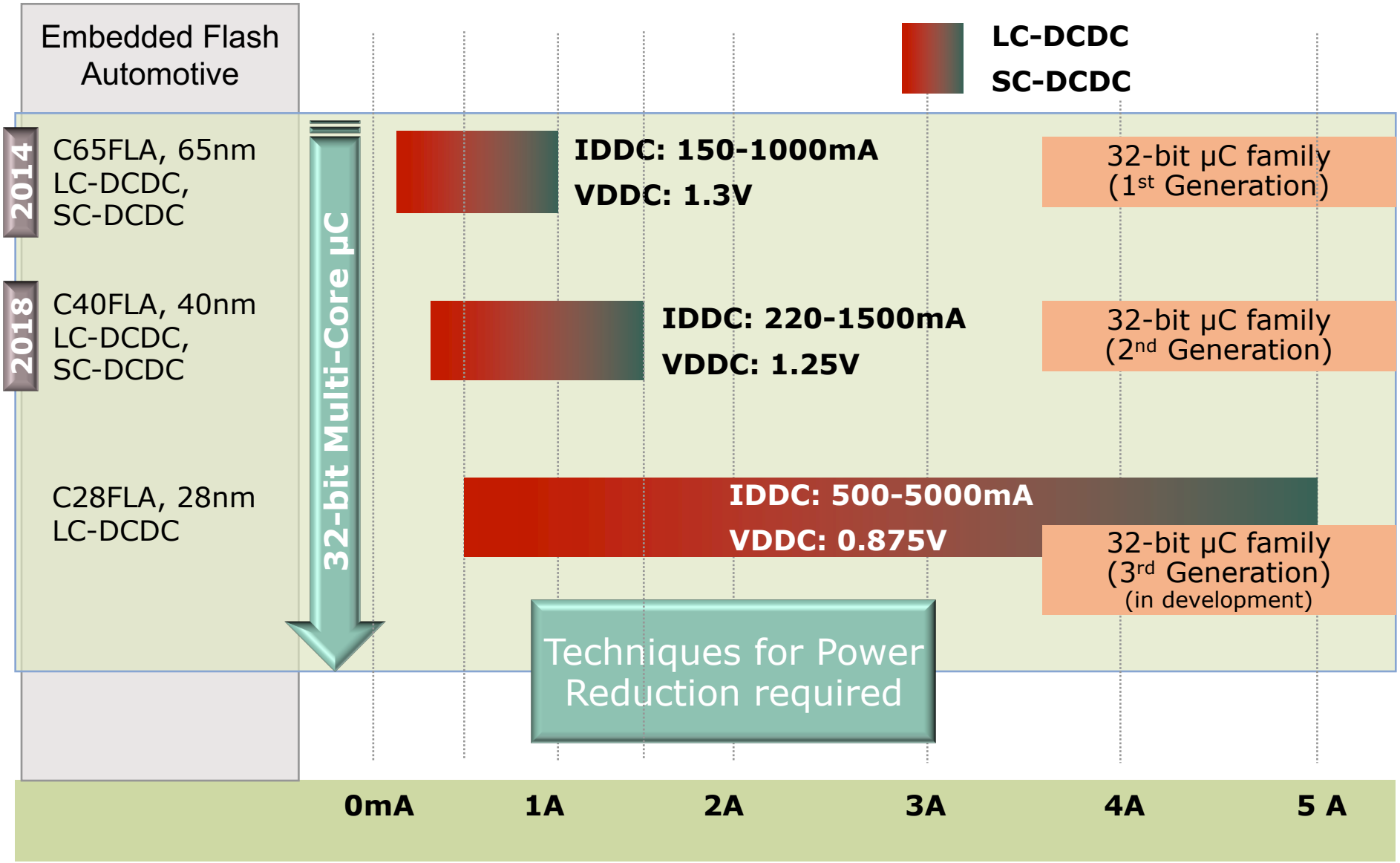
IFX Automotive Microcontroller

Supply Current Demand



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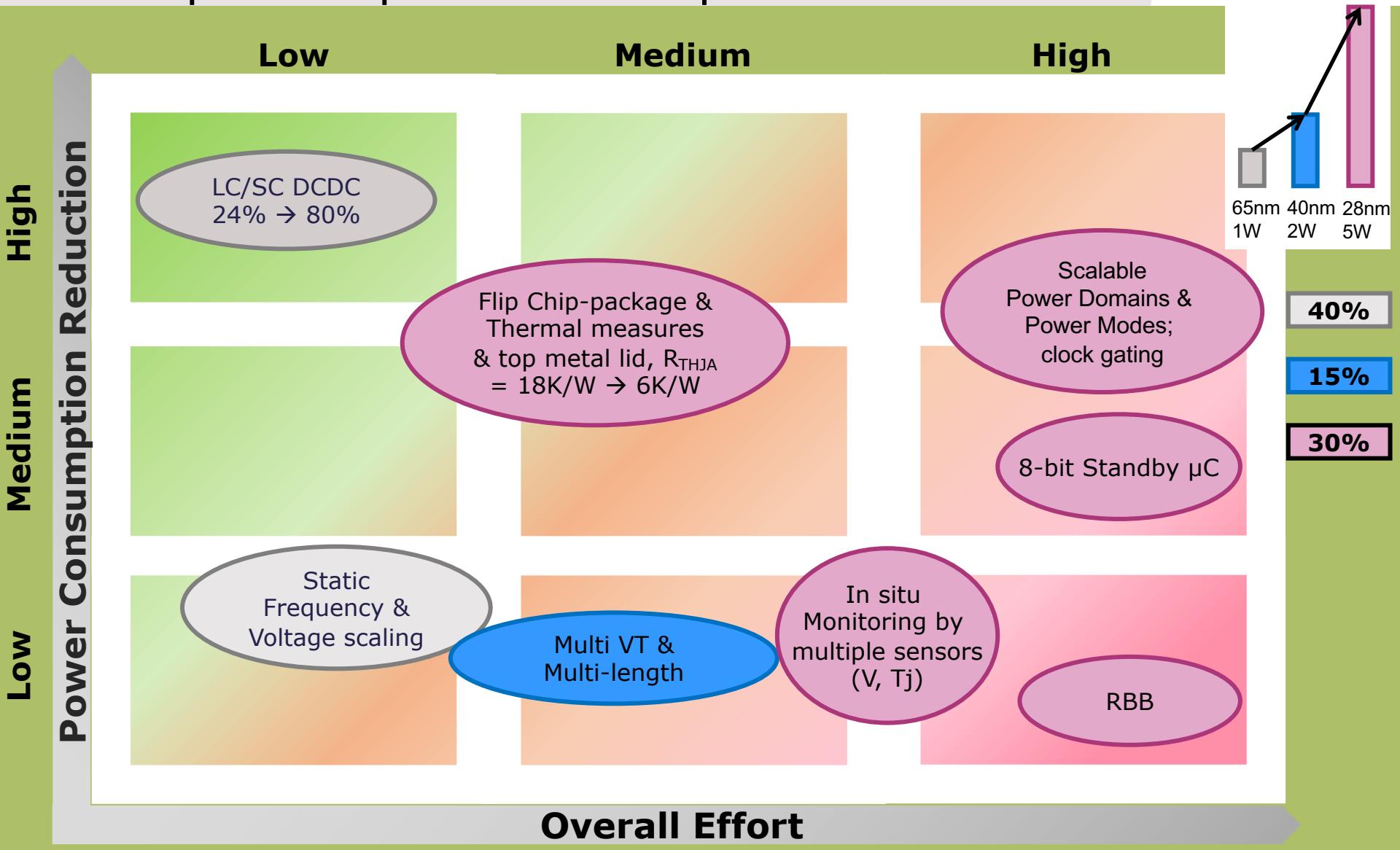
IFX Automotive Microcontroller

Techniques for power & Vdrop reduction



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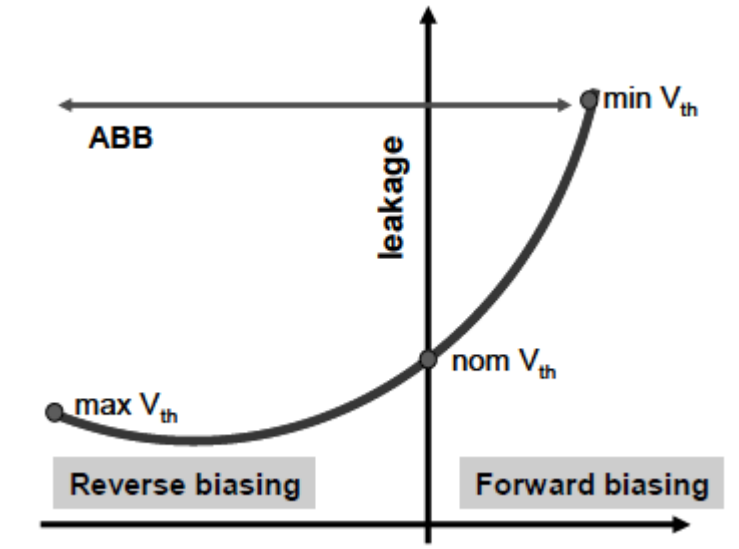
IFX Automotive Microcontroller
Development of Body Bias Test Chip, I

Transistor Body Biasing

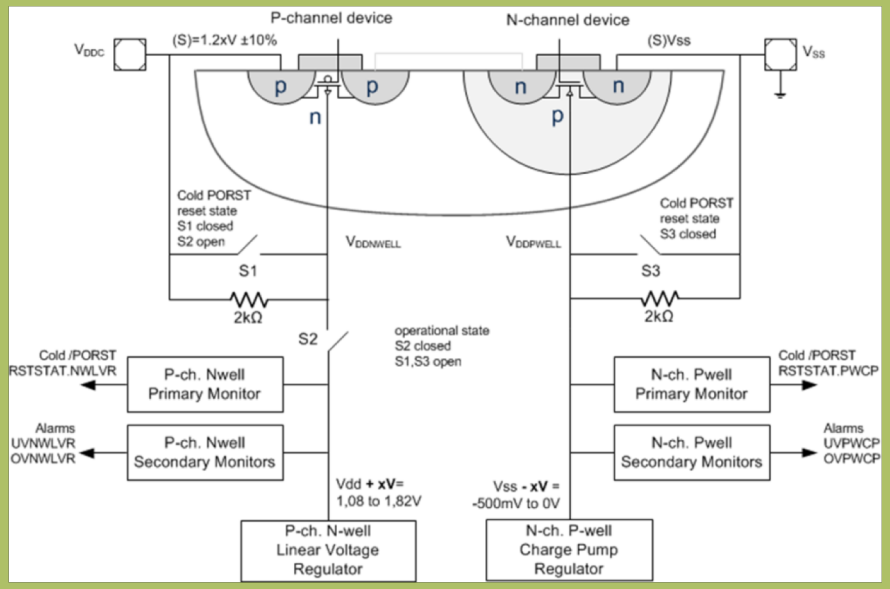
- **Investigations** for power consumption reduction by Body Bias
- **Transistor Body Bias (BB)** can be applied to adopt the threshold voltage of MOS devices



Adaptive **V**oltage **S**caling (**AVS**)
Adaptive **B**ody **B**ias (**ABB**)

Test Chip: PMS, 40nm

- **N-well:** Linear Voltage Regulator (LVR)
- **P-well:** neg. charge pump (CP) + LVR
- **Critical** path monitoring (DUT), stop clock and scan-out in case of error



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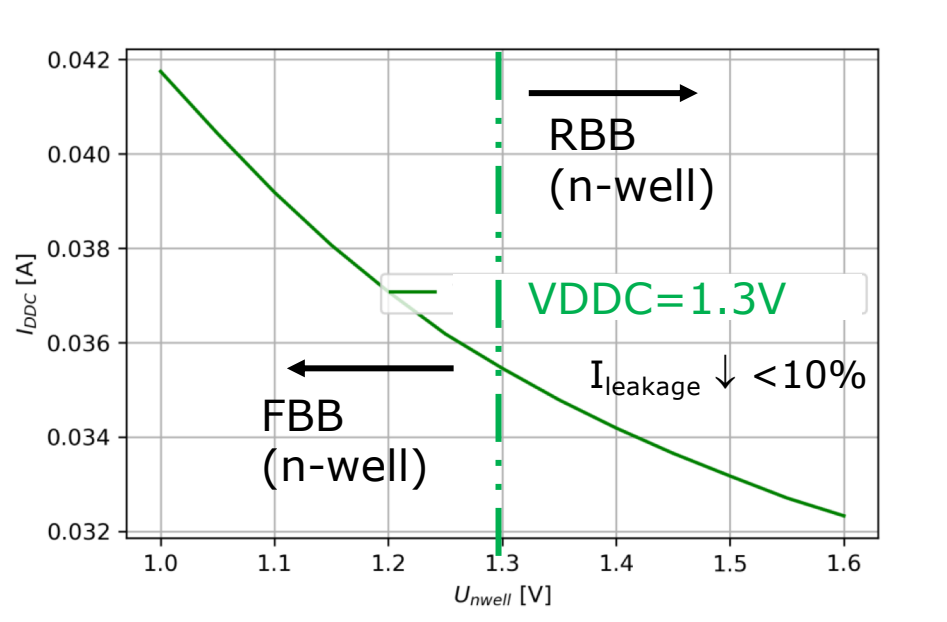
IFX Automotive Microcontroller
Development of Body Bias Test Chip, II

Test Chip: Results

- **P-well=-300mV by Charge Pump**
- **Tj=85°C**
- **Corner process (NfPf)**



RBB Side Effects

- **Timing Sign off**
  - Increased Jitter, clock domain crossing (w/ & wo RBB)
- **Area penalty**
  - 0.4-1.0 mm^2
- **EMC**
  - Emission↑ as Cap_{filler} ↓
- **Functional Safety**
  - E.g. complexity↑ due to well-Voltage Monitoring
- **Production Test**
  - complexity↑, test time↑
- **Latch Up Robustness**
  - E.g. parasitic bipolar effects

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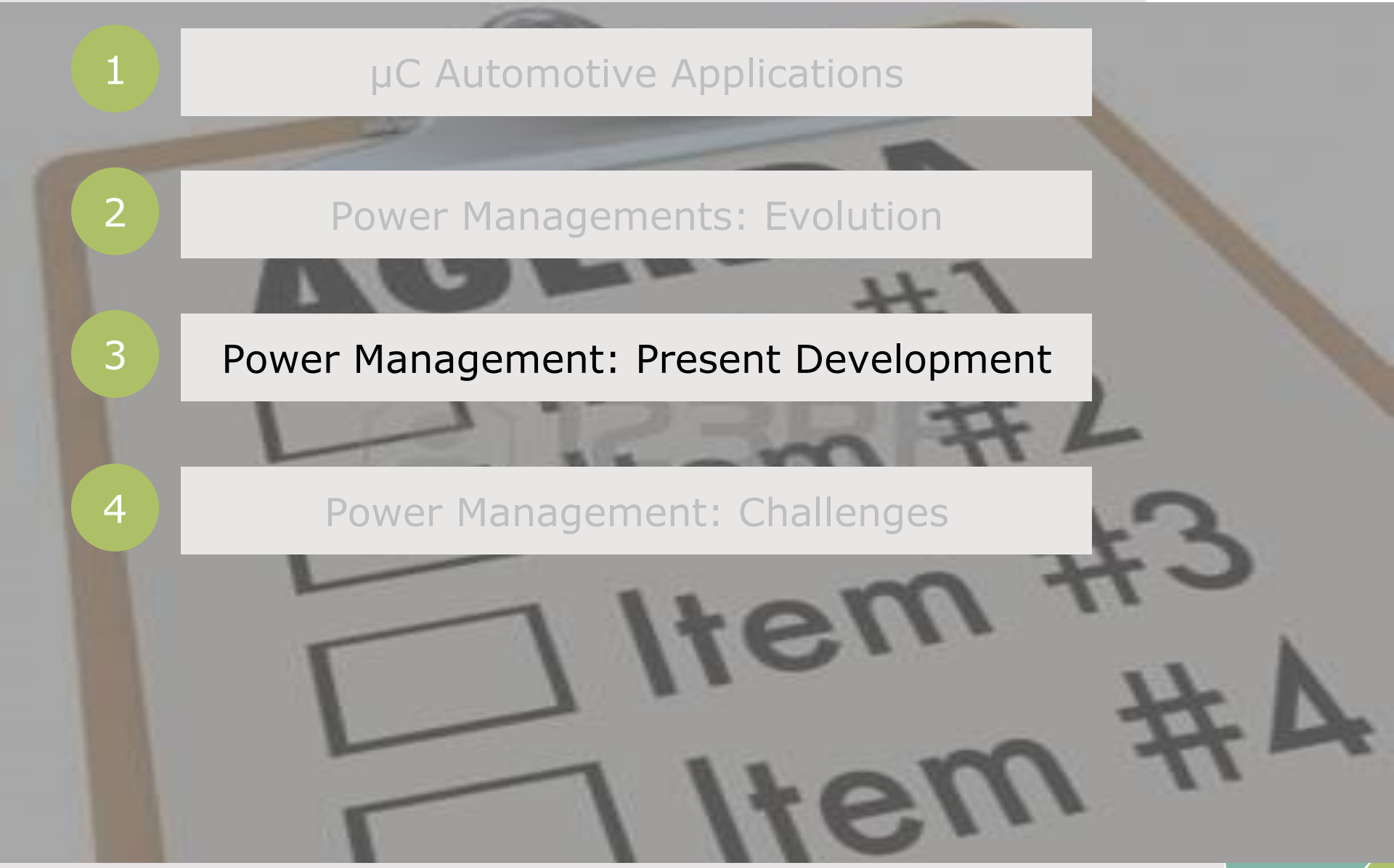

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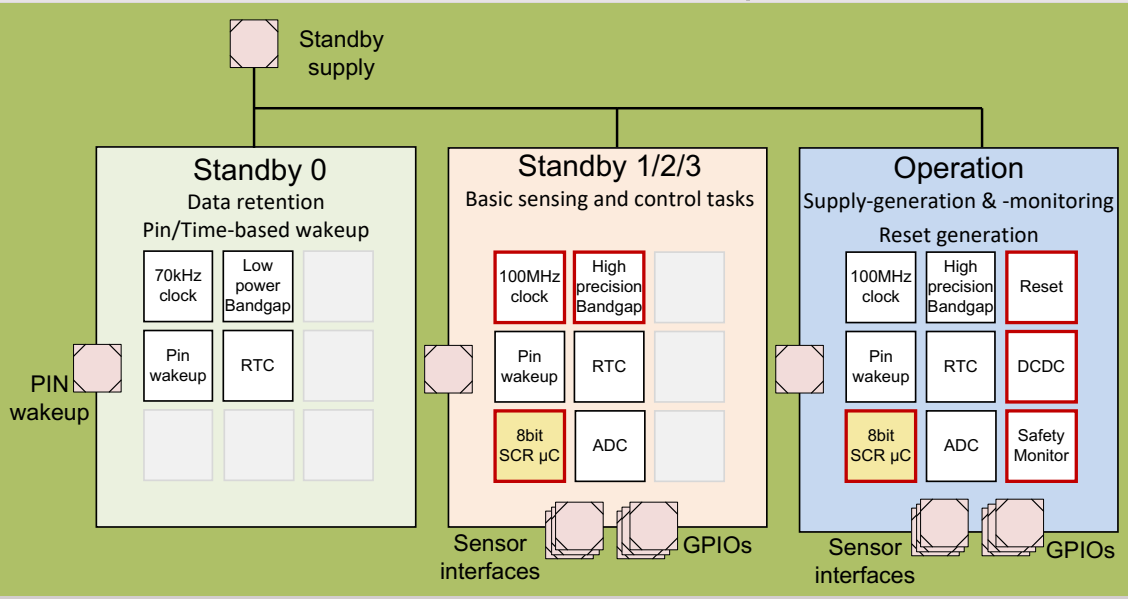
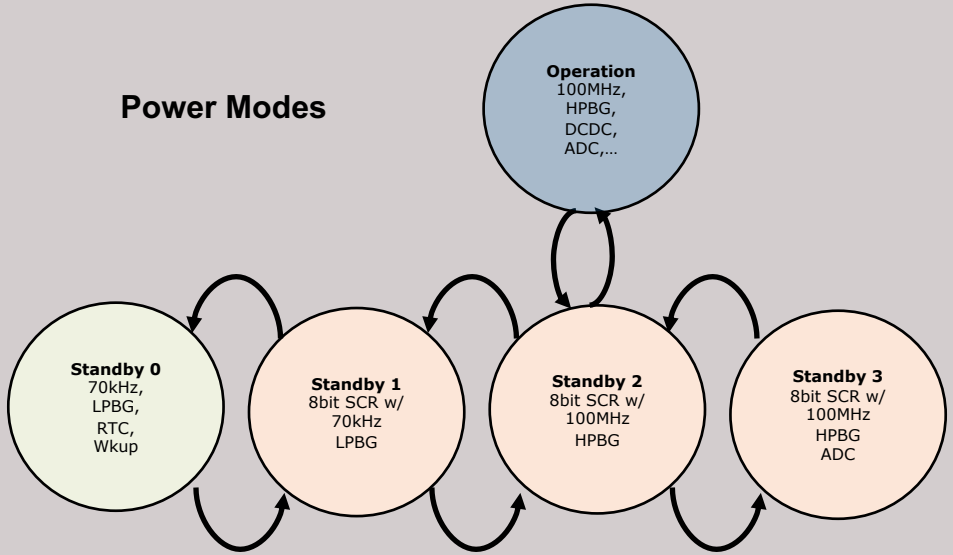
Power Management: Present Development

Scalable Power Domains & Power Modes;





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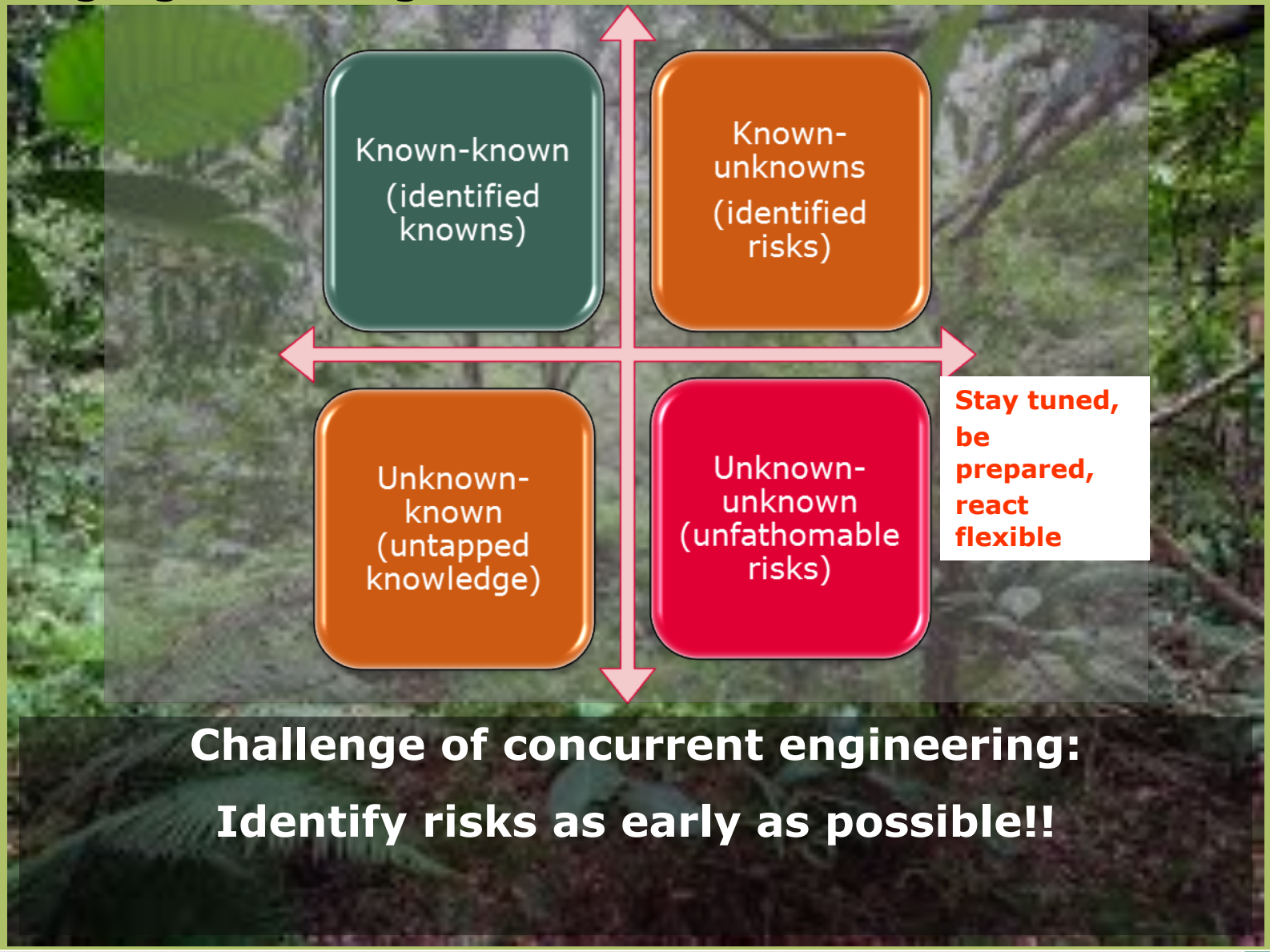
Power Management
Managing Challenges



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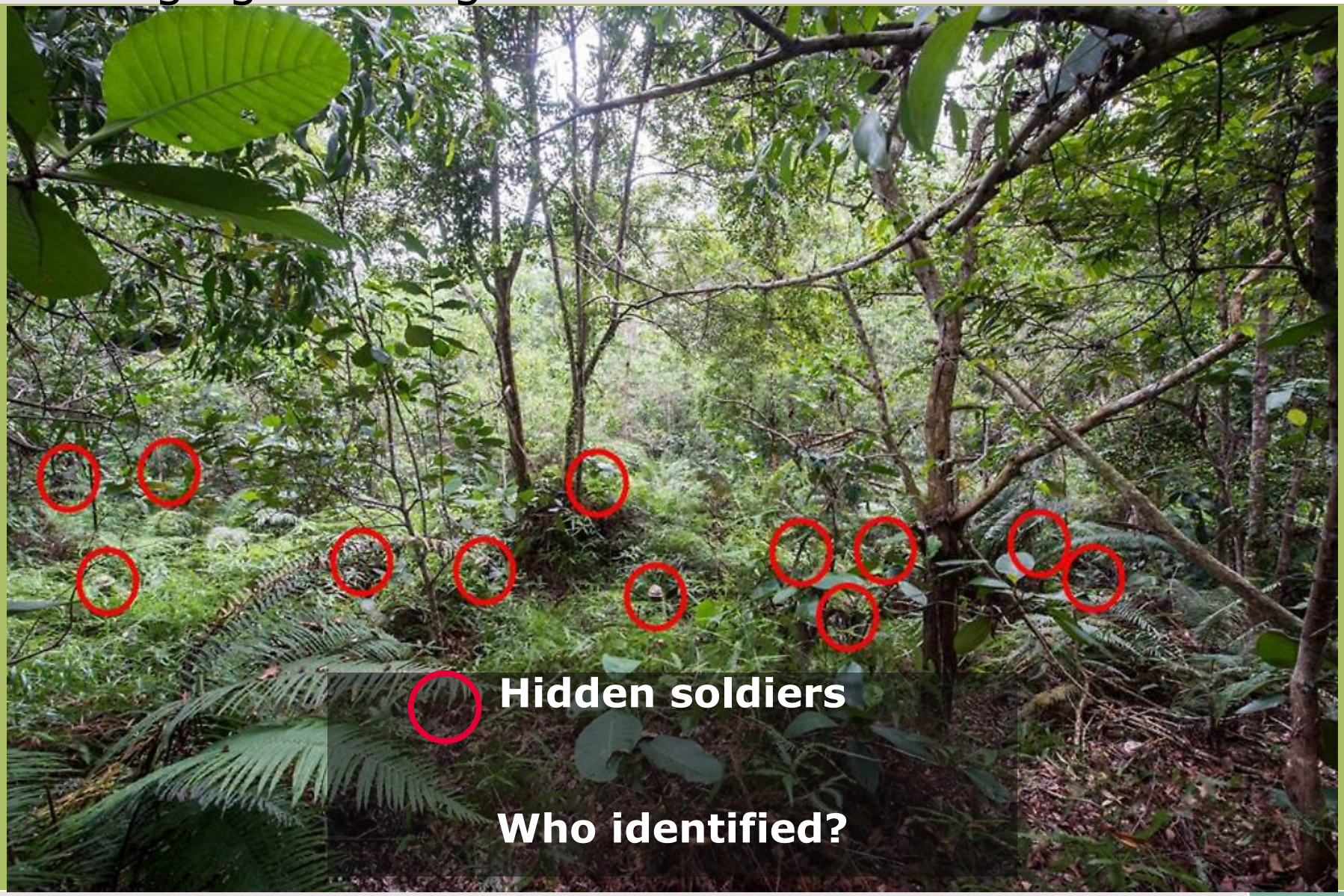
Power Management
Managing Challenges



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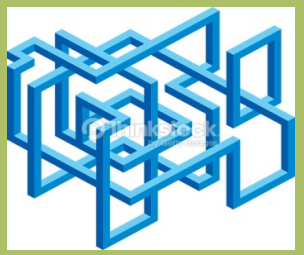
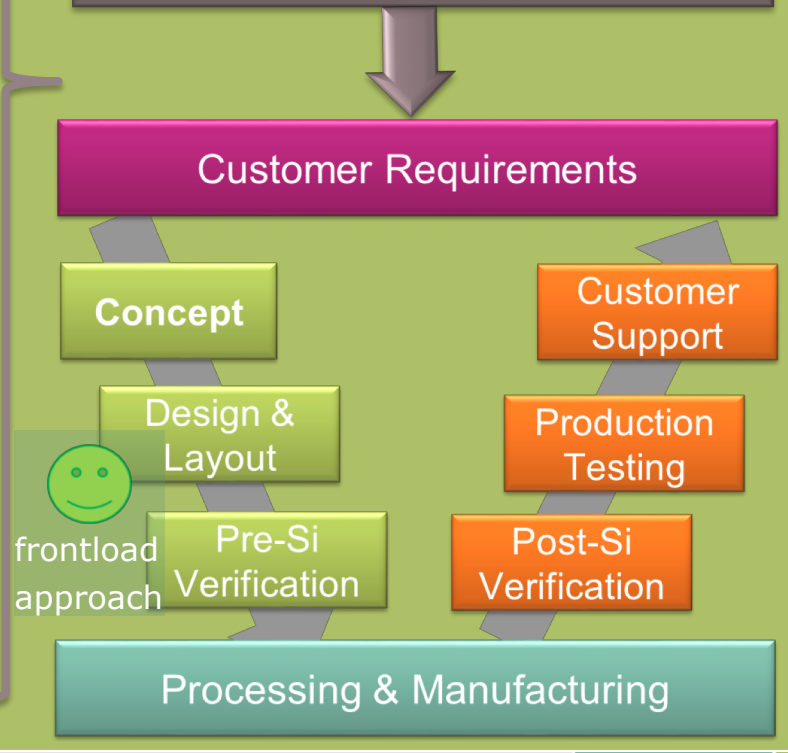
Power Management
Managing Concurrent Engineering

	Challenge	What
	New Technology	▪ Leakage ? ▪ Matching? ▪ Drift effects? ▪ EOS ▪ …
	Design Complexity & Robustness	▪ Efficiency, Resolution ▪ New applications ▪ Cross Functional System (ana, dig) ▪ …
	Business Case, Time to market	▪ Test time ↓ ▪ Si area ↓ ▪ Zero defect ▪ Dev. Cycle time ▪ …
	Physical Integration & XTALK	▪ Power Integrity ▪ Signal Integrity ▪ PDN ▪ Packaging ▪ …

How

- **Continuously** spy for technical risks and provide solutions in time (frontloading approach)
  - Pre-development (e.g. Uni cooperation)
  - New methodologies



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To the Technical Leads out there…
Avoid problems in the project , else…

Customer	Delivery delayed	
Management	Business Case drops	
Colleagues & Team	Focus Team or Task Force	

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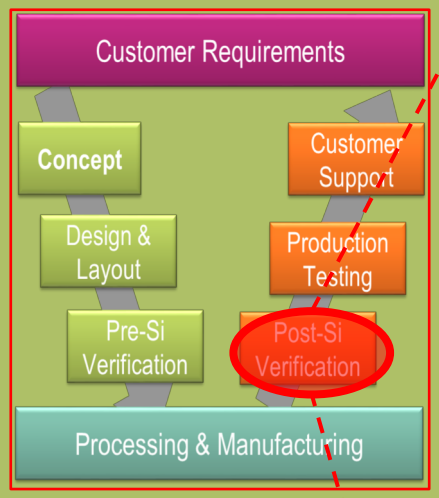
Ex. 1) Power- & Signal Integrity (PI-SI)

XTALK issue: LC-DCDC impact on SAR ADC channels

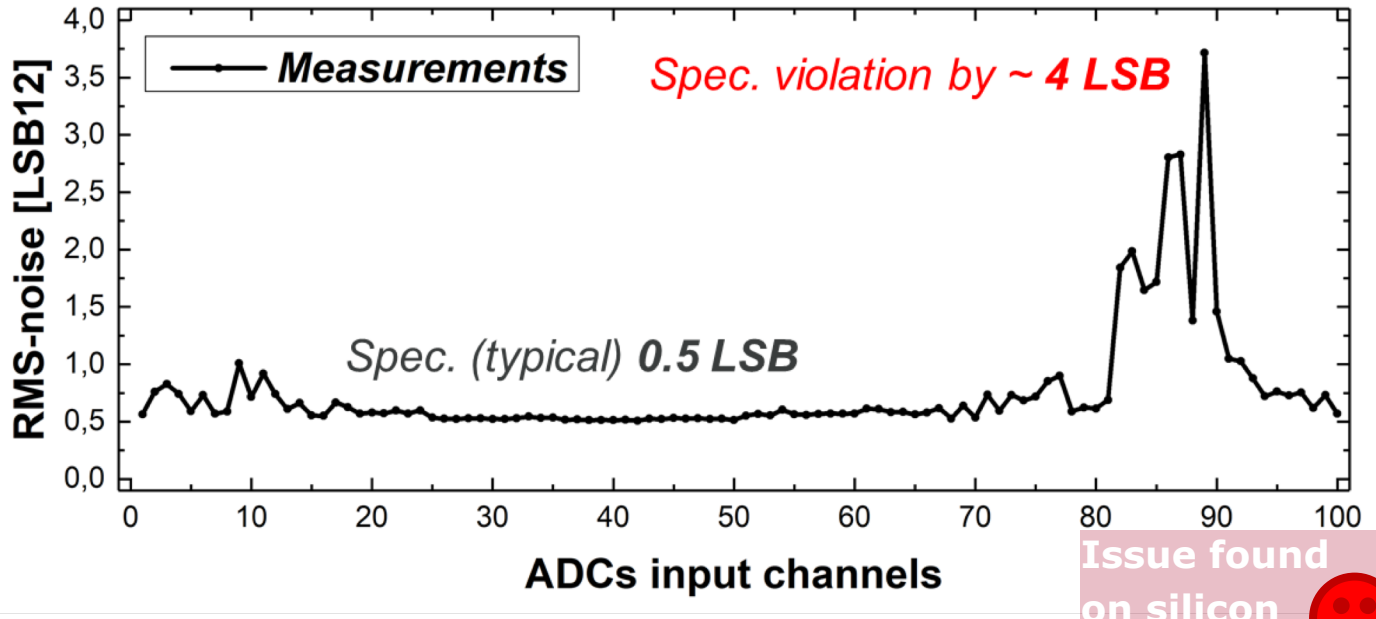
V-Model



Aggressor: DC/DC step down (buck)

Victim: Input channels of 12 bit **SAR ADCs**

Those ADCs experience crosstalk due to inductive coupling at package-level due to large di/dt of DC/DC gate drivers



Issue found on silicon

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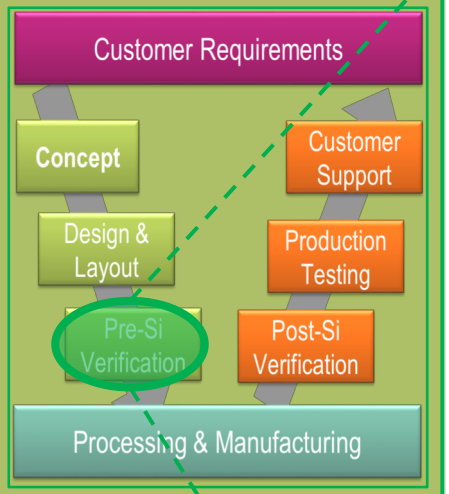
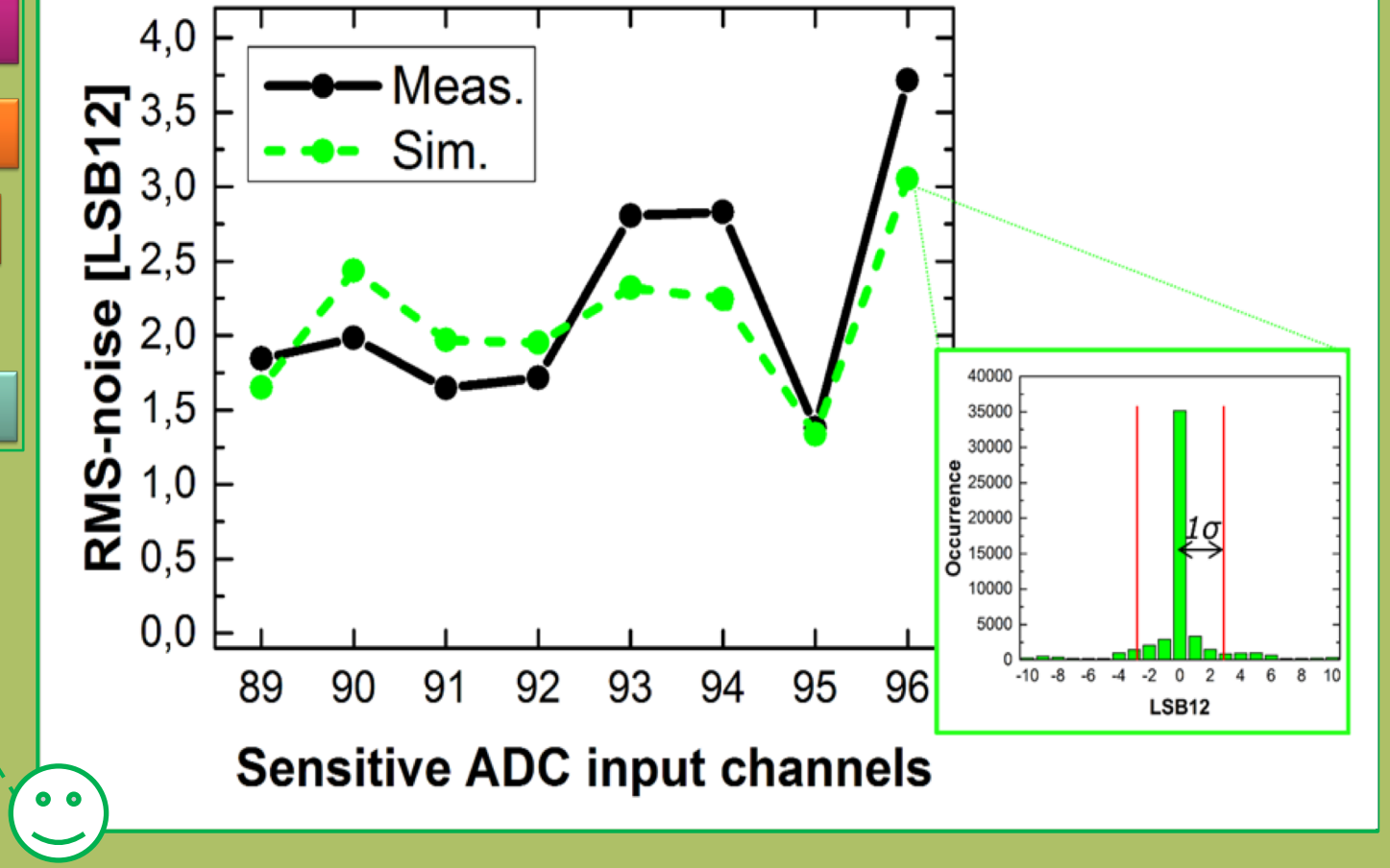
Ex. 1) Power- & Signal Integrity (PI-SI)

Dev. Methodology to handle XTALK effects (PCB)

V-Model





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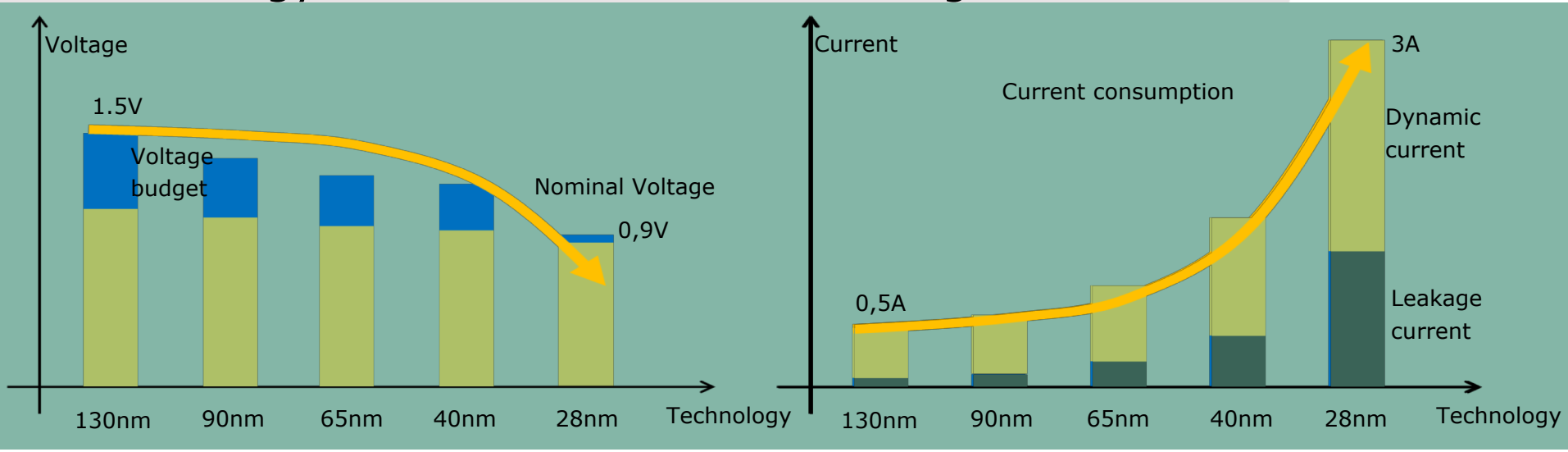
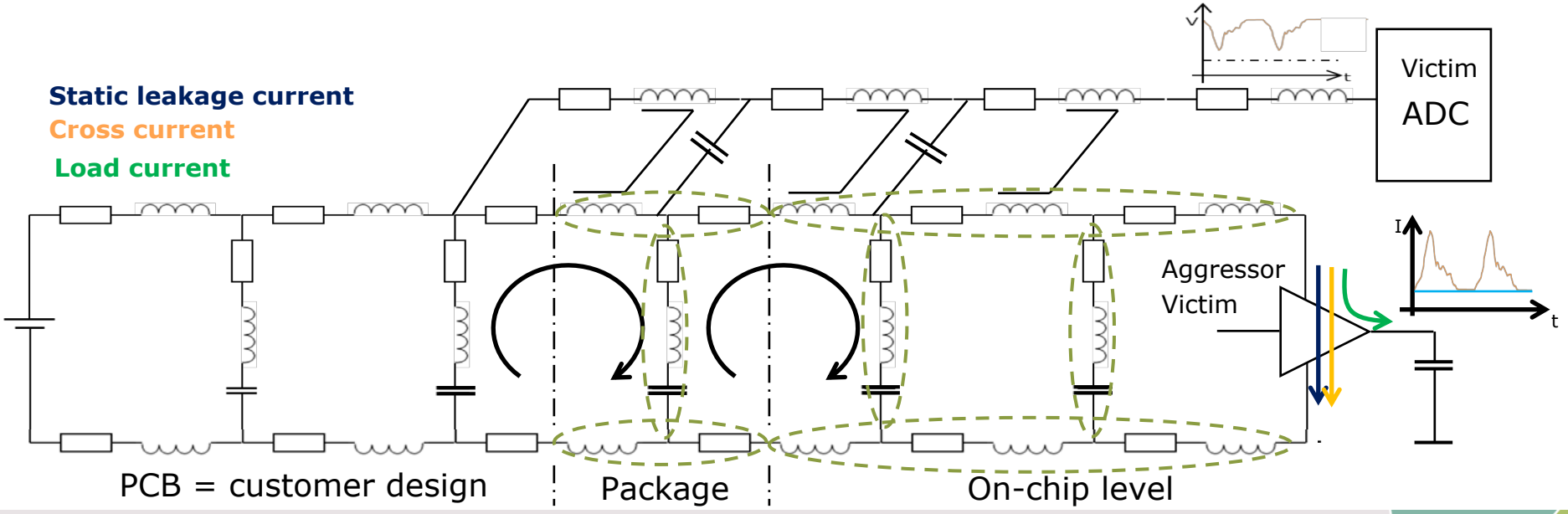
Ex. 2) Power Distribution Network

Methodology to ensure efficient PDN design





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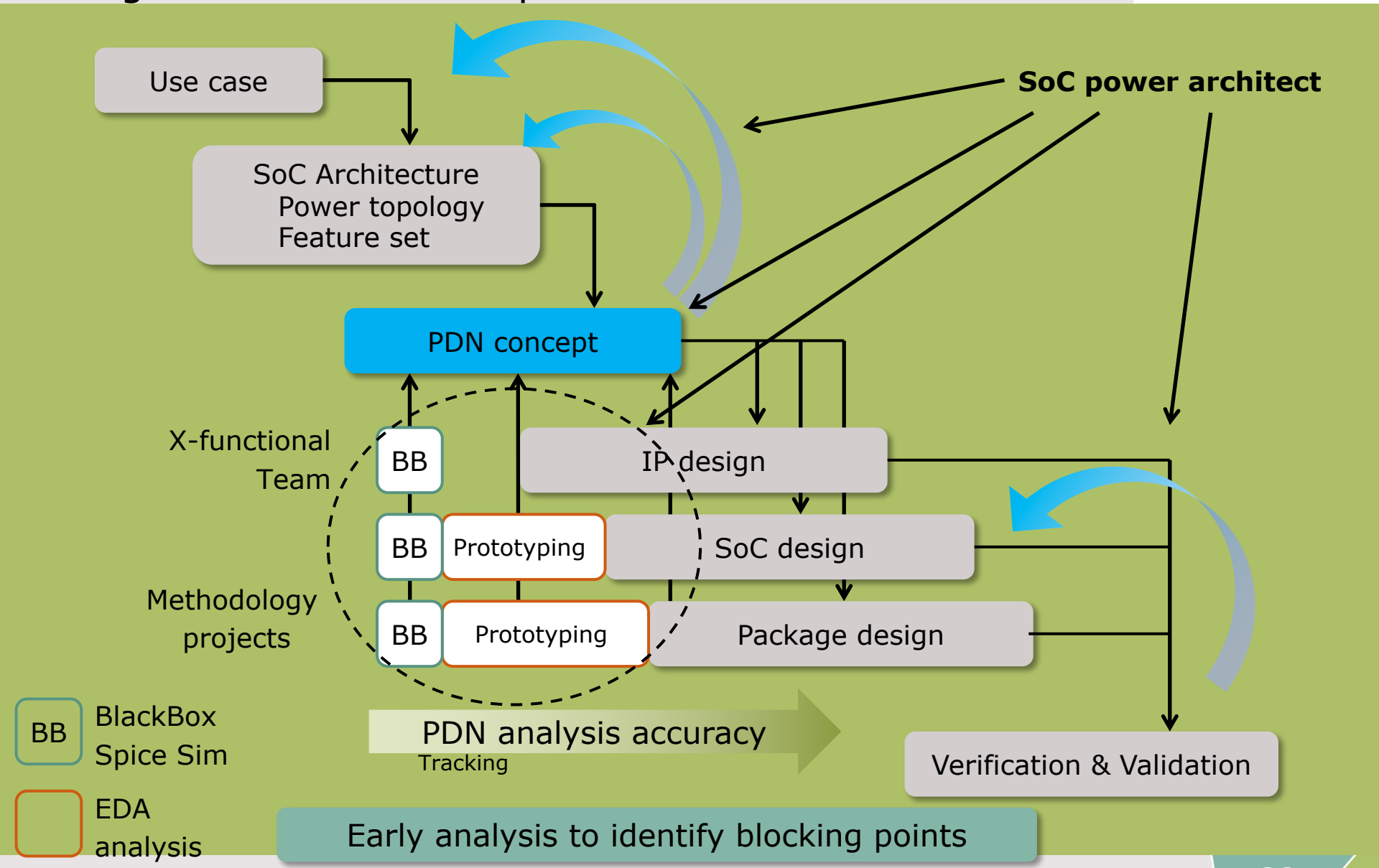
Ex. 2) Power Distribution Network

Design flow: Concurrent process



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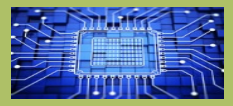
Ex. 3) Robustness Verification

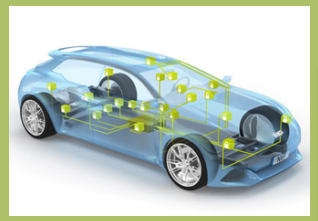
Provoke field returns artificially



Technology

- Physical failure mechanisms
- Aging
- Split dependency

Strategy document



Application

- Power Pattern
- Aggressors
- WC Scenarios
- Mission Profiles

Mixed Signal System on SoC

- Physical implementation
- Design Sensitivity Matrices
- Design constraints

Design

Investigate on:

- Design Parameter Margins
- Performance under system conditions
- Risks of FAR's

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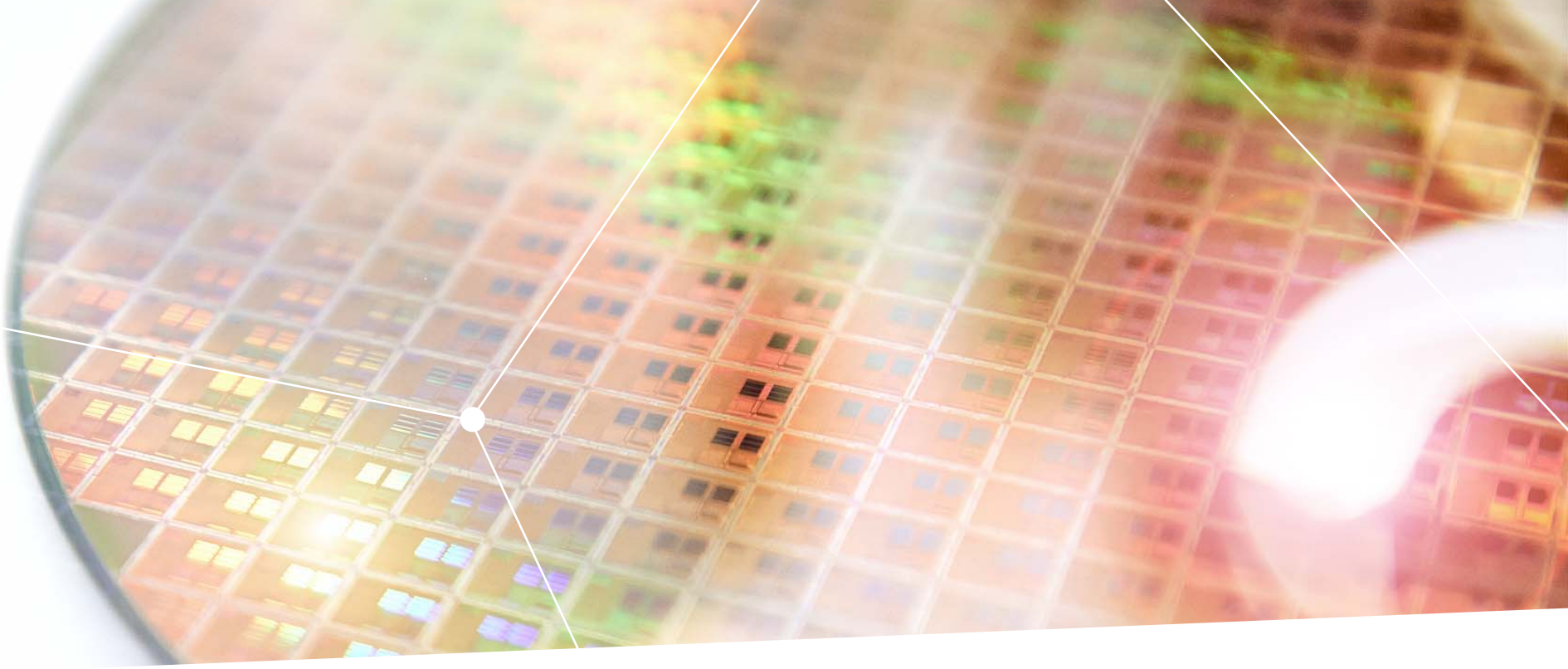

Many Thanks for your attention

Questions?

Backup

Part of your life. Part of tomorrow.

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