



ASE GROUP

# New Generation Power Packaging Technology

## IC Embedded Substrate Solution for Advanced Package/SiP

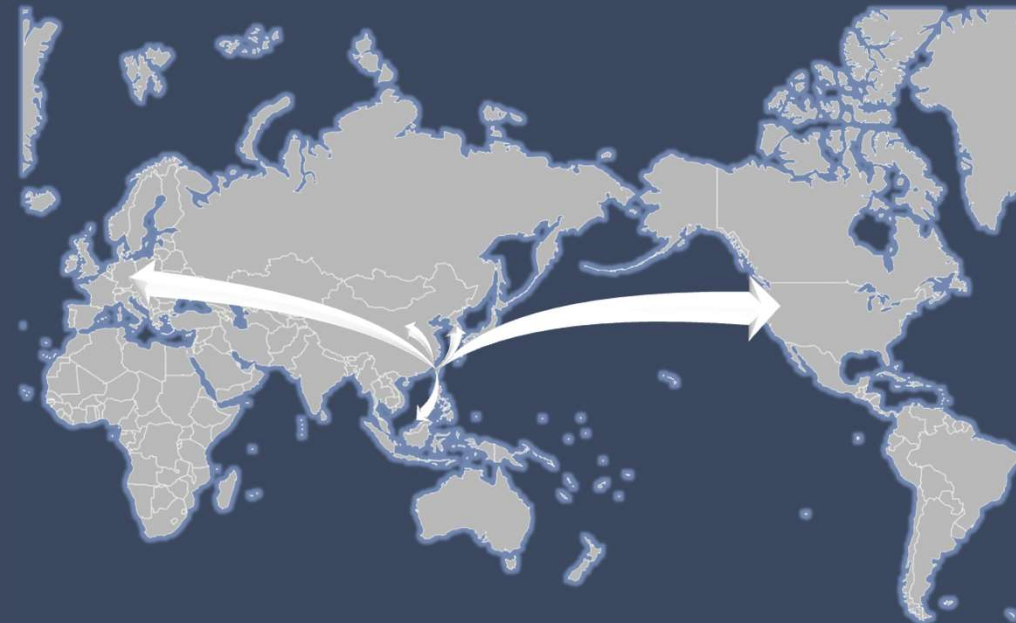
Presented by : Chien-Fan Chen

2018/10/17



# Content

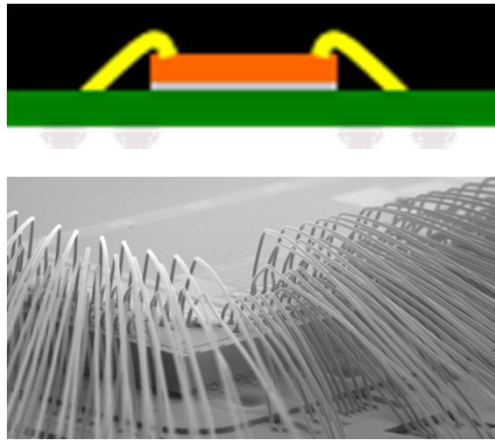
- **Interconnect Evolution**
- **ASE Embedded Solutions & Applications**
- **Future Trend & Demand**
- **Summary**



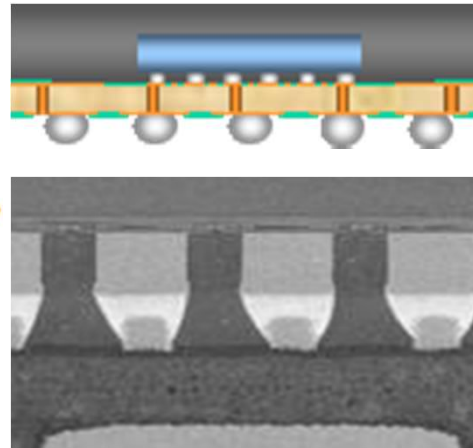
# • Interconnect Evolution



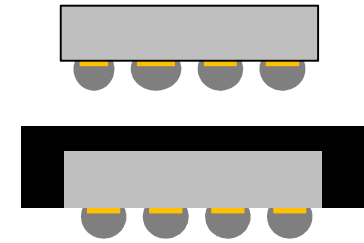
# Interconnect Evolution



Wire Bond

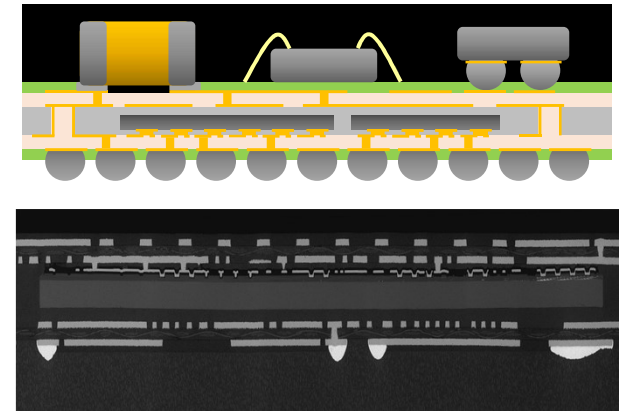


Flip Chip



Wafer Level CSP &  
Wafer Level Fan out

## Cu Interconnection



Embedding Chip

- Embedding chip into substrate, and electrical contacts to the embedded chips by drilled & metalized vias.
- By mounting passives and packages on such substrate to form a SiP Module.

# Benefits of Embedded Solution

## Miniaturization & Design Flexibility

- Embedded chip enables more space for other components or shrinks overall solution
- Design flexibility now shifts from 2D to 3D

## Improved Thermal & Electrical Thermal Performance

- Shorter interconnections reduce parasitics - minimizes distortion and power loss
- Lower electrical & thermal resistivity in package improves power performance

## Improved Reliability and Mechanical Stability

- High mechanical system stability due to stable Cu interconnections.

# Main Drivers of Embedded SiP Module

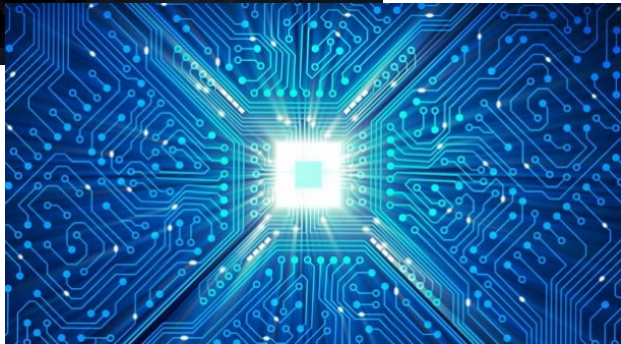


**Miniaturization**

**Enhanced Performance**

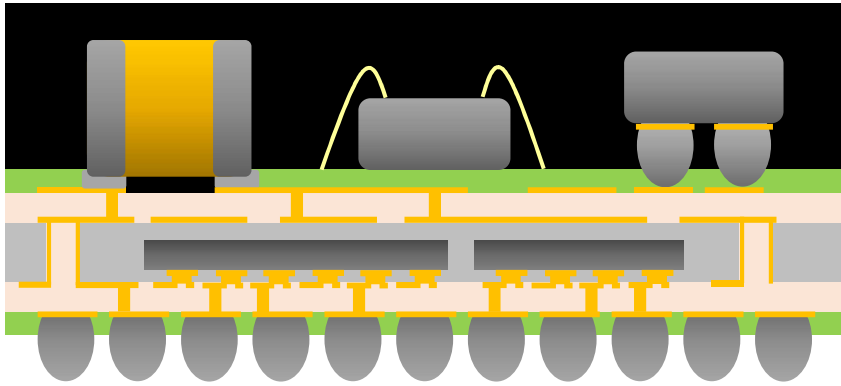


**High Integration**



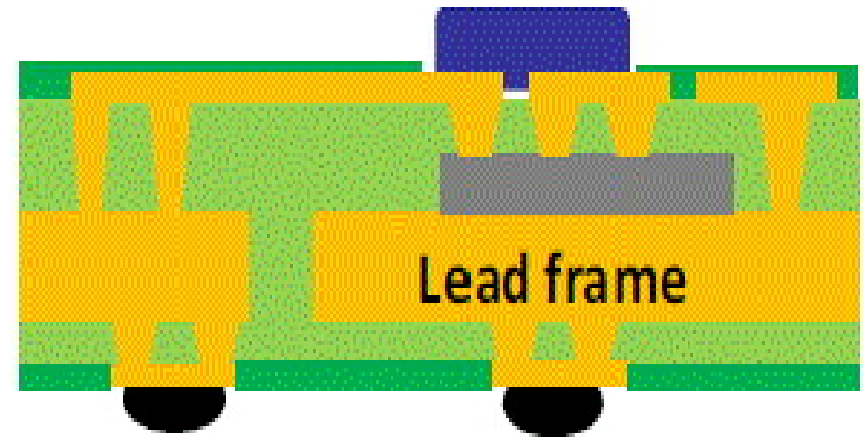
- **ASE Embedded Solutions & Applications**





# SESUB

**S**emiconductor **E**MBEDDED IN **SUB**strate



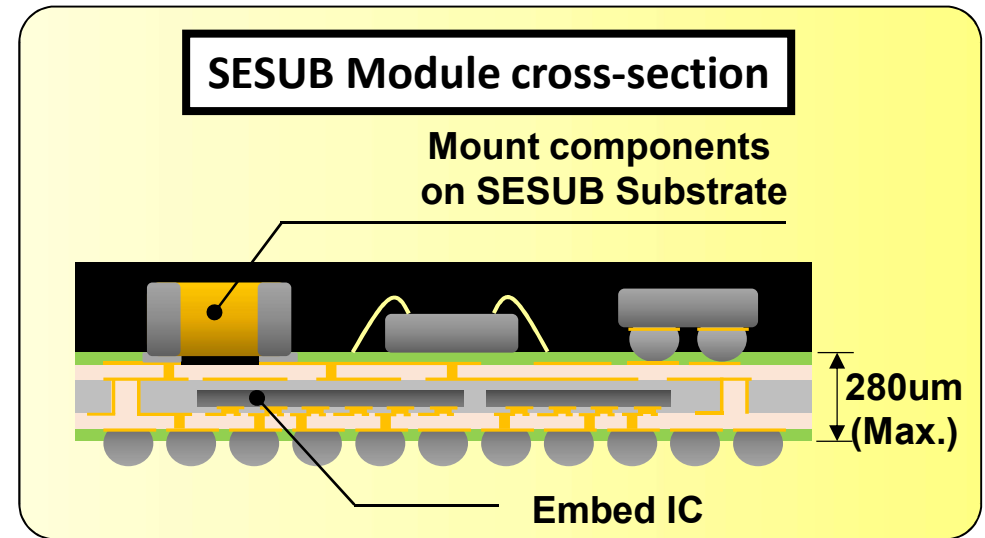
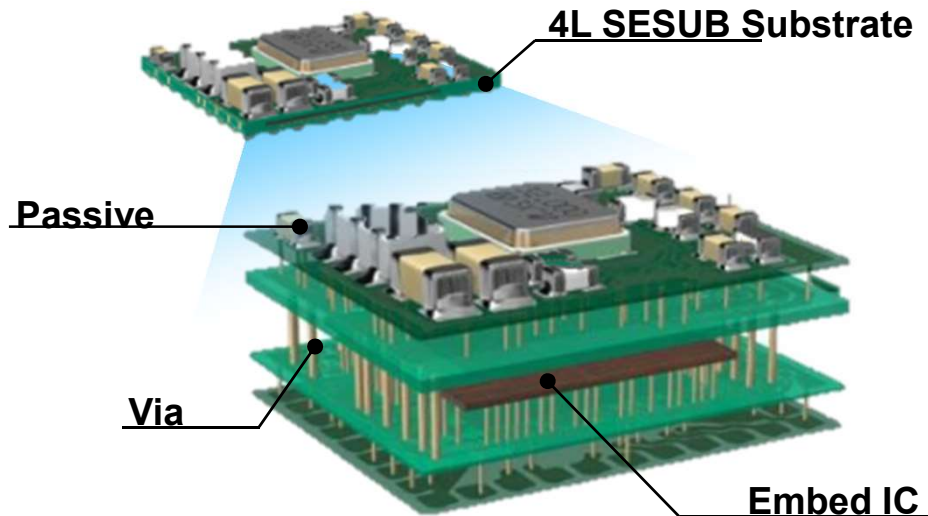
# a-EASI

**A**dvanced **E**MBEDDED **A**ctive **S**ystem **I**ntegration

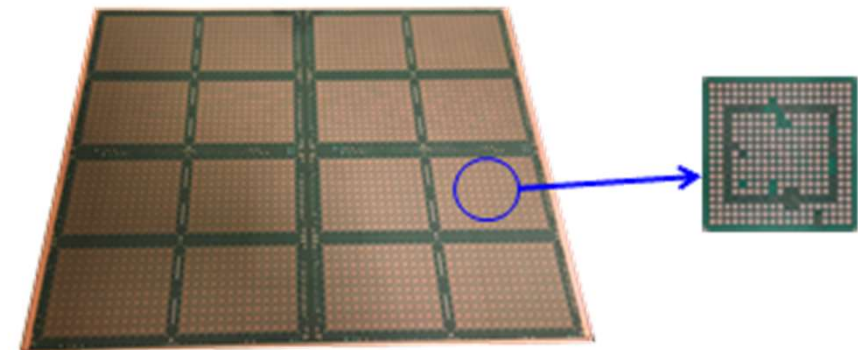


# What's *SESUB* ?

**SESUB** = Semiconductor Embedded in SUBstrate



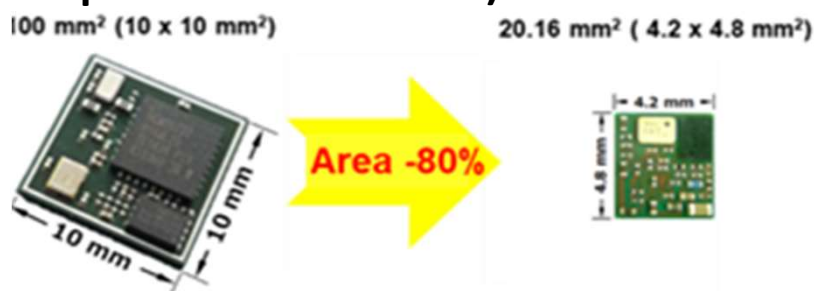
- SESUB technology had been proven a mature technology
- Transferred SESUB technology from TDK and production in a panel form of  $512 \times 408 \text{ mm}^2$  (2X) with cost benefit
- IC wafer grinded to  $50\mu\text{m}$  (min.) and embedding in resin substrate
- Thickness normally 4L  $250\mu\text{m}$  (Max.  $280\mu\text{m}$ )
- Multiple dies (Max. 4 to date) could be embedded



# Embedded SESUB SiP Module Benefits

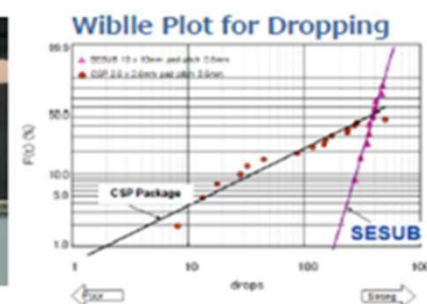
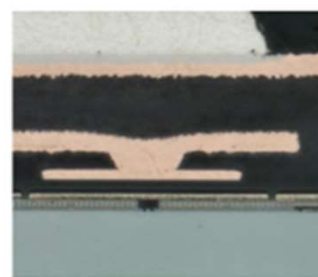
## PCB Miniaturization

- Average Package Body Size Shrink of >40%
- Top and Bottom surfaces of substrate free for other components (Maximizing Component Surface Area)



## Mechanical Robustness

- Highly Reliable Copper Interconnections (No Solder)
- Weibull Plots Show > than 200 Drop to 1st Fail



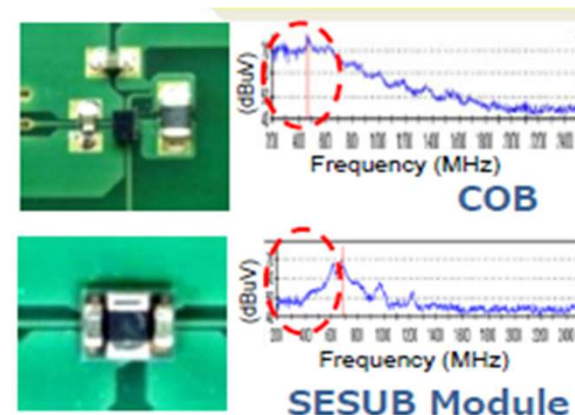
## Improved Heat Dissipation

- Reduction of Insulate Materials to PCB
- Allows Top Side Surface for Heat Distribution
- 7-15% usually seen for standard designs



## Improved Electrical Performance

- Short Cu Connections Improve Parasitic and Distortions



# SESUB Existing Major Applications

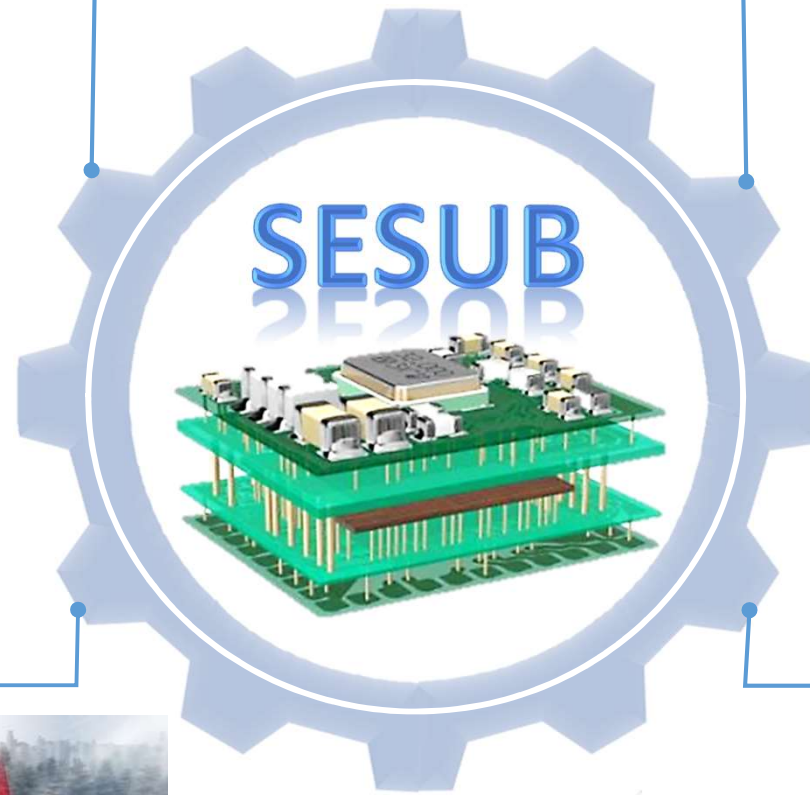
## Data Center

- Power Convertor
- Optical
- Memory
- Controller



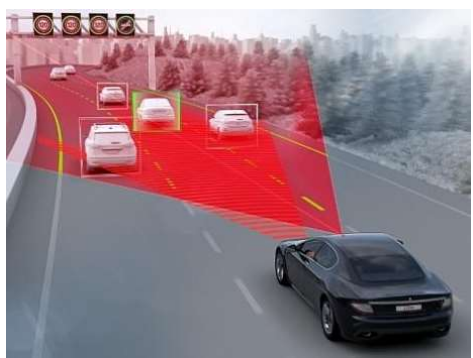
## Smart Phone

- Power Management -
- Wireless Charge -
- WIFI/BT -
- AR/VR/MR -
- Audio -
- 5G -
- AI -



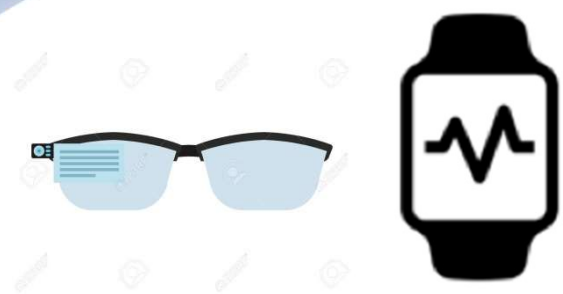
## Automotive

- Image Sensor
- Radar
- Infotainment



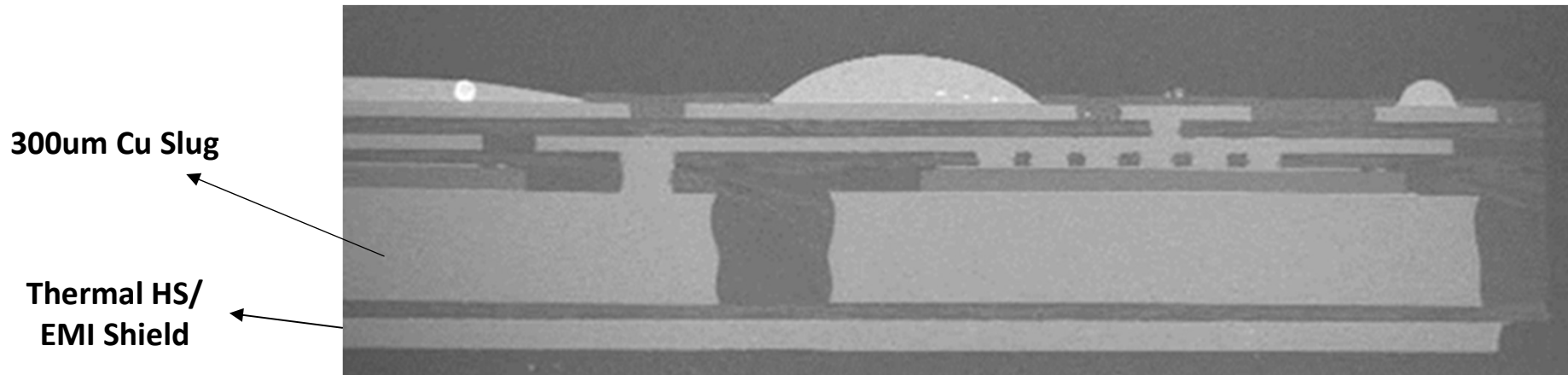
## Sensor & Optical

- HRM -
- PD -
- Controller -



# What's *a-EASI*?

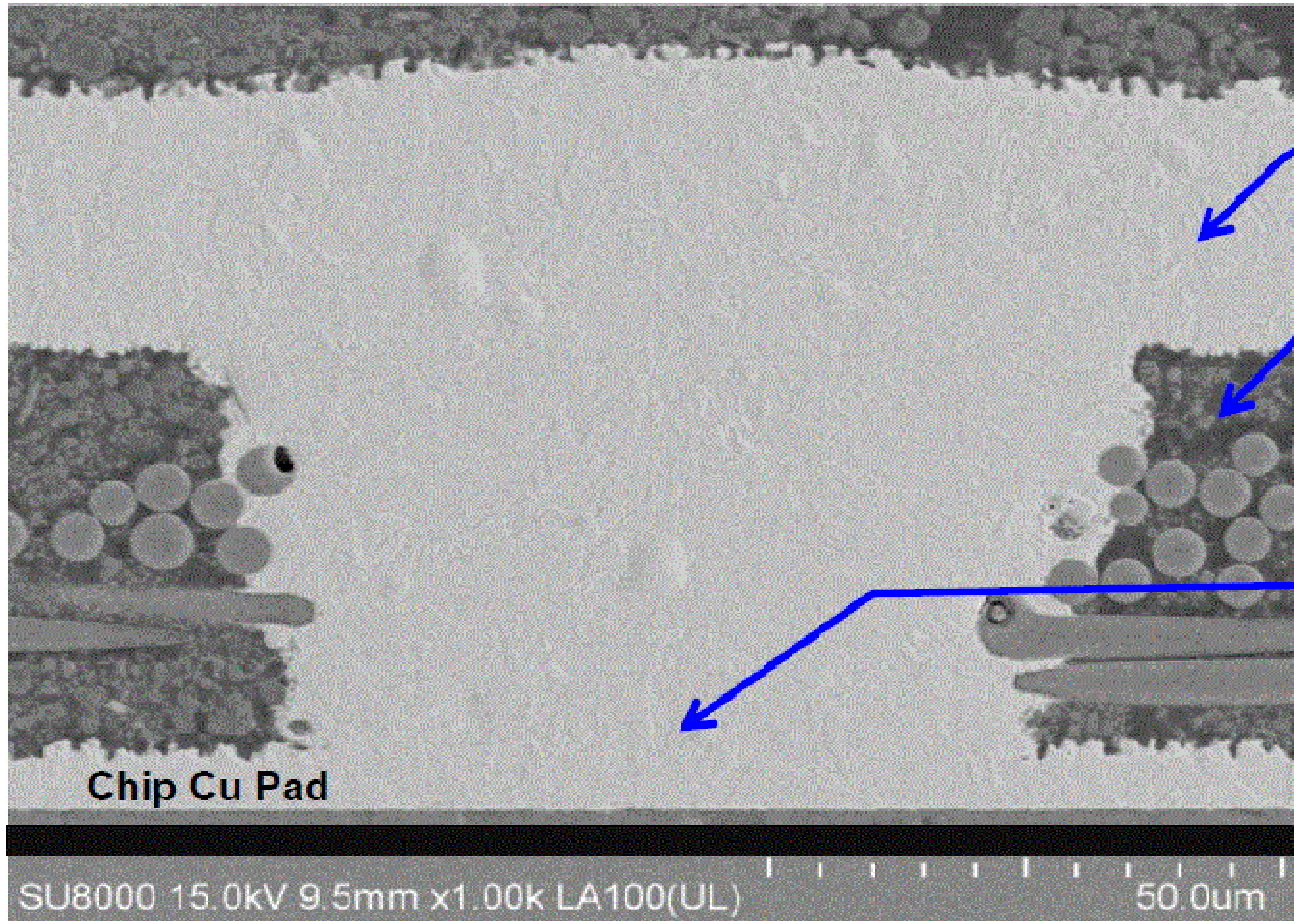
**aEASI = Advanced Embedded Active System Integration**



- Utilizes Mature Organic Substrate Process Modified to Meet **High Power Applications**
- Hybrid Power Package Combining Lead frame & Substrate Technologies
- **Good Current Capability- ~60A** (Integrated Power Stage Example), **~ 1.9W/mm<sup>2</sup>**
- 300um thick Copper Heat Spreader/Electrical Pad (Back of Die)
- Deep Full Filled Vias to Die **~ 130um Diam**
- Ultra Low Resistivity Die Attach Interface

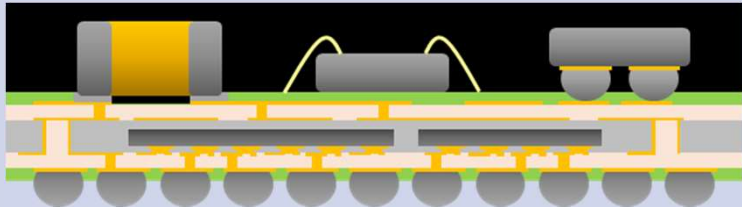
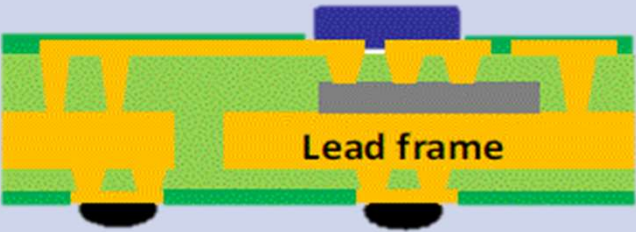
# a-EASI Cu Interconnect Highlights

\* Design for power devices



- Thick Cu RDL (32 um).  
Minimize turn on resistance.
- Prepreg material provide  
>2.5KV breakdown voltage
- 50um via diameter (Equal  
to 4 x 1 mil wire bond in  
conductor area)
- Cu to Cu interface.  
Minimize reliability risk in  
high current density  
condition

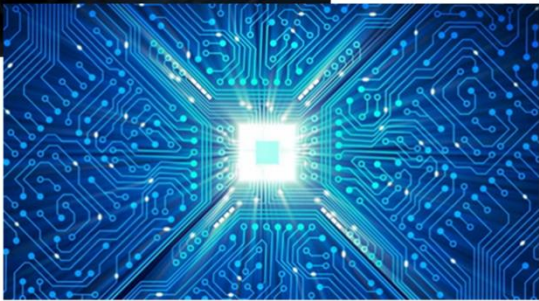
# ASE Embedded Solution Comparison

Solution	SESUB	a-EASI
Structure		
Base	Organic core & Pre-preg	Lead frame
Pinout	BGA/LGA	BGA/LGA/QFN
Package size	<b>200+ (mm<sup>2</sup>)</b>	<50( mm <sup>2</sup> )
Thermal	Good	<b>Excellent</b>
IOs	<b>Up to 1000</b>	Up to 100
Power	<20+ (W)	<b>1000+(W)</b>
Application	PMIC, Audio, Sensor, Optical, Connectivity, MCU, FEM, Memory, Image module, etc.	MOSFET, Regulator, DCDC, IGBT, power modules, etc.

# Miniaturization



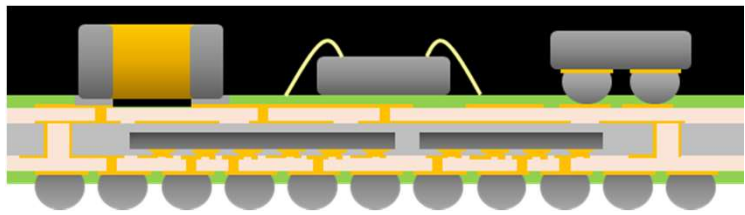
# Enhanced Performance



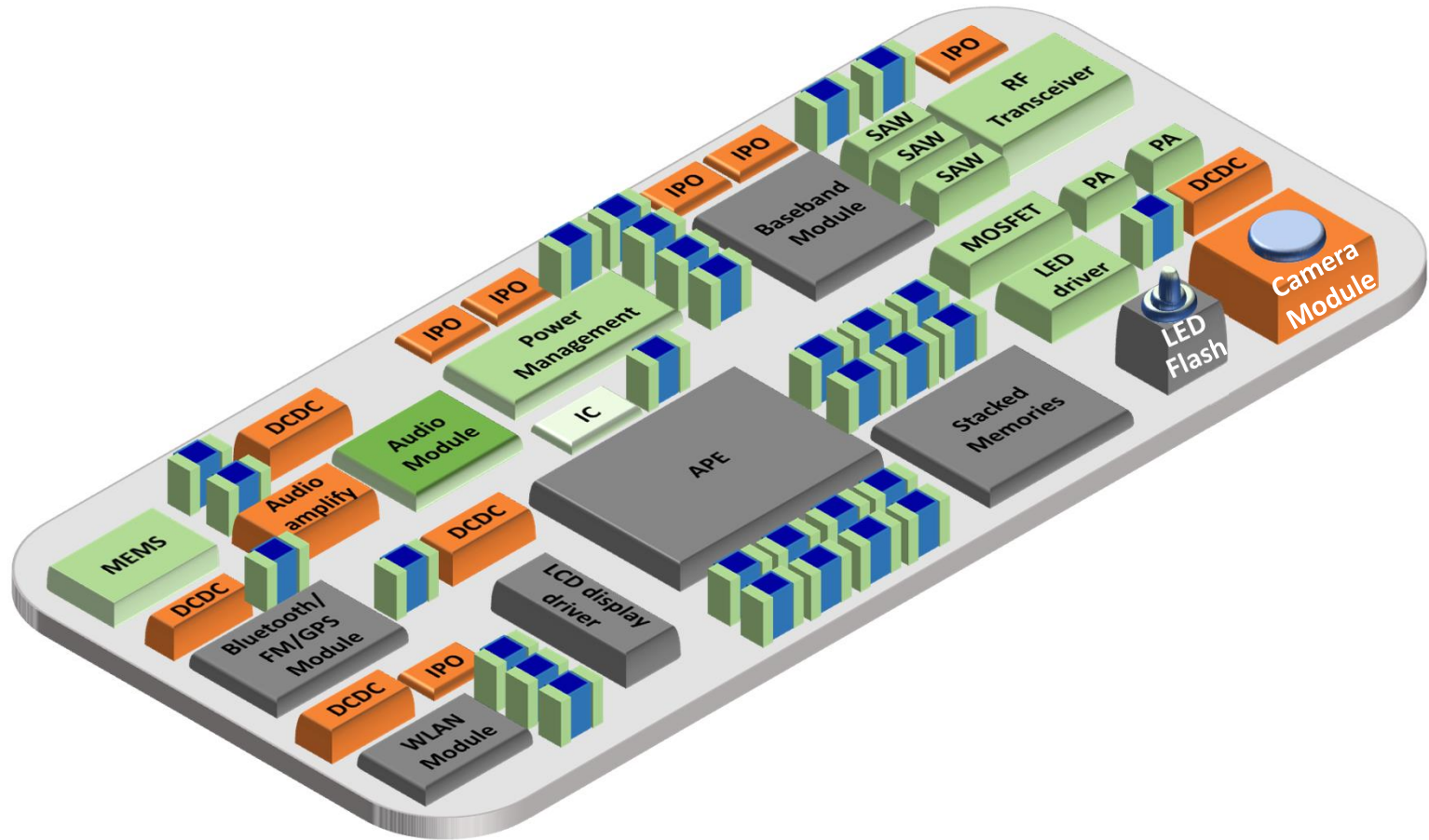
# High Integration

# • Future Trend & Demand

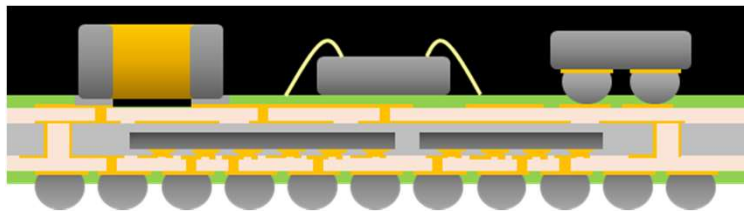




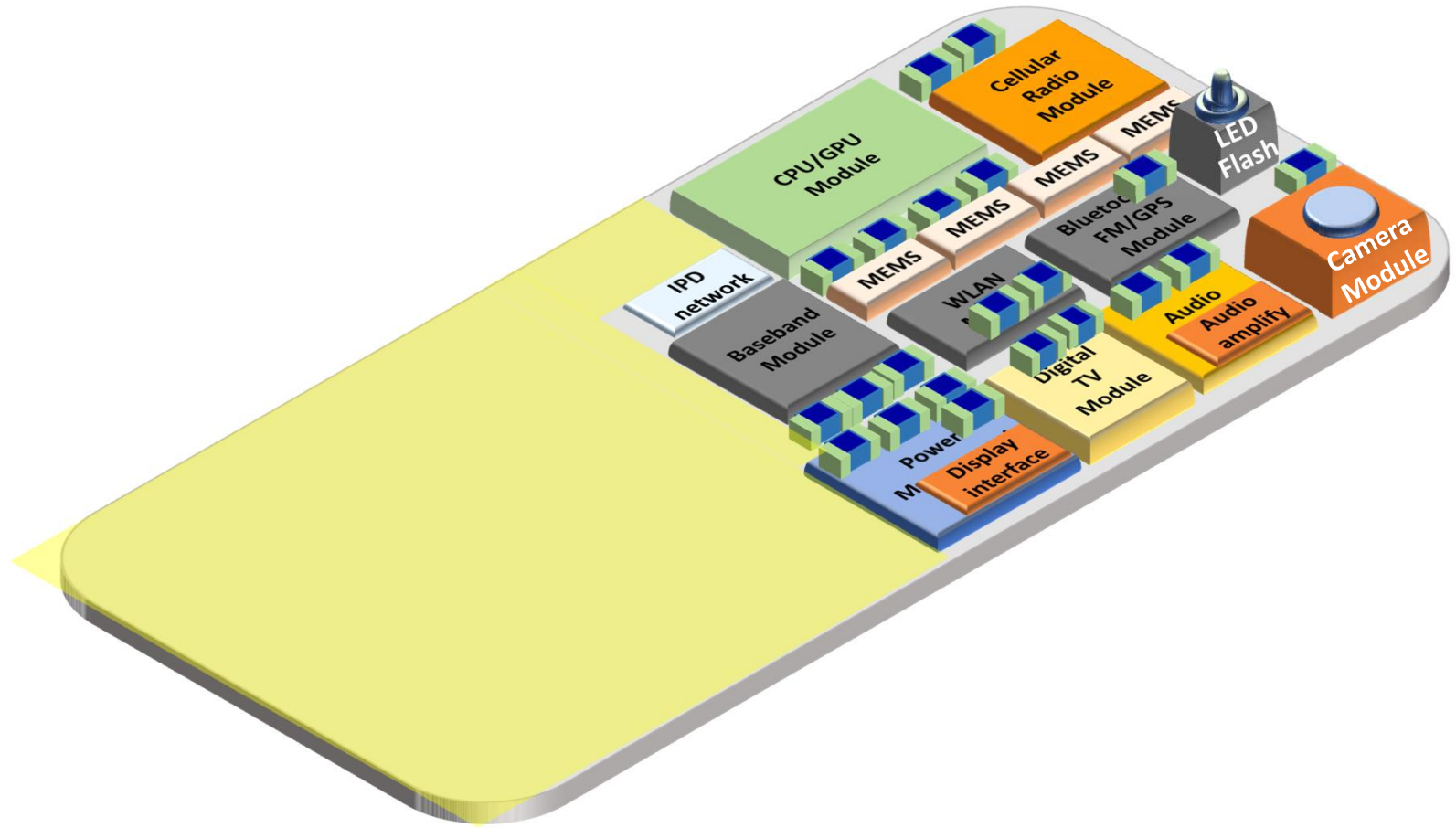
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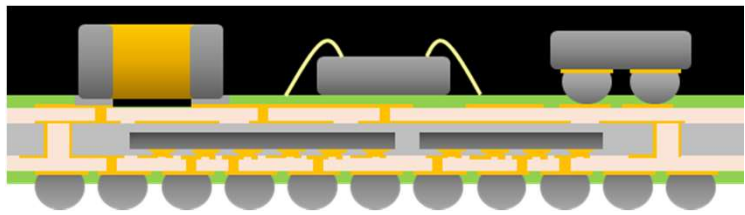




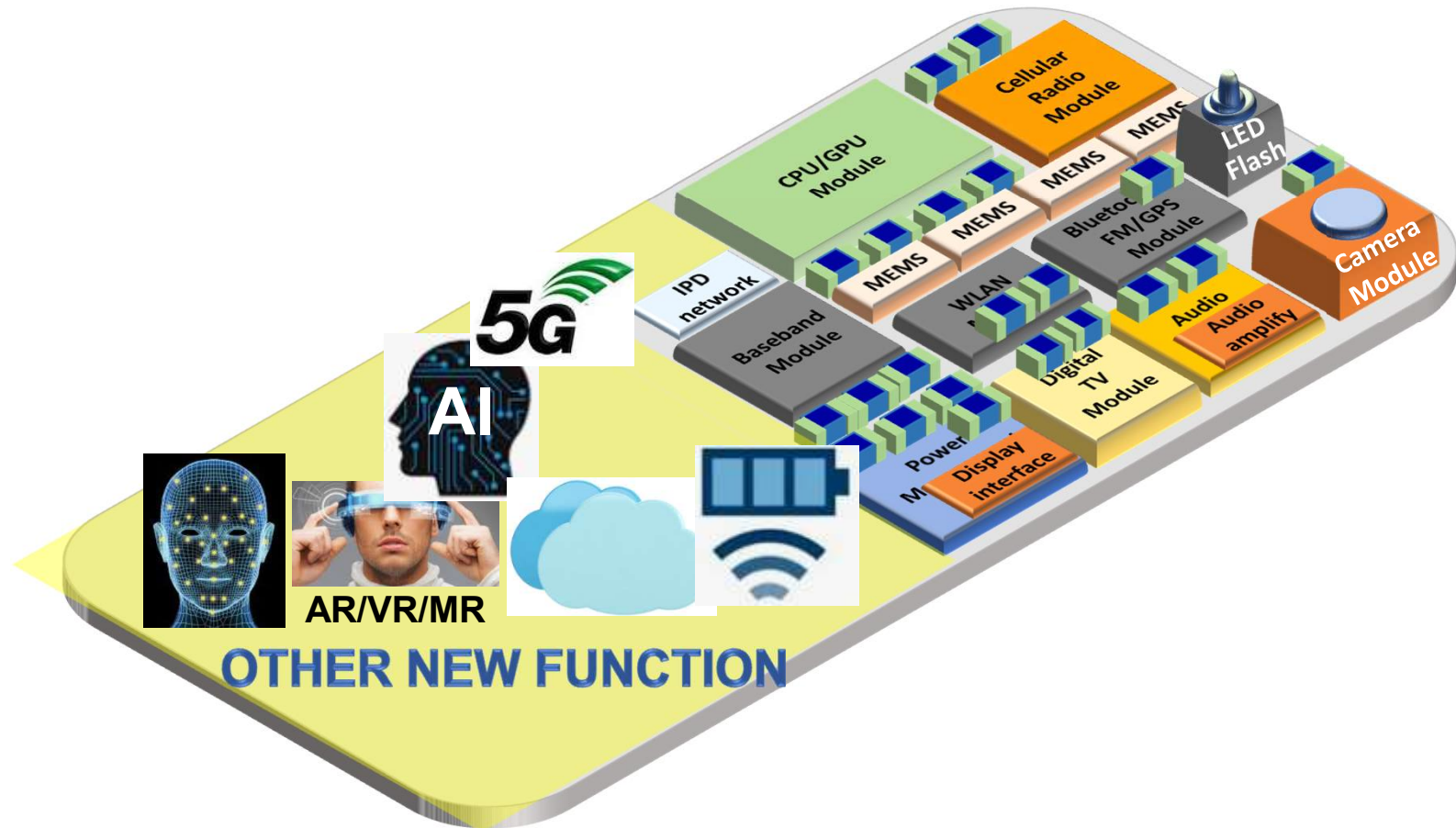


# SESUB





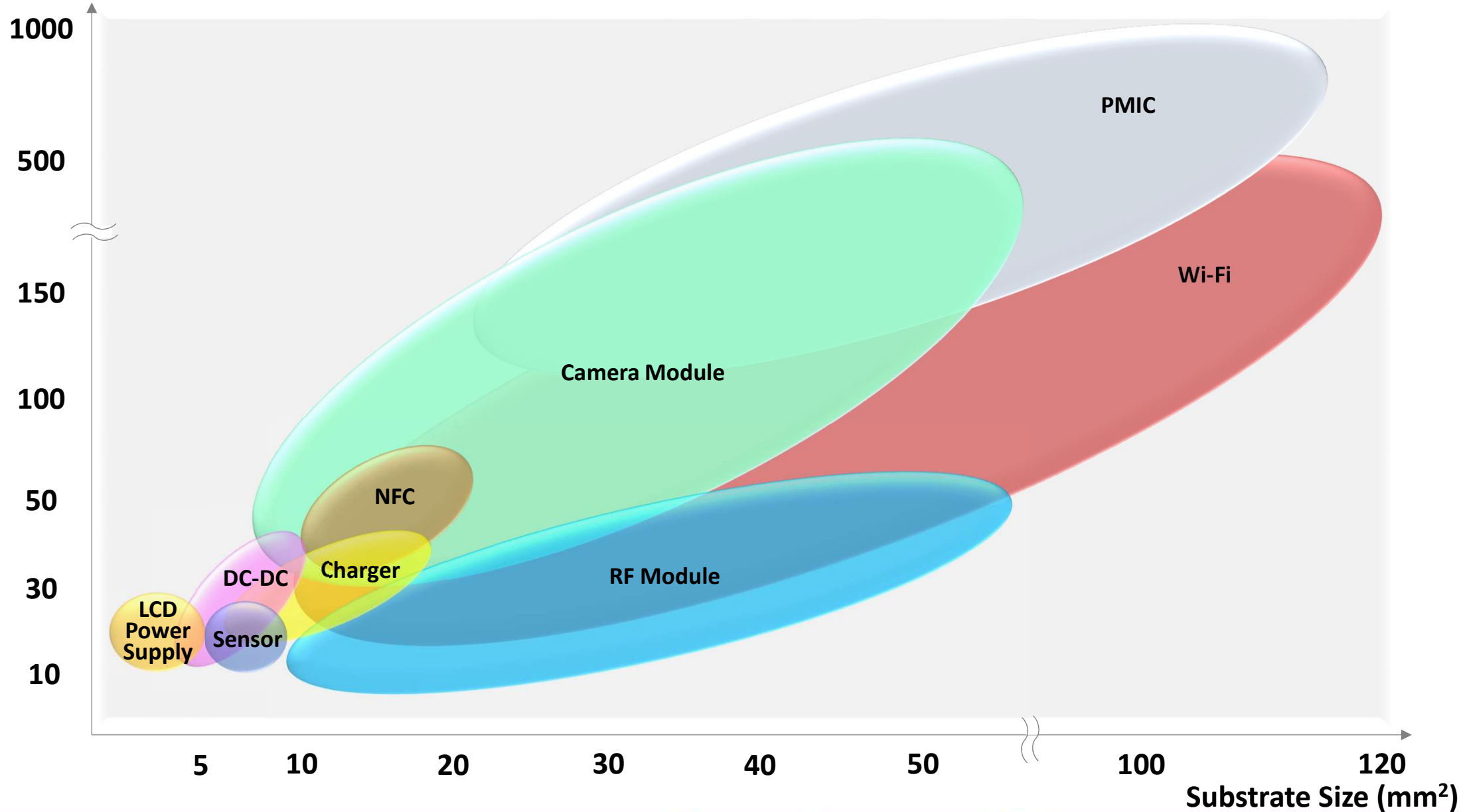
# SESUB



- **Board assembly simplification and X-Y dimension reduction could be enabled by embedded die architecture.**

# Targeted Application Domain

Ball Pin Count



# • Summary



Design

Embedded Substrate

Simulation

***Embedded  
Package / SiP***

Test

Bumping

Assembly / SMT



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**Thank You**

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