A 100MHz IVR PMIC with On-silicon Magnetic Thin Film Inductors

Peng Zou, Song Wei, Xie Qiang, Chen Liang, Chen Yue, Huang Chen, Wang Jiake, Wang Xinyu, Li Hongwei, Cui Xiaojuan

Hisilicon Semiconductor Co., Ltd. A Huawei Company, Shenzhen, China

www.huawei.com

LEGAL NOTICE

THIS PRESENTATION AND RELATED MATERIALS AND INFORMATION ARE PROVIDED "AS IS" WITH NO WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION, OR SAMPLE. HUAWEI ASSUMES NO RESPONSIBILITY FOR ANY ERRORS CONTAINED IN THIS PRESENTATION AND HAS NO LIABILITIES OR OBLIGATIONS FOR ANY DAMAGES ARISING FROM OR IN CONNECTION WITH THE USE OF THIS PRESENTATION.

NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED HEREIN.

Current State of Inductor Based IVR Technology

- **Very small pool of participants (publically)**
  - ✓ Large funding & patience
  - ✓ Wafer fabrication infrastructure
  - ✓ Cross-discipline engineering team
- **Limited progress being reported since 2010**
- **Magnetic Thin-film Inductor IVR saves power, space and cost?**
  - ✓ Still a hypothesis to be proven
- **Efficiency— the biggest hurdle to convince customer**
  - ✓ 2 stage conversion vs. single stage
  - ✓ Thin film inductor efficiency @high frequency?

	[1]	[2]	[3]	[4]	[5]
Year	2010	2012	2014	2017	2017
Company	Intel	Columbia Univ./IBM	Intel	Intel	Ferric
Process Technology	90nm CMOS	45nm SOI	22nm CMOS	14nm CMOS	130nm BCD?
Inductor Technology	Monolithic Strip-line Inductor	2.5D Interposer /Strip-line Inductor	Package Inductor Air Core	Monolithic/ Solenoid Inductor	Monolithic/ Solenoid Inductor
Core Material	Ni80Fe20	NiFe	Air Core	NA	CZT
Inductor Quality Factor	NA	~1.2*	NA	~3.8*	20
Fsw(MHz)	100	75	140	100	100
L(nH)	17	5.9	1.5	1.5	10
Vin(V)	NA	1.8	1.7	1.5	1.8
Vout(V)	NA	1.1	0.88	1.15	0.9
Peak Efficiency	76%	74%	90%	84%	~78%
Iout_max(A)	400	>4	700	0.42	3A
Conversion Ratio (Vout/Vin)	NA	0.61	0.59	0.66	0.5

[1] J. T. DiBene, et al., “A 400 Amp Fully Integrated Silicon Voltage Regulator with In-die Magnetically Coupled Embedded Inductors,” IEEE Applied Power Electronics Conf., Palm Springs, CA, 2010
[2] N. Sturcken, et al., “A 2.5D Integrated Voltage Regulator Using Coupled-Magnetic-Core Inductors on Silicon Interposer Delivering 10.8A/mm^2,” ISSCC, pp. 400-401, 2012
[3] E. Burton, G. Schrom, et al., “FIVR-Fully Integrated Voltage Regulators on 4th Generation Intel Core SoCs,” IEEE Applied Power Electronics Conf., pp. 432-439, 2014
[4] H. Krishnamurthy, et al., “A Digitally Controlled Fully Integrated Voltage Regulator with On-Die Solenoid Inductor with Planar Magnetic Core in 14nm Tri-Gate CMOS,” ISSCC, pp. 336-337, 2017
[5] N. Sturcken, “Thin Film Inductors for Integrated Power Conversion”, IEEE Applied Power Electronics Conf., Tampa, Florida, 2017

Integrated Power Delivery from More Moore Perspective

- **Processor core counts continue scale up**
- **Supply voltage scaling down plateaued**
- **Thermal constrained power density limit → dark silicon**
  - ✓ Portion of cores would be turned off at any given time
  - ✓ Dynamic and heterogeneous power/thermal management needed
  - ✓ Super-threshold and near-threshold domain coexist
- **IVR becomes a must-have technology**
  - ✓ Conventional VR is ill-suited for variety and granularity of voltage domains.
  - ✓ Minimizing voltage variation for timing convergence, i.e. thinking 50mV's impact at 0.8V and 0.4V supply voltage, respectively.

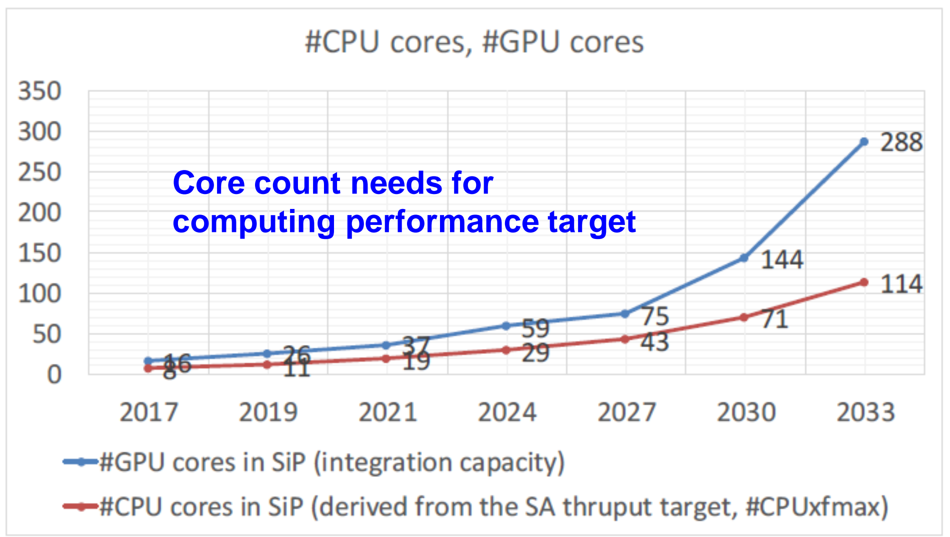
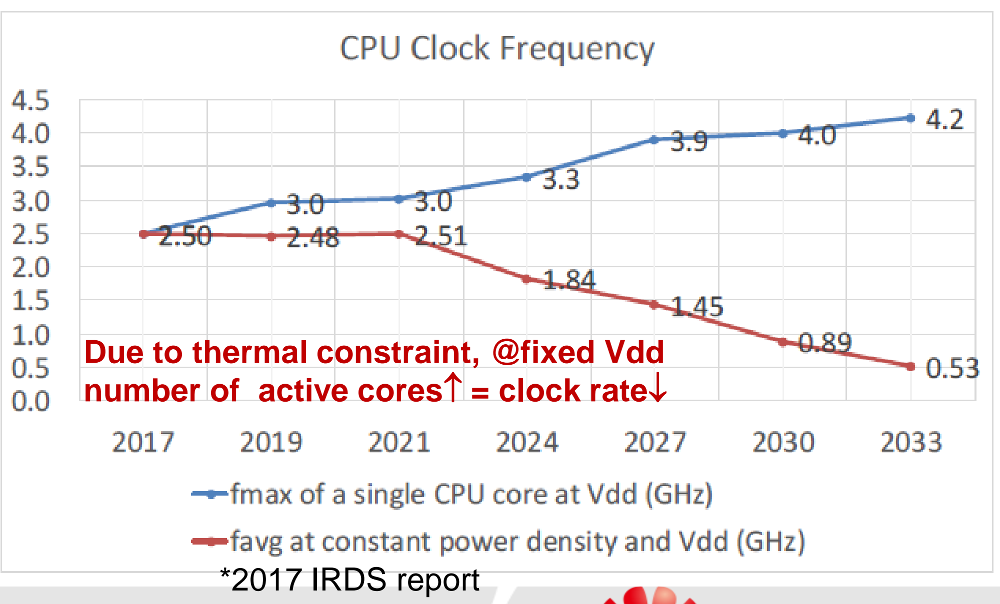


Figure MM-4 Number of CPU and GPU core in an 80mm² die



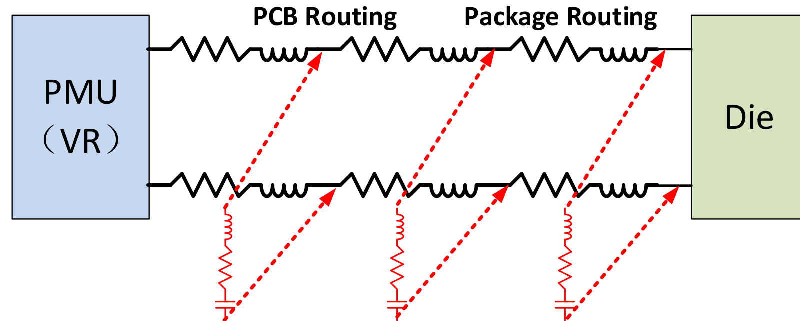
*2017 IRDS report

YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
	P54M36	P48M28	P42M24	P36M21	P32M14	P32M14T2	P32M14T4
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5-f1.0	i1.0-f0.7
Logic device structure options	finFET FDSOI	finFET LGAA	LGAA finFET	LGAA VGAA	LGAA VGAA	VGAA, LGAA 3DVLSI	VGAA, LGAA 3DVLSI
Logic device mainstream device	finFET	finFET	LGAA	LGAA	LGAA	VGAA	VGAA
DEVICE STRUCTURES							
	FinFET FD-SOI	FinFET Lateral Nanowire	Lateral Nanowire FinFET	Lateral Nanowire Vertical Nanowire	Lateral Nanowire Vertical Nanowire	Vertical Nanowire Monolithic 3D	Vertical Nanowire Monolithic 3D
DEVICE ELECTRICAL SPECS							
Logic device mainstream device	finFET	finFET	LGAA	LGAA	LGAA	VGAA	VGAA
Power Supply Voltage - Vdd (V)	0.75	0.70	0.65	0.65	0.65	0.60	0.55

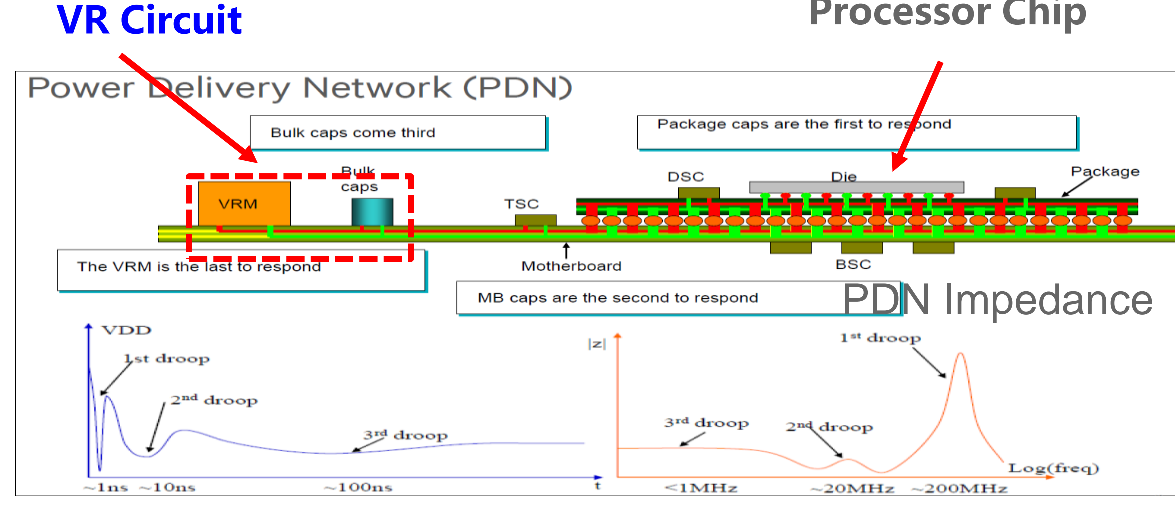
HUAWEI

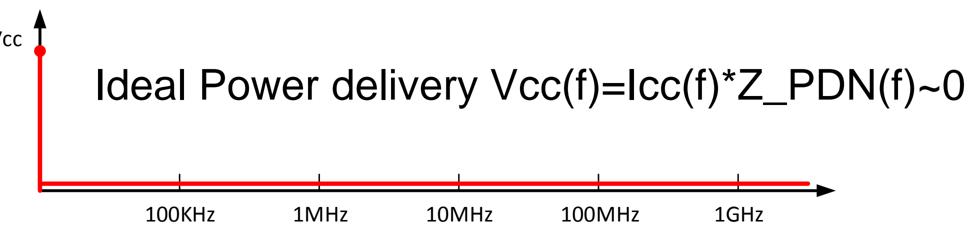
IVR from Power Delivery Perspective

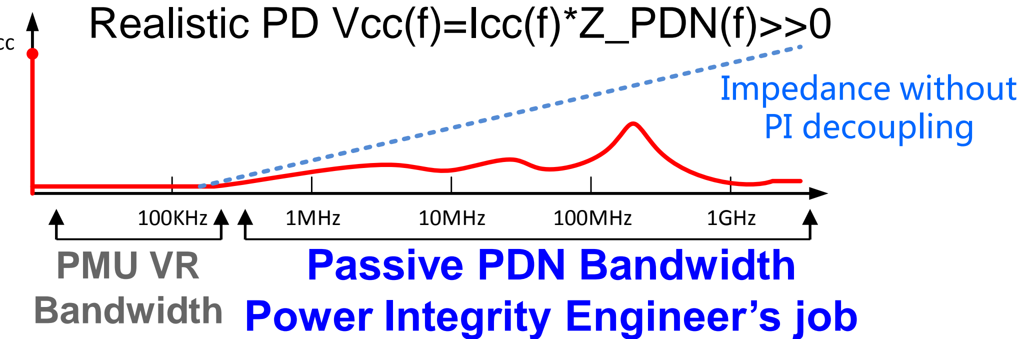
- **Conventional VR regulation bandwidth has no effect to PDN impedance above 500KHz**
- **Reducing Supply voltage variation largely depends on power integrity design: passive decoupling capacitors for die/package/PCB**
  - ✓ Passive decoupling always leads to several resonance peaks in PDN impedance profile
- **With limited room to further lower PDN impedance, future processor's supply voltage variation is expected to worsen**
- **IVR is among limited options to further lower PDN impedance**
  - a) eliminating PDN bottleneck due to PCB/package
  - b) active PI decoupling from ~100MHz regulation bandwidth



Decoupling capacitors to lower impedance at specific frequency



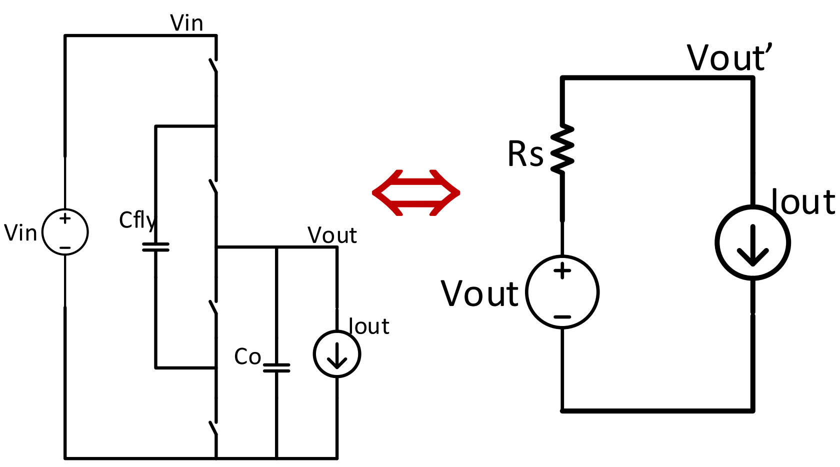




Can We Live with Inductor-less IVR?

- On-die LDO and switched capacitor converter have been favorite subjects in PowerSoC community
  - ✓ Implementation and efficiency challenges of integrated buck converter are difficult to overcome
- **LDO and switched capacitor VR cannot replace buck converter as POL VR in case of high power density applications.**

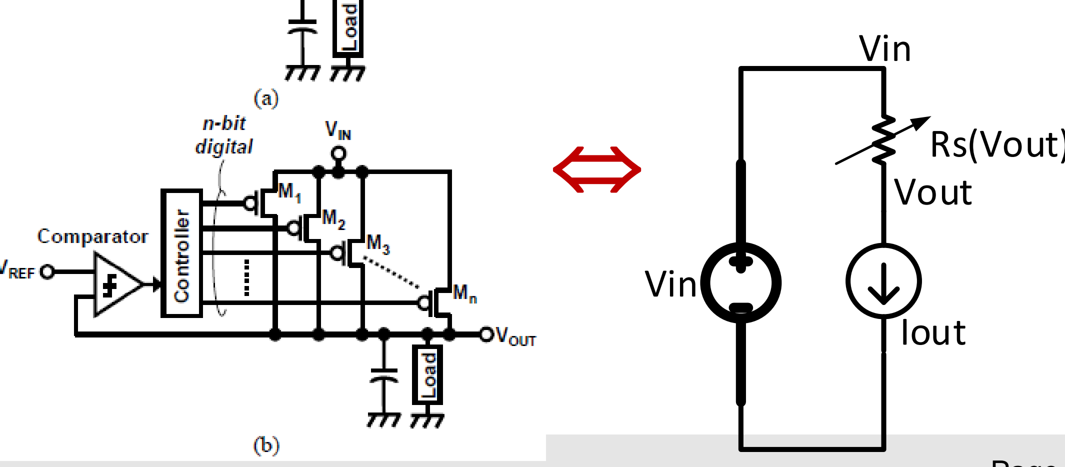
Switched capacitor converter difficult for good load regulator under high current load.



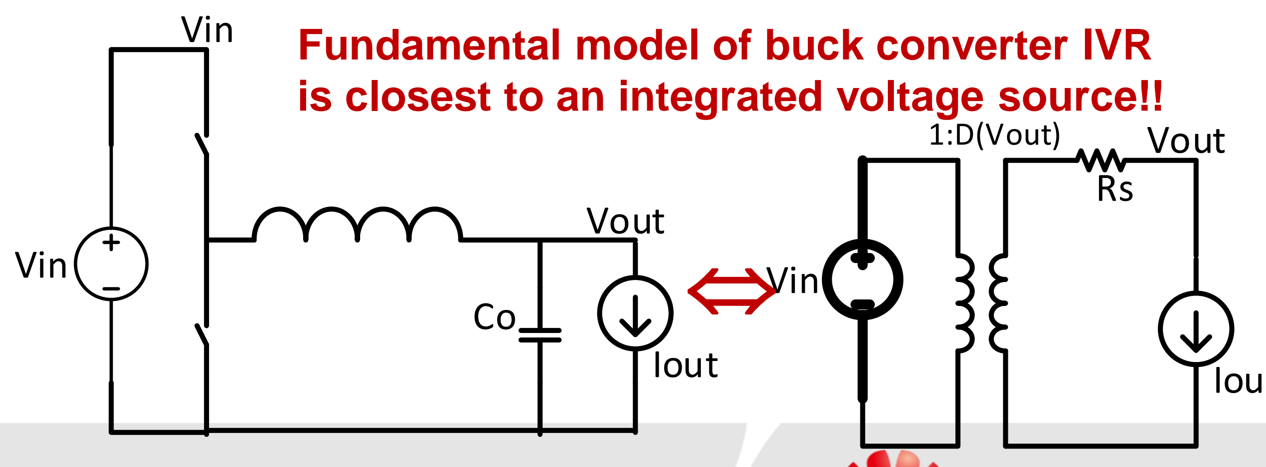
LDO is equivalent to a variable resistor.

Peak current and load transient challenge is passed to input VR stage of LDO.

Trade-off between load regulation and efficiency.



Fundamental model of buck converter IVR is closest to an integrated voltage source!!



100MHz IVR PMIC with Integrated Magnetic Inductors

Key Features

Process technology: 40nm CMOS

Operating frequency: 80~140MHz

Input voltage: 1.4V ~ 2.2V

Output voltage: 0.5V ~ 1.2V

Number of VR cells: 8 (2-phase coupled buck VR)

Total number of phases: 16

Maximum output current: 1.25A/phase

Peak efficiency: 82% @1.8V to 0.85V

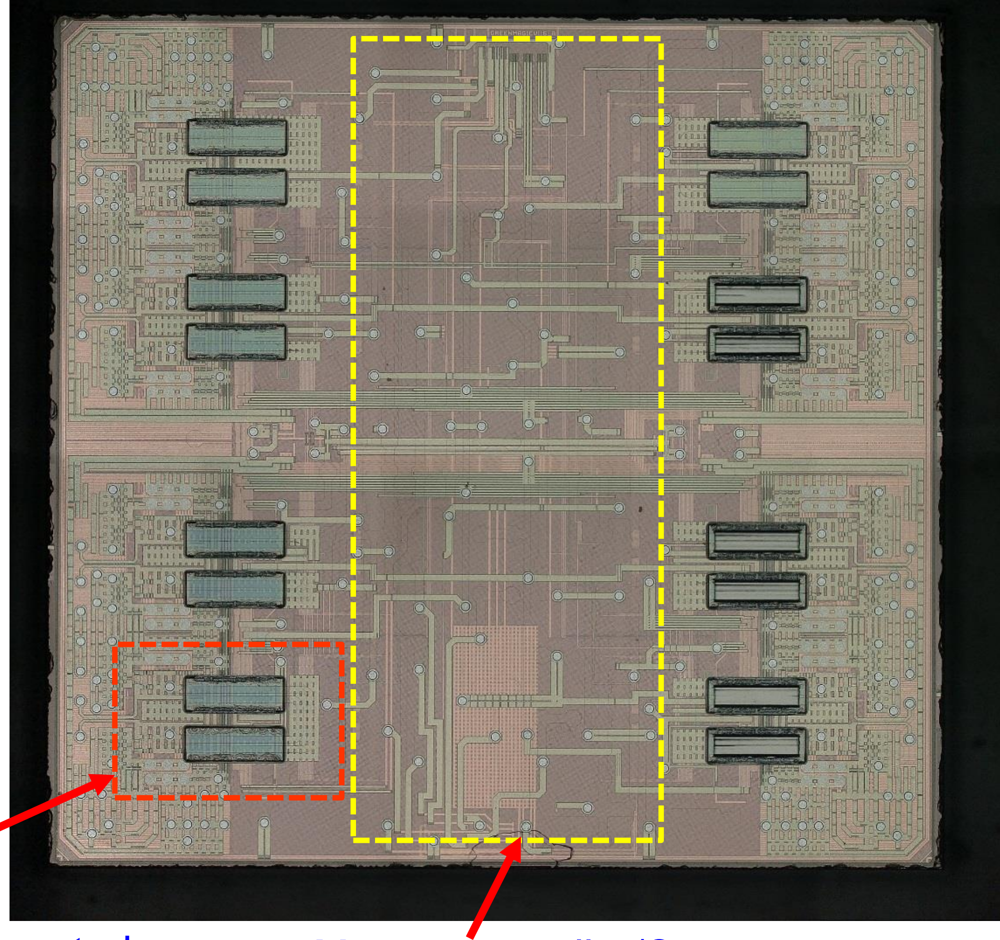
Inductor technology: coupled strip-line inductor

Inductance: 6~8nH

Coupling coefficient: 0.8

Package technology: WLCSP

Chip size: ~15mm^2



Strip-line Magnetic Thin Film Inductor

Magnetic film properties:

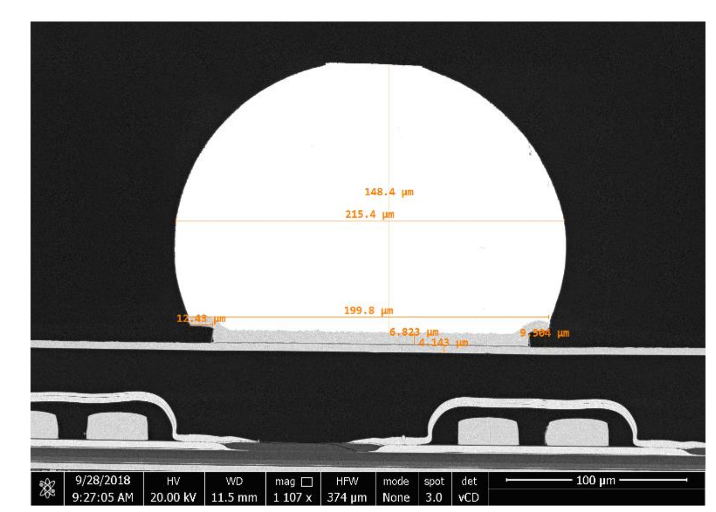
- laminated CoZrTaB alloy
- H_k=15Oe
- H_{c_hard}=0.27Oe
- Saturation flux density ~ 1.0T
- Resistivity = 115µΩ•cm

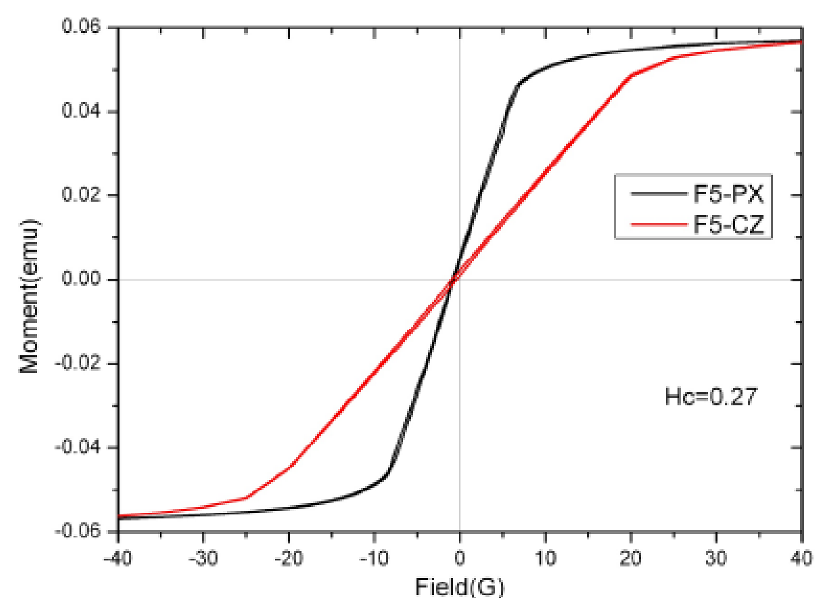
Inductor properties:

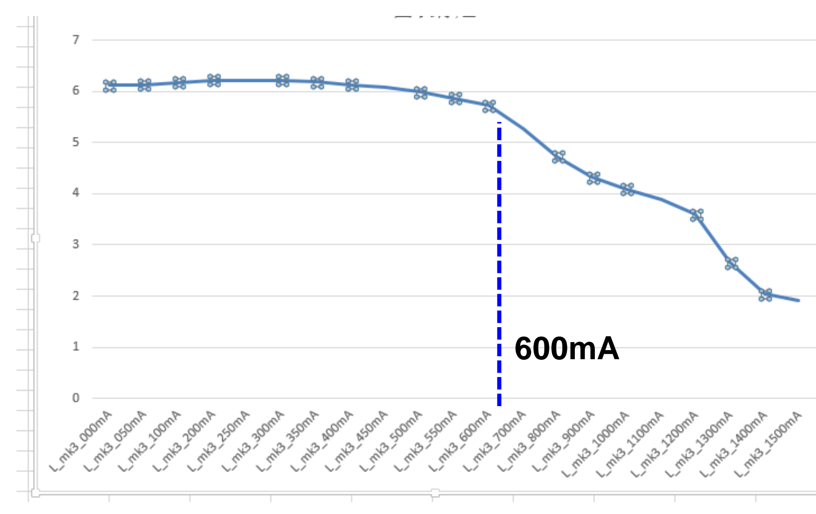
- Inductance 6~8nH@100MHz
- Rdc ~60mΩ
- Rac 400~500mΩ@100MHz
- Isat ~600mA@100MHz

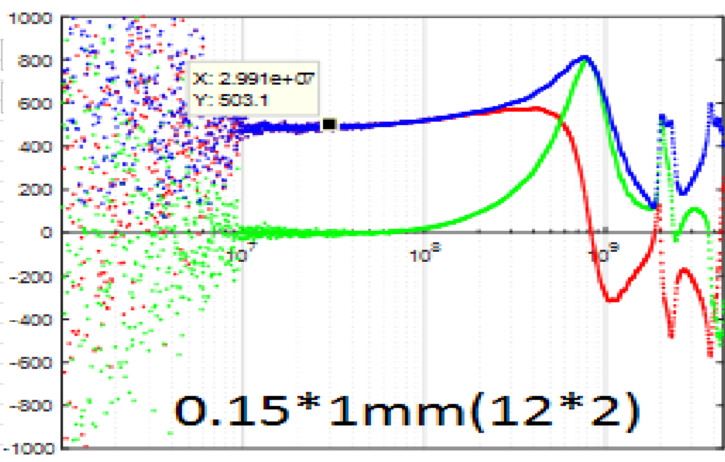
Integration technology:

- On-die
- Compatible with WLCSP









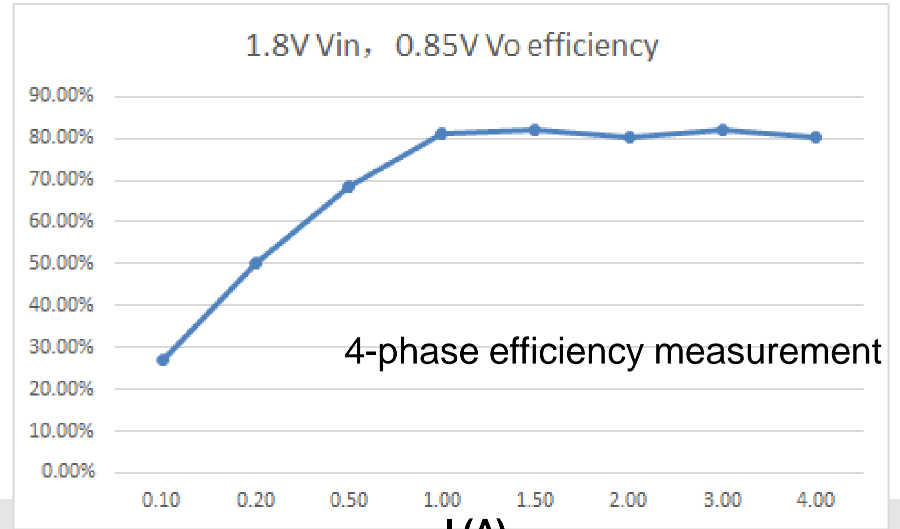
3mmx3mm laminated 4um thick CZTB film sample VSM (above) and Permeability (bottom) measurement

HUAWEI TECHNOLOGIES Co., Ltd.
HUAWEI Confidential
HUAWEI

100MHz IVR Circuit Implementation

Key VR Controller Features

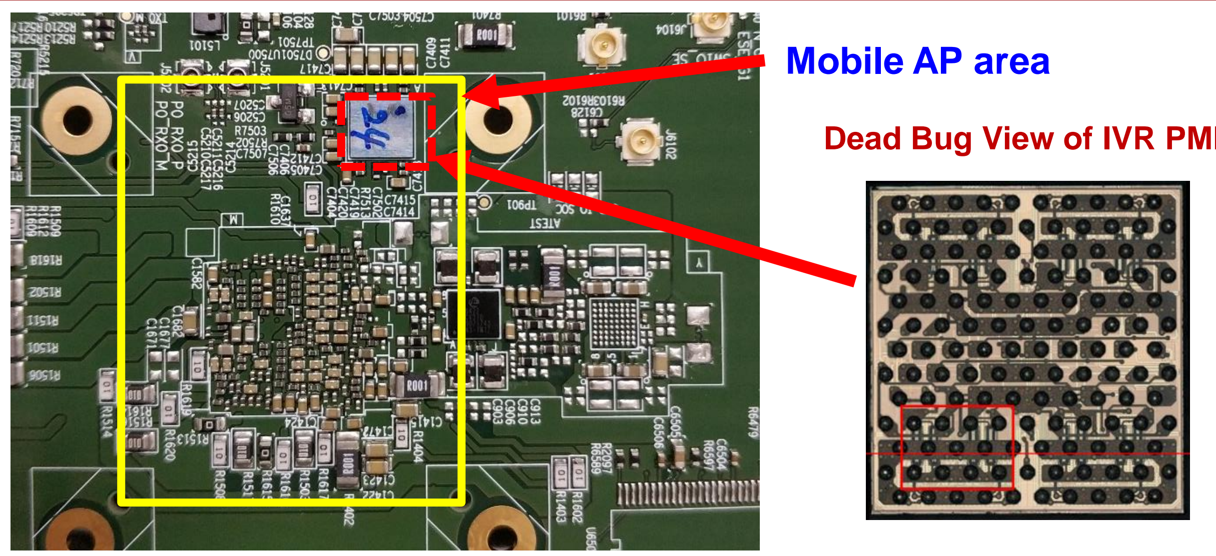
- Cascode power stage for 2V input voltage
- Input voltage: 1.4V ~ 2.2V
- Output voltage: 0.5V ~ 1.2V
- 2-phase coupled inductor buck converter as basic VR unit; total 8 VR cells
- Fast transient control scheme: hysteresis (fast loop)+conventional voltage mode (slow loop)
- UGB of fast regulation loop up to 100MHz
- Current balancing control for 16 phases ~20mA residual error

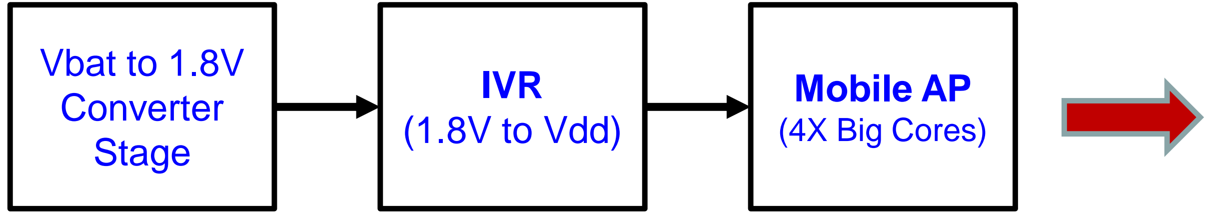


Cascode Power Stage Topology &
Fast + Slow Dual Regulation Loop Architecture

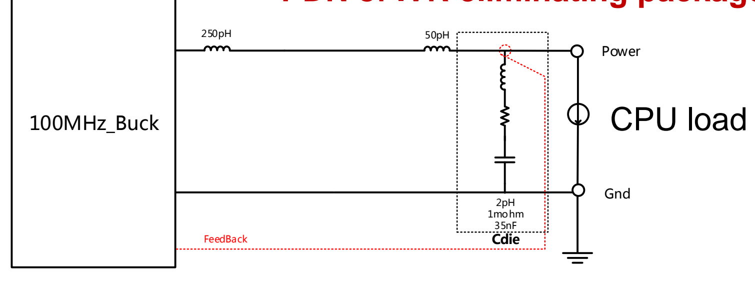
System Test Setup

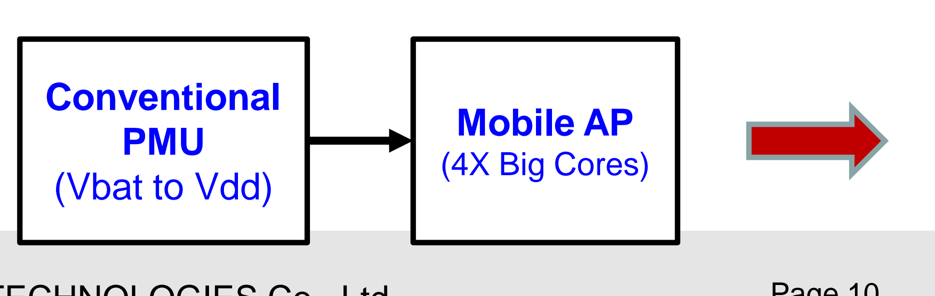
- Power delivery comparison between IVR and conventional PMU was carried out.
- Mobile AP is on the opposite side of PCB.
- IVR testing setup eliminates all output PCB/package decoupling capacitors.
- **IVR powers 4 big ARM cores, and total output capacitance ~56nF (on AP die).**



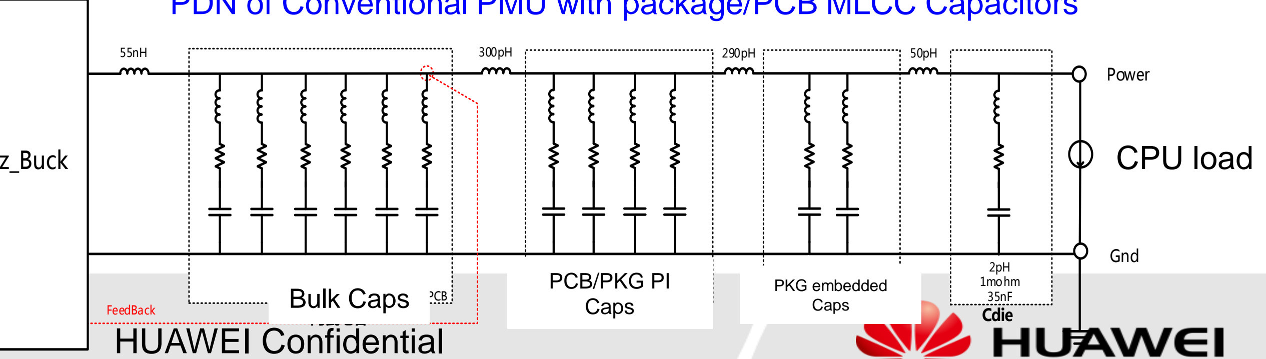


PDN of IVR eliminating package/PCB MLCC Capacitors



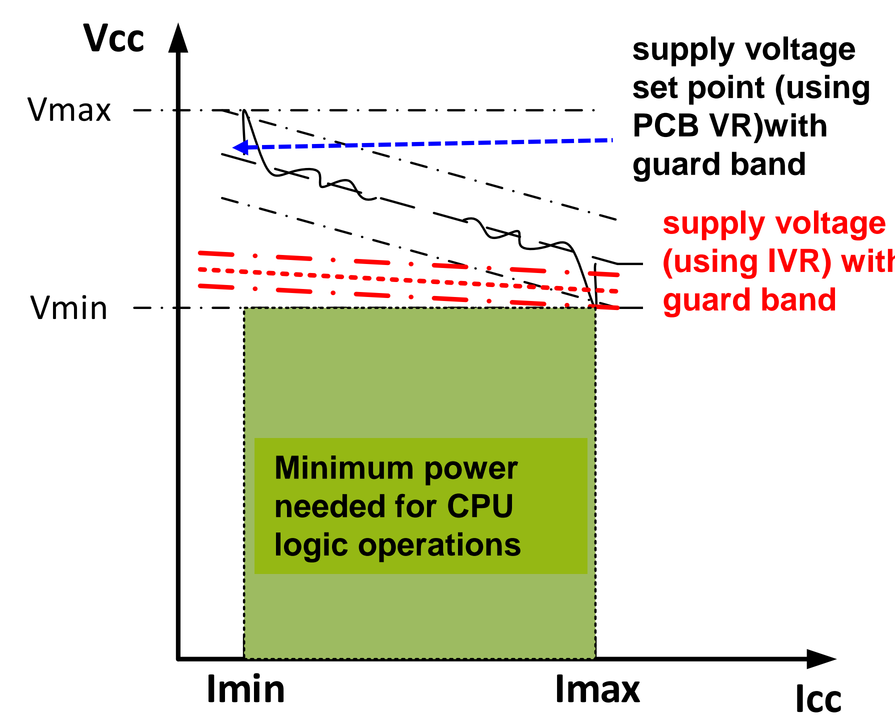


PDN of Conventional PMU with package/PCB MLCC Capacitors



IVR Improves Energy Efficiency of Power Delivery

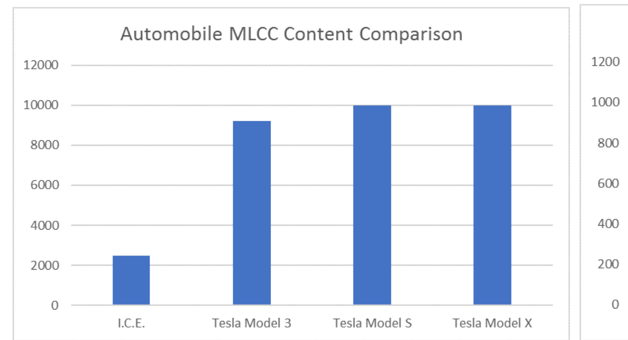
- ~100MHz switching frequency and high regulation bandwidth can reduce supply voltage variation → less guard-banding in supply voltage, less power
- Increase output capacitance (on-die or close to die) can help further on lowering supply voltage; challenges are in how to implement more capacitance
  - ✓ Increasing die size of mobile AP
  - ✓ Implementing MIM capacitor in AP
  - ✓ Low parasitic package IPD capacitor
- IVR can relax PCB/package PDN design requirements
- Achieving substantial system energy efficiency gain to offset conversion efficiency loss due to 2 stage conversion is essential
  - ✓ Amplitude of voltage guard band reduction may be workload dependable
  - ✓ What to incentivize customer adoption?

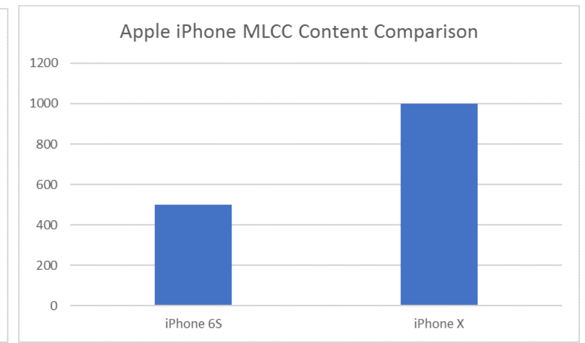


Energy efficiency improvement from reduced guard band in supply voltage, due to IVR's moderate load line and reduced droop

An Unexpected Catalyst for IVR's Commercial Adoption

- ❑ Growing gap between MLCC supply and demand
- ❑ Cost (component price & PCB area) of using MLCC may become top issues for system engineers.
- ❑ Prolonged Shortage (>5yr) could ignite more interest for IVR's less MLCC dependent nature.

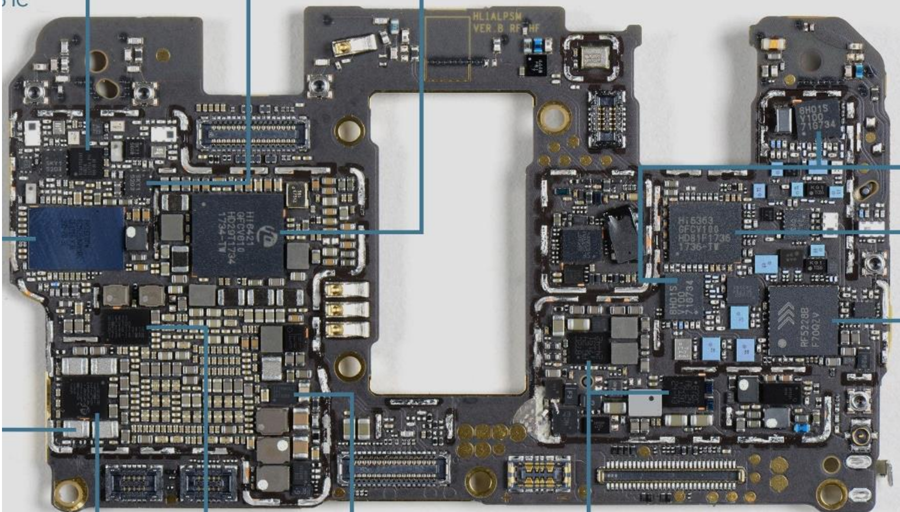




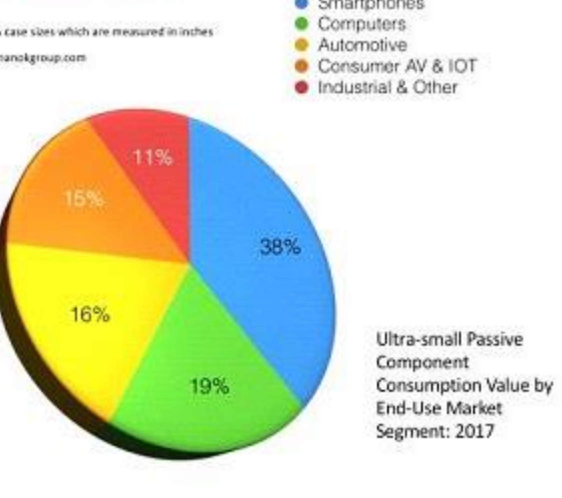
MLCC demand increase is expected trend.
Multiple end markets compete limited supply.

MLCC Shortages Are Creating Challenges In Multiple End-Markets in 2018
03/02/2018 // Dennis M. Zogbi in: Passives

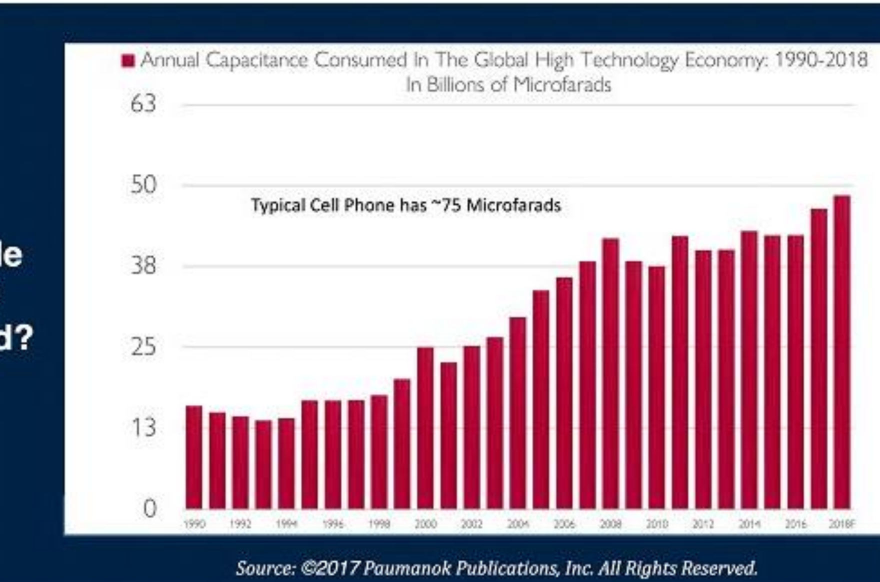
Limited Capacity To Stack Ceramic Dielectric Will Extend MLCC Shortages To 2020 and beyond.



Typical smartphone system has noticeable amount of MLCC content.



*Based on technical report from TTI, Inc.



Supply Chain Challenges of Commercializing Magnetic Inductor IVR

Where to manufacture?

	Cost	Cross Contamination	Decoupled from specific CMOS node	12-inch process
Foundry	High?	Big concern	Business model?	yes
OSAT	less	Less sensitive	flexible	yes

Cobalt price's significant surge and plunge creates uncertainty on cost expectation of thin film inductors.

Fabrication bottleneck from magnetic thin film deposition

- PVD deposition of 5μm and thicker laminated magnetic film
- Thick copper RDL layer deposition for inductor windings

Material cost and sourcing

- Usage amount of magnetic material can be a major challenge for cost down
- May be too susceptible to volatility in Cobalt price
- Limited sourcing channels for CoZrTa may create hurdle for high volume adoption, i.e. smartphone.

Availability of high through-put 12-inch magnetic PVD tool?

- Existing PVD tool is not optimized for this application

Final Thoughts

- **Break-through on integrated magnetic inductor IVR must happen for future mobile and server processors.**
- **Improved energy efficiency from lowered supply voltage by IVR is demonstrated. How far to trigger product adoption?**
- **On-die strip-line magnetic inductors are compatible with high volume wafer process flow; many supply chain challenges have to be addressed before mass production.**
- **Productization of IVR with magnetic inductors may be sooner than we think…**
- **Some areas for future research:**
  - ✓ Alternative core materials – saturation magnetic flux density 2T or higher, resistivity > 500μΩ•cm
  - ✓ High efficiency VR topologies for both IVR input stage and IVR

Thank you

www.huawei.com