Non-linear Control for Linear Regulators

Arijit Raychowdhury
Georgia Institute of Technology
arijit.raychowdhury@ece.gatech.edu

PowerSoC 2018
Outline

- Motivation
  - Digitally Assisted and All-Digital LDOs

- Discrete Time All-Digital LDOs
  - Loop Architecture and Circuit Design
  - Reduced Dynamic Stability
  - Measured Results

- Switched Mode Control
  - Hybrid, Dual-Loop Topologies
  - Measured Results

- Unified Voltage and Frequency Regulation
  - Loop Architecture and Circuits
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- Conclusions
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SoC as a Dynamic Platform

Maximize performance & efficiency
- Independent V/F control regions
- Scenario-based power allocation
- Dynamic V/F control
- Workload-based core activation & shutdown

Deliver optimal power for just-in-time performance

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Linear and Low Dropout Regulators

**LC-VR**
- High efficiency
- Package integration
- Continuous Vout
- Large domains
- Fast response

**SC-VR**
- High efficiency
- Discrete Vout
- Medium response
- Low energy density

**Linear Regulator**
- Lower efficiency
- Die integration
- Finest domains
- Fastest response

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**Analog PMOS based LDO**

VREF

\[ V_{\text{REF}} \]

\[ P_{\text{INT}} \]

\[ P_{\text{OUT}} \]

\[ V_{\text{OUT}} \]

\[ R_1 \]

\[ R_2 \]

\[ A_V = \frac{\beta \cdot A_{\text{AMP}} \cdot g_m \cdot Z_{\text{LOAD}}}{(s - P_{\text{INT}})(s - P_{\text{OUT}})} \]

\[ \beta = \frac{R_2}{R_1 + R_2} \]

The important poles are internal \((P_{\text{INT}})\) and output \((P_{\text{OUT}})\)
All-Digital Discrete-Time LDO

- Mostly synchronous; Continuous time systems are also possible
- Single stage comparator
- Control Logic can implement PI control
<table>
<thead>
<tr>
<th>Analog LDO Regulator</th>
<th>Digital LDO Regulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>+High bandwidth</td>
<td>+No analog Components with synthesizable control</td>
</tr>
<tr>
<td>+Excellent small signal performance</td>
<td>+Decouples loop gain from operating voltage</td>
</tr>
<tr>
<td>+High power supply rejection (PSR)</td>
<td>+Large operating range (both supply voltage and load current)</td>
</tr>
<tr>
<td>+No Noticeable Ripple</td>
<td>-Output ripple</td>
</tr>
<tr>
<td>Limited by slew rate of the power PMOS</td>
<td>-Low PSR, Low Bandwidth</td>
</tr>
<tr>
<td>Narrow operating range</td>
<td>Ideal for digital load supporting DVFS</td>
</tr>
</tbody>
</table>

Ideal for supply sensitive analog load

Ideal for digital load supporting DVFS
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All-Digital Discrete Time LDOs

128 – Bit Bidirectional Barrel Shifter with built in Programmable Gain and Fine Grained Clock Gating

- IBM 130nm Process
- $V_{IN} = 1.0V - 0.50V$
- $V_{OUT} = 0.9V - 0.45V$
- Max $I_{LOAD} = 5mA$

- Fully digital and synchronous design with variable gain control through a 128-bit barrel shifter
- Fine-grained clock gating reduces 30% of controller power
- Clocked comparator input provides high input gain.

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Enhancing Transient Performance

- Higher CLK Frequency & Gain for large load steps enable RDS
- An externally programmable \( \Delta \) (nominally 50mV) and fast, transient clocks (nominally 400MHz) are employed.

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Reduced Dynamic Stability (RDS)

- RDS results in 8x improvement in measured settling time.
- RDS reduces the voltage droop in response to a load step by as much as 60%.

[8] ISSCC 2015
Origin of Limit Cycle Oscillations
- Quantization of the control loop at the comparator and at the output plant
- Relay based control is the key quantizing block in the loop

Control Principle and Modeling
- Describing function models the interaction of linear and non-linear components of the control loop

Key Results and Observations
- Increasing sampling frequency increases the mode of oscillation
- $F_{LOAD}/F_S$ needs to be bounded to limit output ripple

Increase in mode
- $I_{LOAD} = 2mA$
- $I_{LOAD} = 100\mu A$

[16] APEC 2015
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Conventional LDOs with Two Loops

- Fast transient loop
- Slow reference tracking loop
- Limited large signal performance
- Slew limited for large current transients
Switched Mode Control (SMC) LDOs

Operation Divided on Voltage Error ($V_{REG} - V_{REF}$)

Dual Loop Switched Mode Hybrid Control

- Two loops separated not in frequency, but in time (or voltage error)
- Good small signal performance (analog loop)
- Fast large signal performance (digital controller)

[18] ESSCIRC 2016

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Optimality in SMC LDO Designs

SMC Design Principle

- **Large transients (|V_{OUT} - V_{REF}| > \Delta):**
  - Place poles in unshaded region for faster rise time (Underdamped)
- **Near regulation (|V_{OUT} - V_{REF}| < \Delta):**
  - Place poles in shaded region for faster settling (Overdamped)
Three stage output-pole dominant analog small signal regulator

Input transconductance stage is followed by a shunt feedback buffer, pushes internal poles to high frequency (100s of MHz)

- IBM 130nm Process
- \( V_{IN} = 1.2V -0.60V \)
- \( V_{OUT} = 1.0V -0.5V \)
- Max \( I_{LOAD} = 12.6mA \)

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[18] ESSCIRC 2016
Key Measurement Results

- SMC enables us to synthesize a system with near-optimal droop response over a large load range.
- Optimal $\Delta$ of 90mV is measured.
- Transient rise time of 18ns is measured for a load step of >10mA.
# Summary: All-digital and Hybrid SMC LDOs

<table>
<thead>
<tr>
<th>All-Digital Loop</th>
<th>Hybrid SMC Loop</th>
</tr>
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<tbody>
<tr>
<td>+Wide operating range</td>
<td>+Excellent small signal gain and performance</td>
</tr>
<tr>
<td>+High current efficiency with adaptive control</td>
<td>+No ripple</td>
</tr>
<tr>
<td>+Low-overhead adaptation with clock control</td>
<td>+Fast transient response with high speed digital loop</td>
</tr>
<tr>
<td>+Fast transient response enabled by RDS</td>
<td>+Output pole dominant analog</td>
</tr>
<tr>
<td>-Output ripple</td>
<td>-Limited operating range</td>
</tr>
<tr>
<td>-Limited small signal performance</td>
<td>-Lower current efficiency</td>
</tr>
<tr>
<td>-Limited Clock Frequency</td>
<td>-Not synthesizable</td>
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Unifying LDO VR and Clocking

SoC PM Vision

Loop Transfer Characteristics

- The local clock and the local supply are generated from the same control loop
- Clock jitter correlated with $V_{\text{REG}}$
- No small signal sensing

TRC VCO and Load Circuits

Tunable Replica Circuit VCO
- Composed of logic and interconnect dominant paths
- Programmable to tens of ps resolution
- Non-inverting path closed via level shifting inverter to create a tunable VCO

Prototypical Load Circuit
- Three stage pipeline with built in self-test
- Error Detection Sequentials to detect timing errors
- High-speed noise generator replicates power state transitions
Key Measurement Results

- IBM 130nm Process
- $V_{\text{IN}} = 0.1V - 0.6V$
- $V_{\text{REG}} = 0.81V - 0.27V$
- $F_{\text{REF}} = 10 - 500MHz$
- Max $I_{\text{LOAD}} = 2.5mA$

- TRC VCO always tracks $V_{\text{OUT}}$
- Frequency & amplitude independent Clock-Data compensation
- Controller current scales with logic frequency and provides high current efficiency
Response to Voltage Droops

- 3mA load step applied here
- $V_{REG}$
- REF CLK: $F_{REF} = 200\text{MHz}$
- Pipeline Error: Pipeline Errors Detected
Response to Voltage Droops

- **V_{REG}**
  - 3mA load step applied here
  - 50ns

- **REF CLK**
  - \( F_{REF} = 200 \text{MHz} \)
  - Pipeline Errors Detected

- **Pipeline Error**
  - Pipeline Errors Detected

- **V_{REG}**
  - 155mV
  - 50ns

- **Local CLK**
  - \( F_{INSTANTANEOUS} = 98 \text{MHz} \)
  - \( F_{STEADY-STATE} = 200 \text{MHz} \)

- **Pipeline Error**
  - 0V
  - No pipeline Error Detected
Resiliency through UVFR Design

- UVFR allows co-regulation of the load supply and the local clock frequency
- A maximum reduction of 27% of voltage guard-band is measured at 10MHz

Summary: Continuous Time LDOs

Phase Based Design
+ Continuous time control
+ Designed with digital gates only
+ Low-overhead multi-phase design
+ Fast transient response and no ripple

- Larger area and controller power
- Limited bandwidth (dominant pole at the origin)

Unified Voltage and Frequency Regulation
+ Single loop control for both supply and clocking
+ Local clock tracks dynamic variations; no timing error

- Droop response limited by the reference frequency
Conclusions

- Digital LDO regulators demonstrate
  - Low Operating Voltage (to NTV) & Low Dropout Voltage (~50mV)
  - Fast Transients with DVFS Support for Digital Load Circuits

- Switched Mode Control (SMC) allows
  - Excellent Small Signal Analog Performance
  - Fast Transient Response enabled by the Digital Loop

- Phase Based regulation allows ripple free operation

- UVFR allows voltage-clock co-regulation and reduction of voltage guard-band in digital load circuits
  - Further demonstrations of UVFR in buck converters (ISSCC 2019 paper with Qualcomm)
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