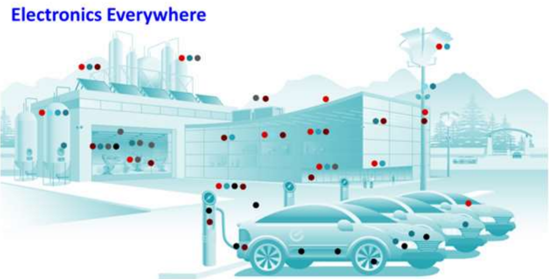
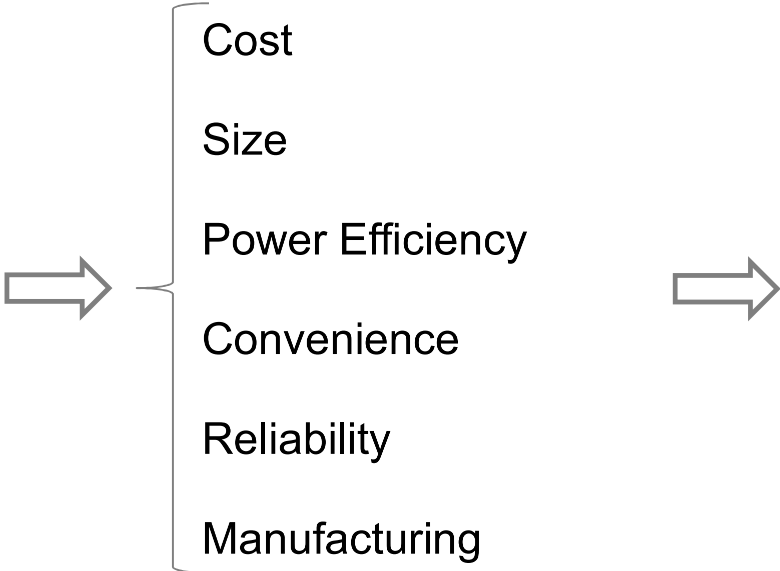
Packaging As a Power Density Enabler

Dr. Sreenivasan Koduri
Texas Instruments Inc.

Oct-2018
KK

Problem Statement:



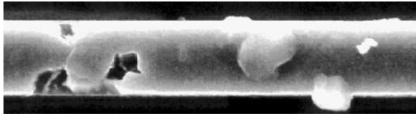


Power Density
(more power/current in smaller area)

Temperature

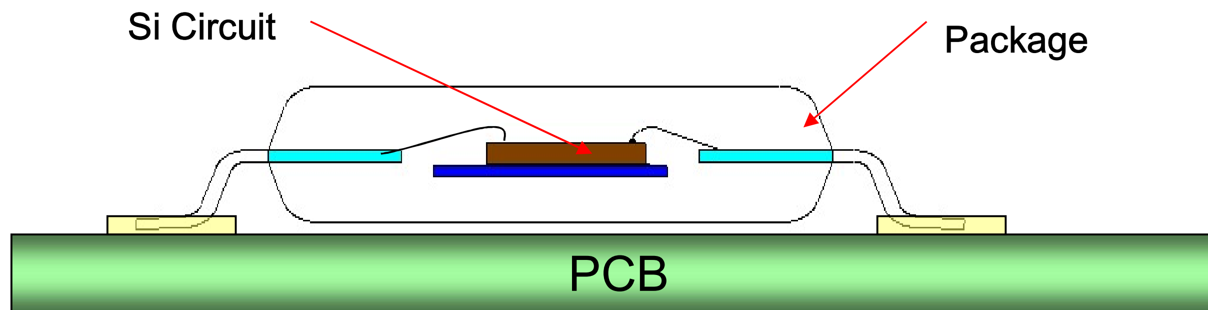
Electromigration

Temperature and EM are shared problems across the system, die, and package.



EM aging
(voids and hillocks)

Purpose of the Package:



- Interconnection between Si and PCB
- Protection and durability of IC
- Defines the size and form factor of the device
- Enables thermal dissipation

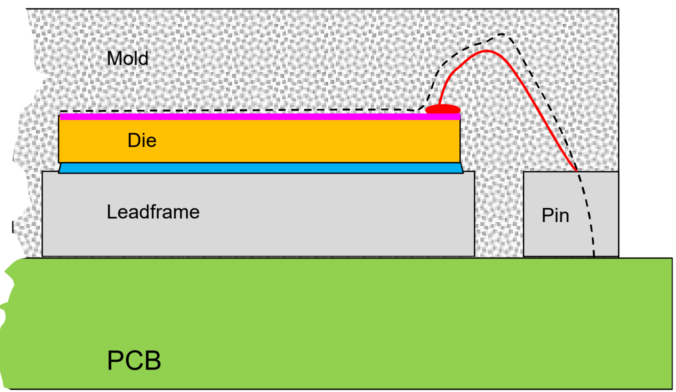
Traditional

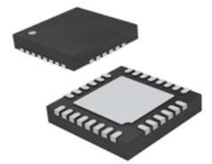
- Enable device functionality
- Improve electrical and thermal specs
- Simplify the device development
- Ease of use

Expanded

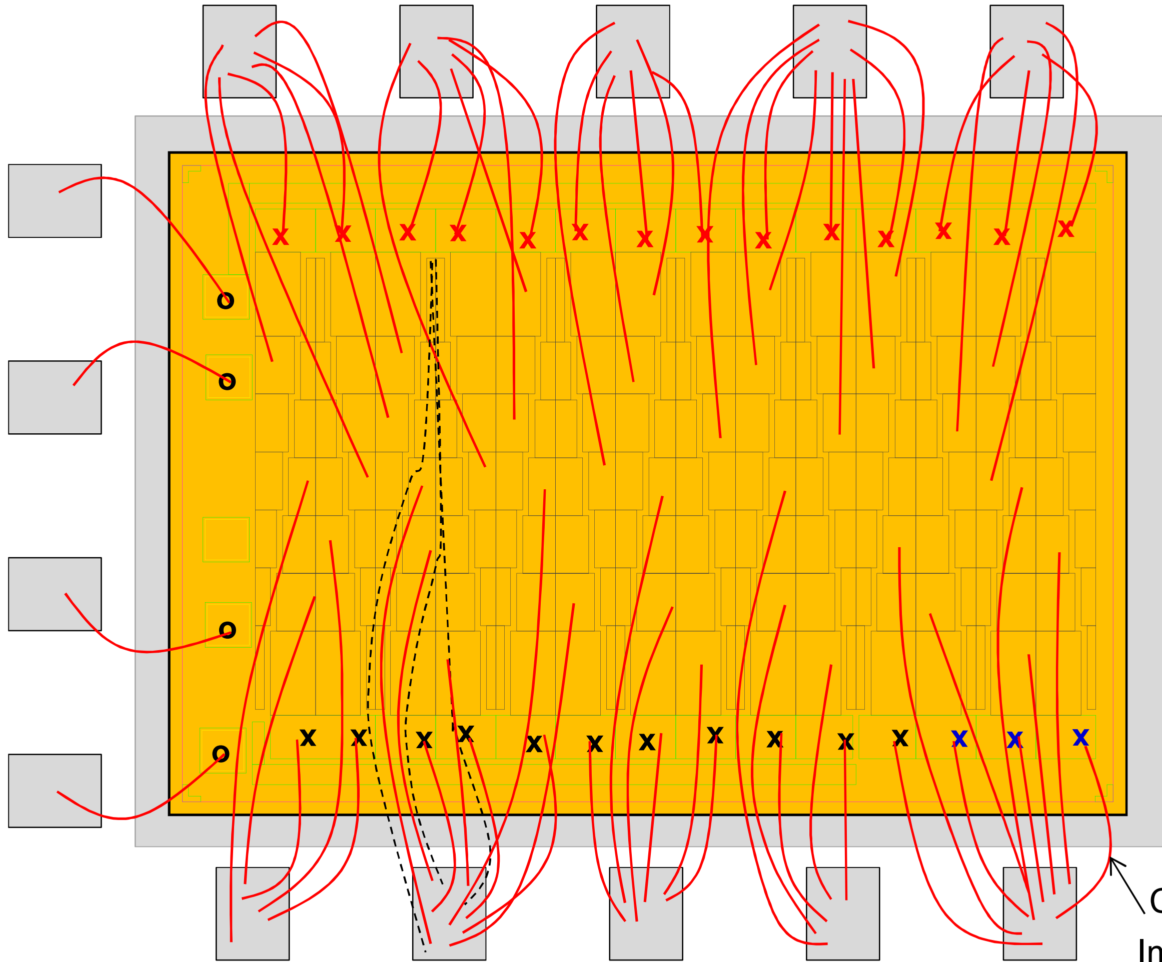
Prior Layout : Typical Power Device

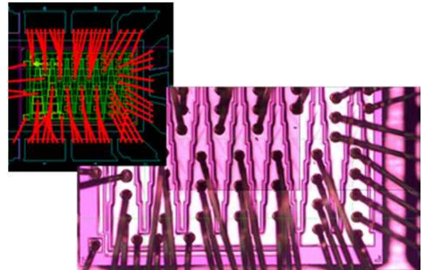
Gold Wire bonds

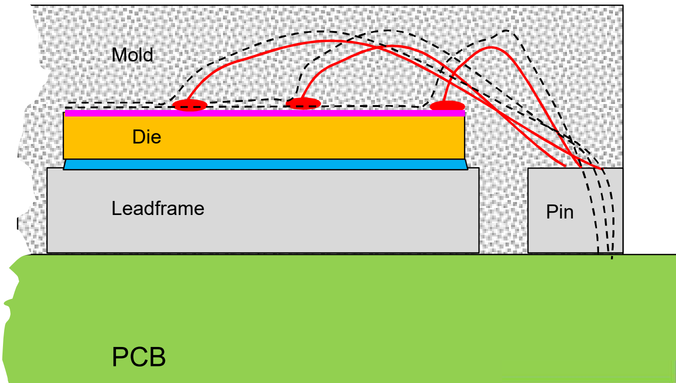




Enhanced Layout : Cu Wire + Gang/Core Bonding.

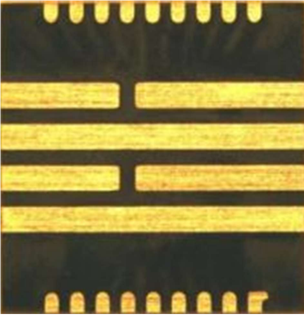



Lobster
TPS51315

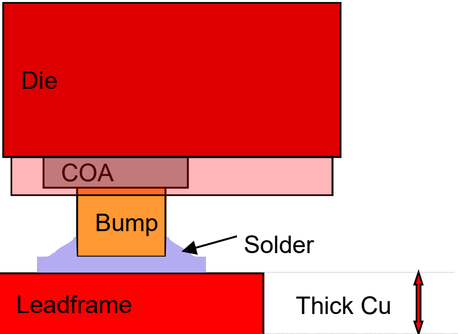


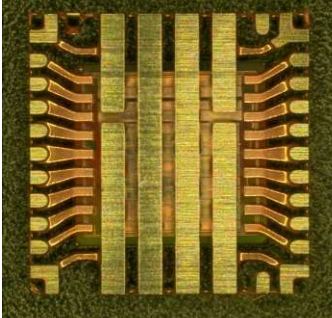
Copper Wire bonds
Improved Cost, RDSon, and EM

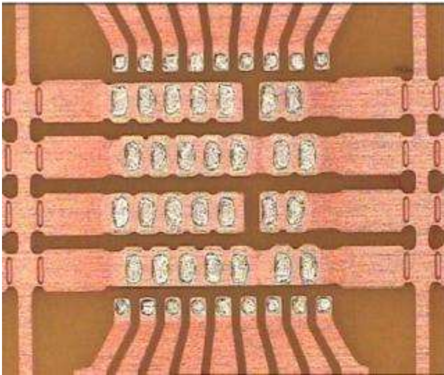
HotRod™ Package: Construction

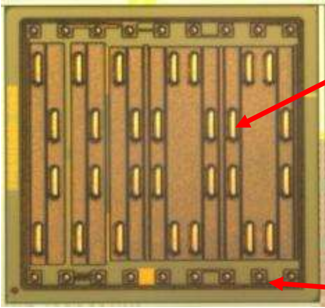

Package Bottom

Significantly Reduces PackageResistance



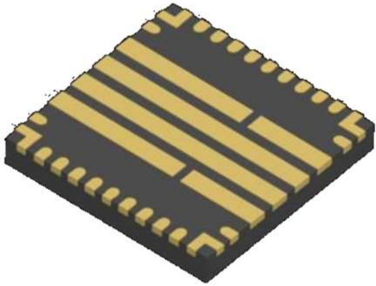

Leadframe & Die Attached


Leadframe

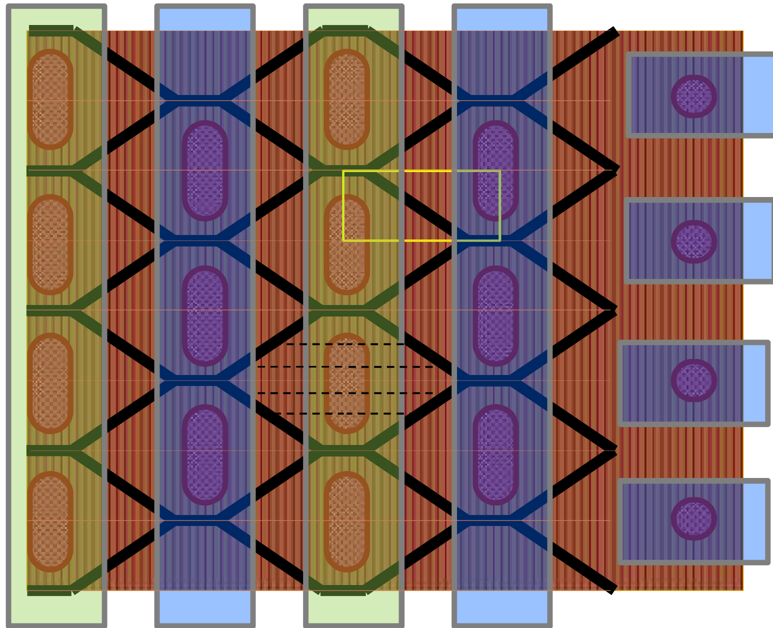

Cu bumps on die

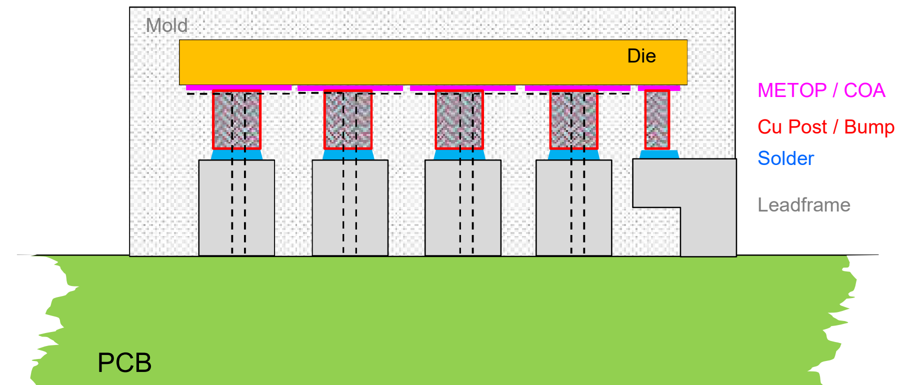
For Power Pins

For Signal Pins

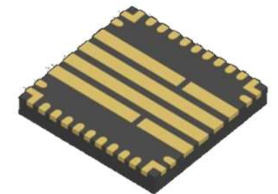

Encapsulated Package

Innovative Layout: HotRod™ Package

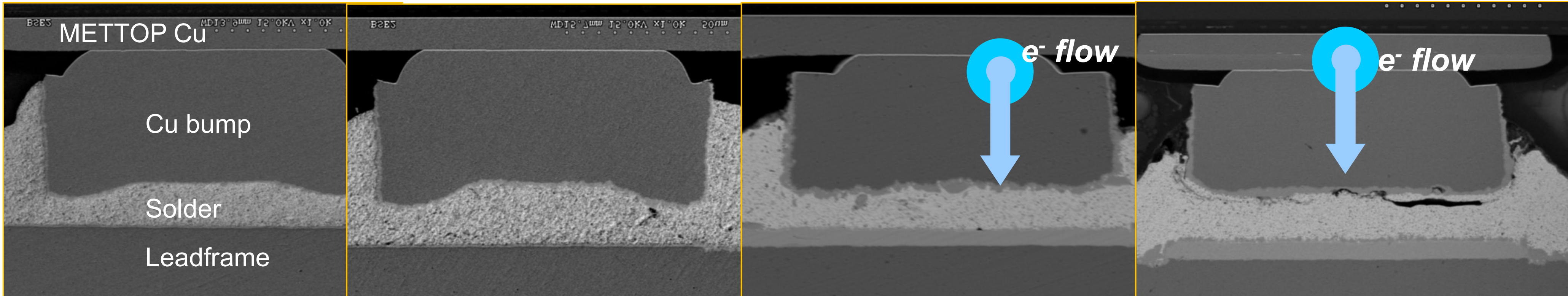




- Replace wire bonds with Cu posts and use leadframe to route power.
- Significantly reduces RDSon (Die and Pkg).
- Enables efficient FET layout and shrinking of die



Power Density: Electromigration



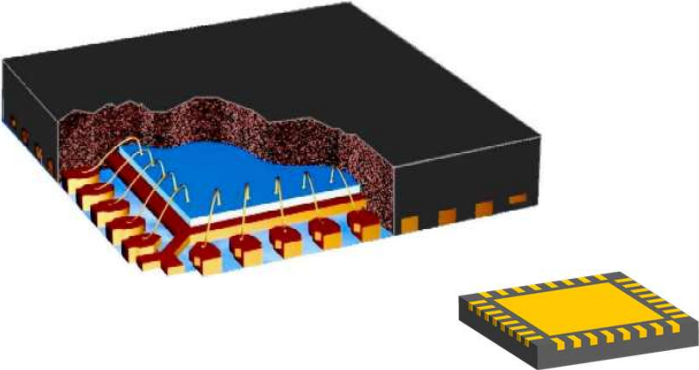
- Cu depletion and solder voiding observed with EM void propagation at Cu-Solder interface.

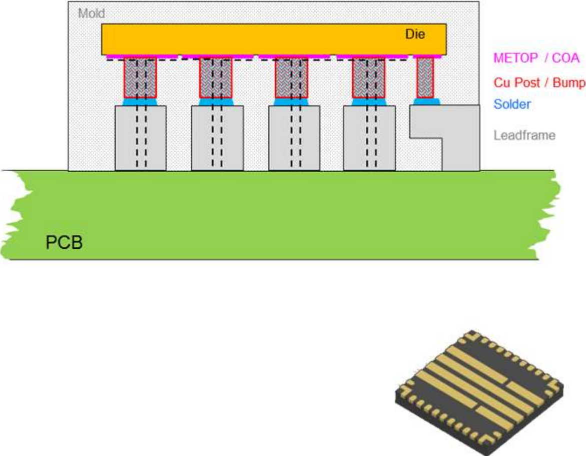
Black's Equation for EM:

$$\text{MTTF} = \frac{A}{J^2} e^{\left(\frac{1}{kT}\right)}$$

A is a constant
J is the current density
k is Boltzmann's constant
T is the absolute temperature in K

Power Density: Thermal Challenges



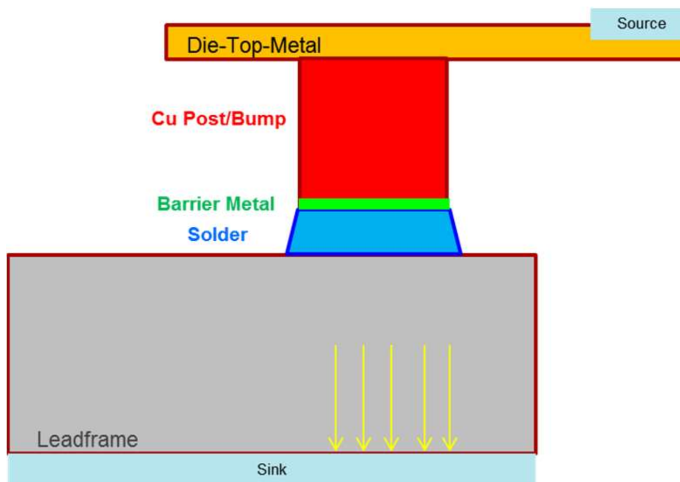


- Reduces thermal contact area from die to the PCB
- Current/Thermal hot spots in the interconnect

Power Density: Potential Solutions

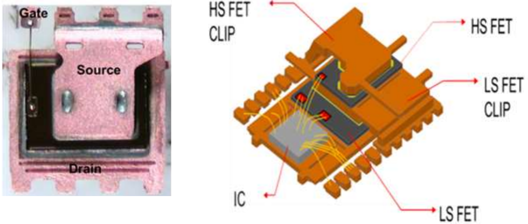
- Barrier metals such as Ni or NiW can slow Cu-Si metal diffusions.
  - Can withstand higher temperatures and current density.
  - Can increase product life while increasing power specs.

- Thermal problems can be addressed with enhanced materials, board design and heatsinking.

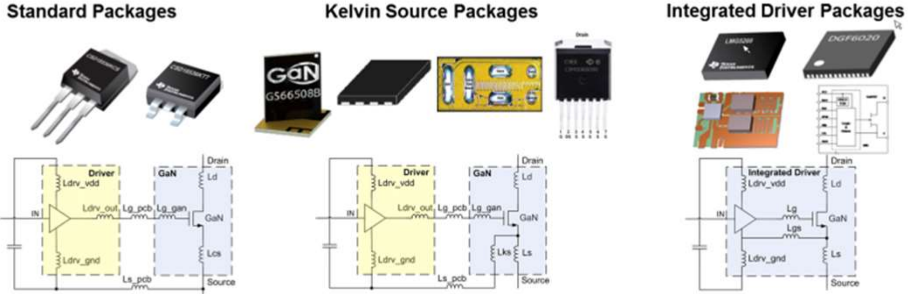


Power Density: Potential Solutions

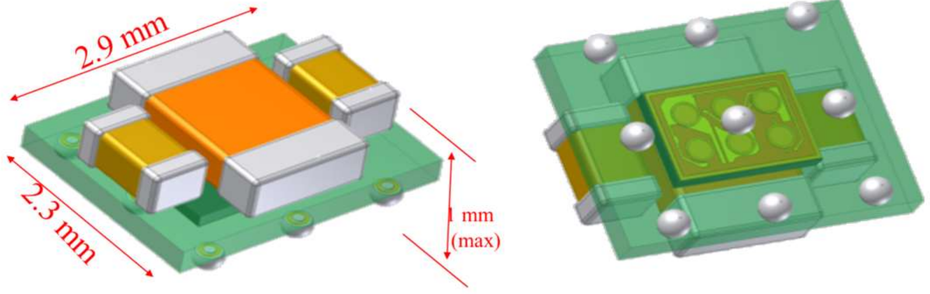
- For discrete FETs, Cu clips are a great solution to address thermal and current densities. These solutions may not scale for integrated LDMOS ICs.

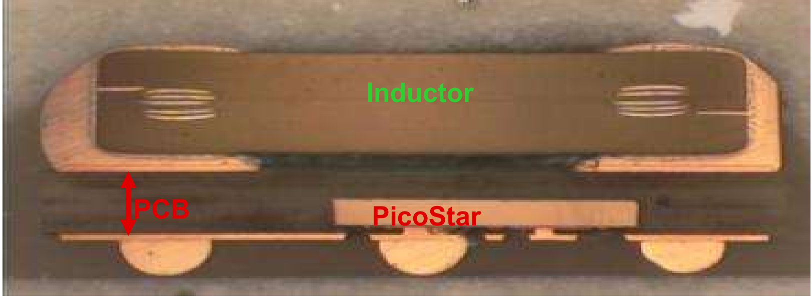


- With the faster switching needs of wide-bandgap (GaN and SiC) products, package inductance becomes an additional challenge. This requires creative solutions with Kelvin pins, or dual-cool QFNs, and/or driver integration.

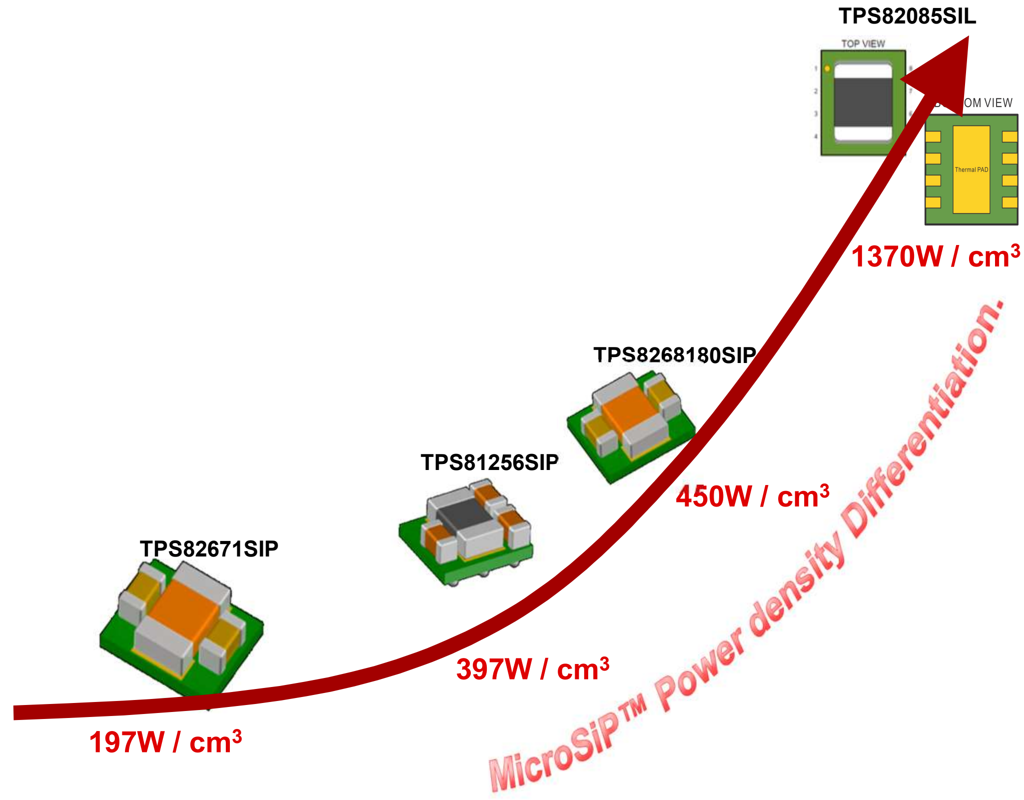


Embedded modules





- Integrating passives close to the ICs, at a package/module level can improve power efficiency and increase power density at system level.
- Embedded packages such as MicroSiP™ can eliminate solder in the interconnect between die and package, while enabling passives integration.



Summary

- Package plays a big role as the power densities increase.
- It takes a range of solutions to address the differing needs.
- Have to co-design the system, die and package for best results.

Thank You !