Low profile & Multi-term Silicon Capacitors

PowerSoc 2018

Murata Integrated Passive Solutions
Frédéric Nodet

Outline

- MIS introduction & PICS technology
- Trends & Roadmap　Low profile & Low-ESL
- Murata Multi-term Silicon capacitors
- ESL of multi-term Silicon capacitors
- Summary

Company name

Murata Integrated Passive Solutions S.A.

April 2017

Murata Integrated Passive Solutions

- Part of Murata since October 2016
- Murata Integrated Passives division
- Manufacturing, R&D and Innovation center

Europe (14)
The Netherlands
Finland ▲●
France ▲●
Germany
Hungary
Italy
Spain
Switzerland
United Kingdom ●

Americas (11)
United States ▲●
Brazil
Canada ●
Mexico

Japan (31) ▲●

Greater China (29) ▲●

Asia and others (15)
Singapore ▲
India
Malaysia ▲
Philippines ▲
Thailand ▲
Vietnam

(No of companies)
Regional Head Offices
▲ Production plants
● R&D Centers

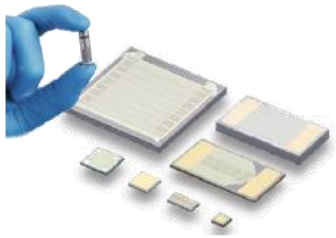
**Murata Manufacturing Co., Ltd. is not included in the number of subsidiaries*

MIS introduction
PICS technology

What is Silicon capacitor?

Key Feature

500 nF/mm²
Miniaturization
No cap degradation

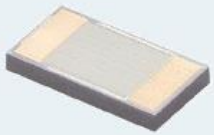
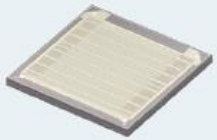
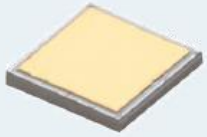
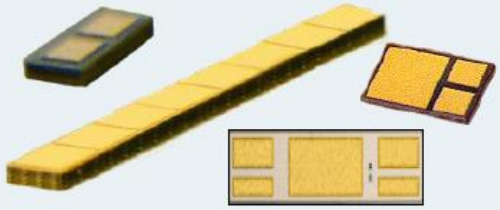
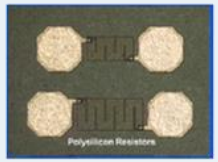


80 µm
Ultra low profile

Up to 100 GHz
Broadband performance
Ultra low insertion loss

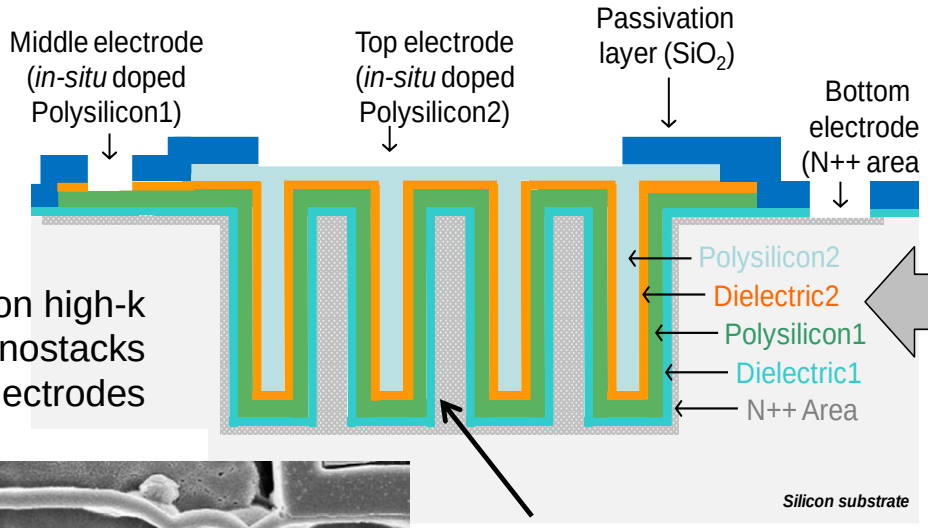
Up to 250ºC
High Reliability
Stable Life

Si Capacitor - Product Type

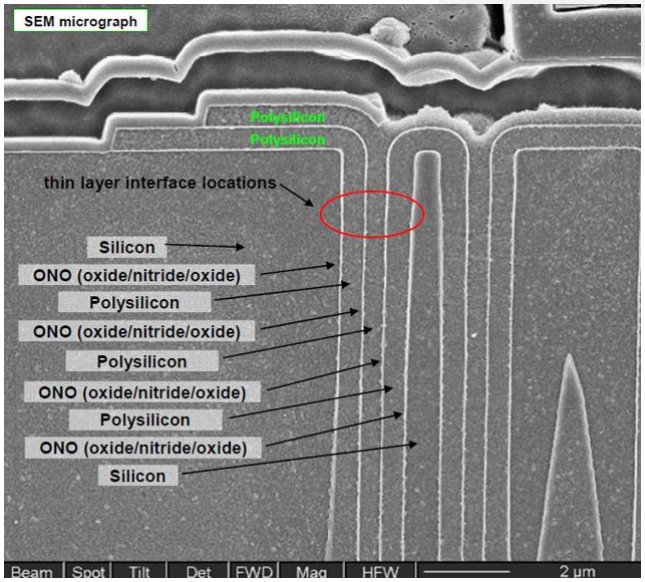
Off-the-Shelf			Customized Solution	
Solder mounting	Wire-bonding / Embedded	Wire-bonding	Capacitor Array Binary Capacitor	IPD (Integrated Passive Device)
				
2 terminal	4 terminal	Vertical		Capacitor + Resistor

3D structure

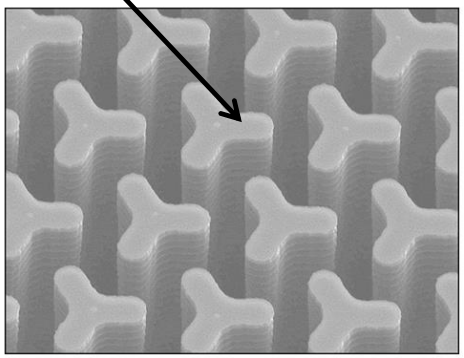
2 parallelized capacitors in a MIMIM architecture to increase the capacitance value

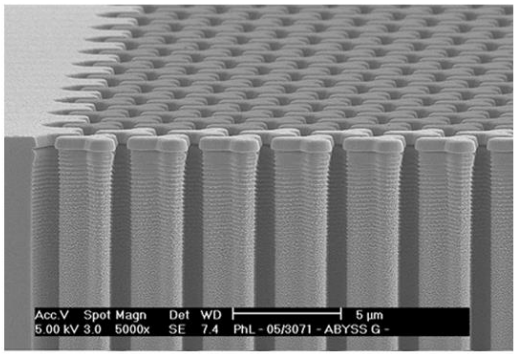


Based on high-k materials nanostacks & barrier electrodes



Tripod

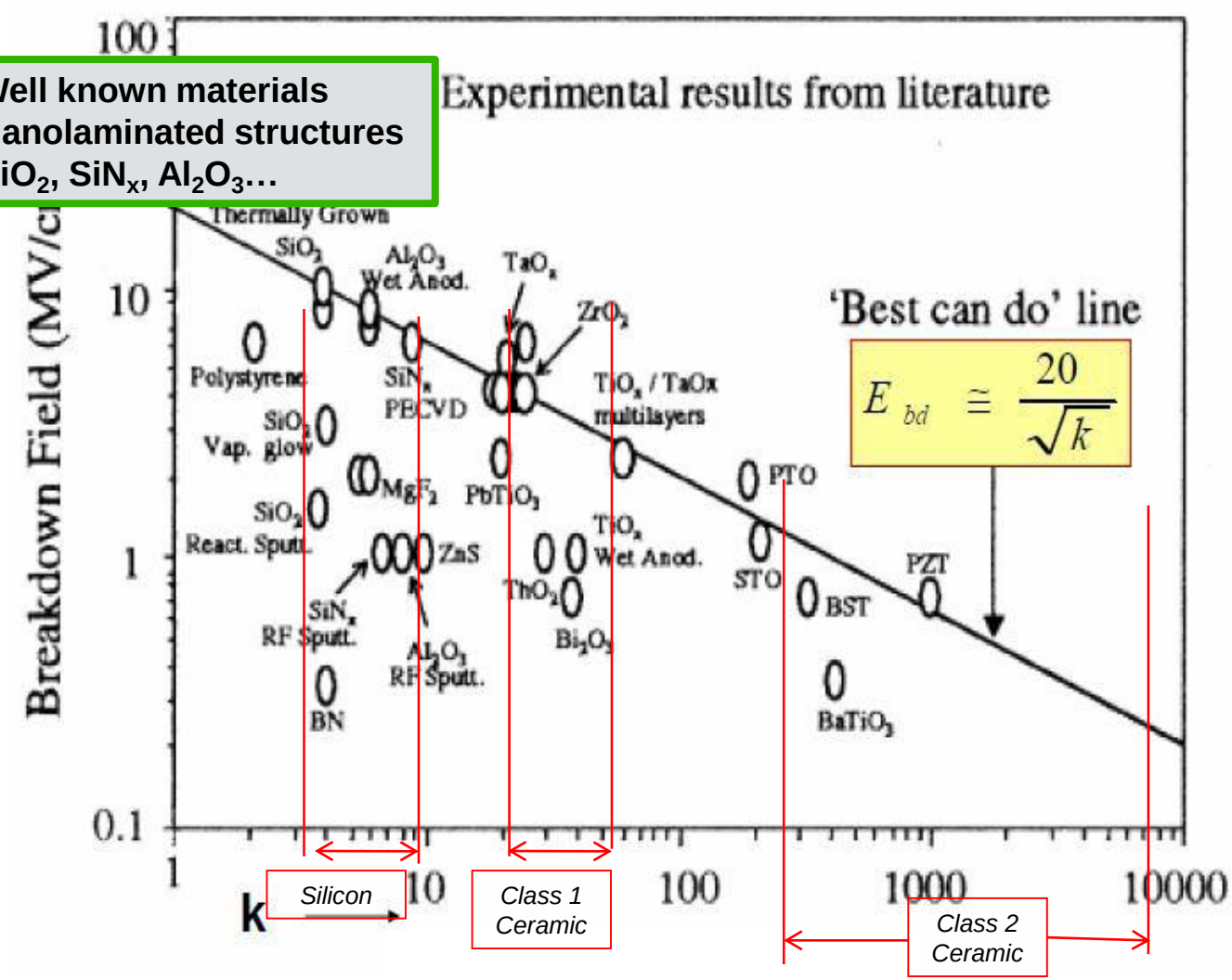




Tilted SEM view

Dielectric materials

Well known materials
Nanolaminated structures
SiO_2, SiN_x, Al_2O_3…



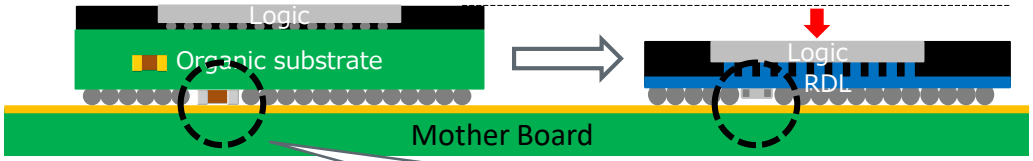
Relative permittivity as a function of Breakdown field

Trends & Roadmap

Low profile & Low-ESL

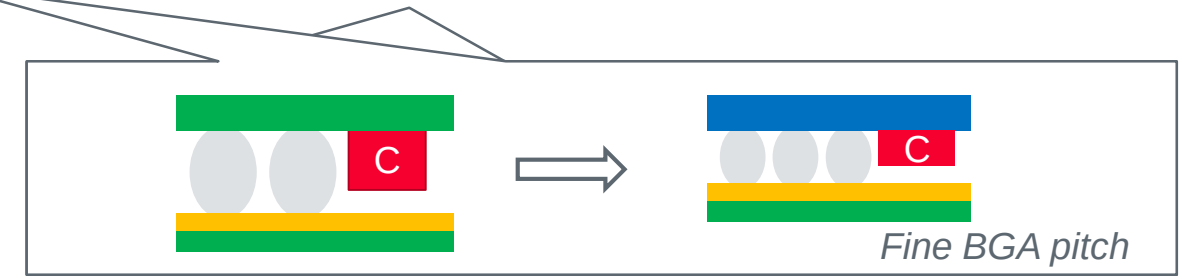
Trends of IC package & Package capacitor

Thickness



FOWLP / FOPLP

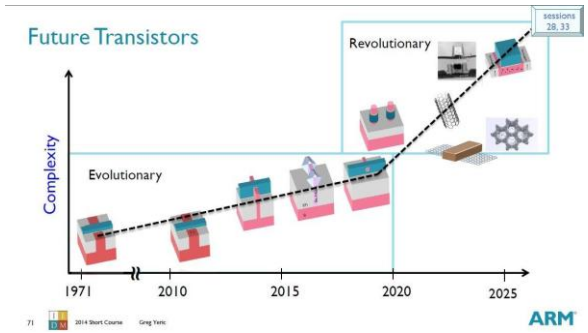
- *Fine L/S (→ Fine BGA pitch)*
- *Low profile*



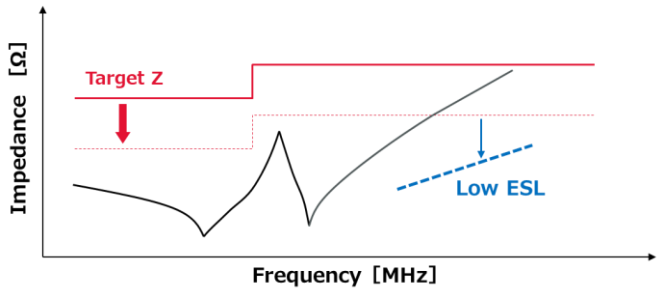
Low profile capacitor is needed

ESL

Microfabrication of process ⇒ Lower target impedance



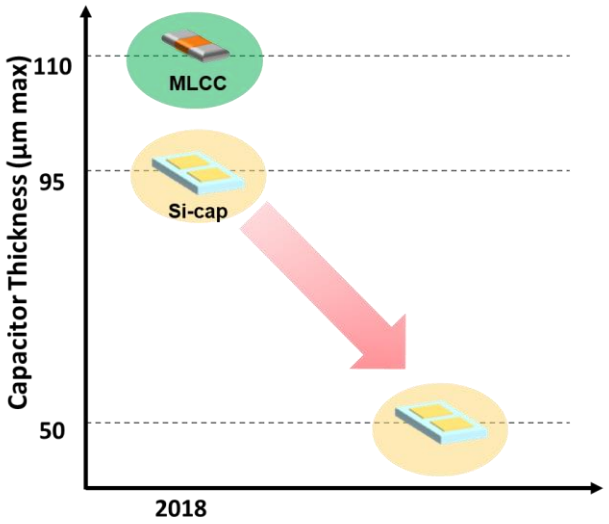
10 nm → 7 nm → 5 nm…



Low ESL capacitor is needed

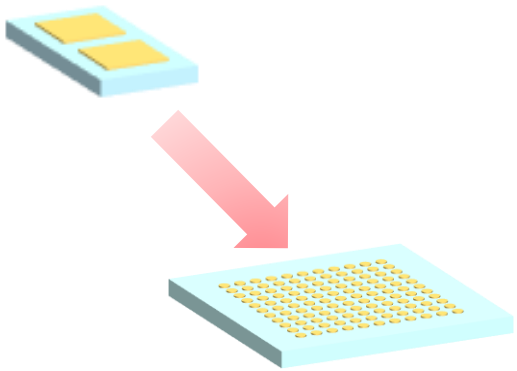
Advantage of Silicon Capacitor

- Low profile



- *Achieve low thickness (~ 50 µm)*
- *Higher robustness*

- Multi-terminal

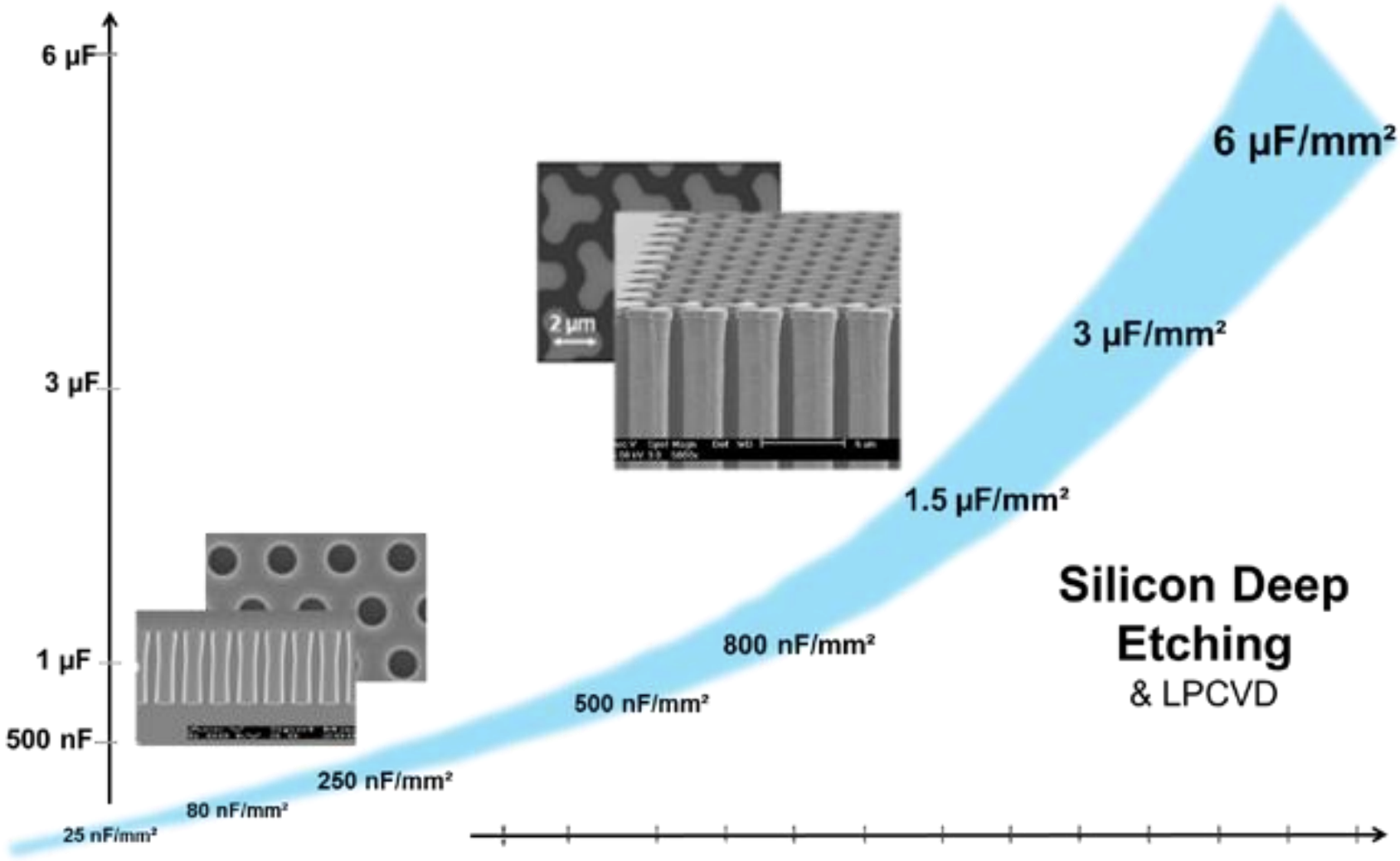


- *Design many terminals on capacitor*

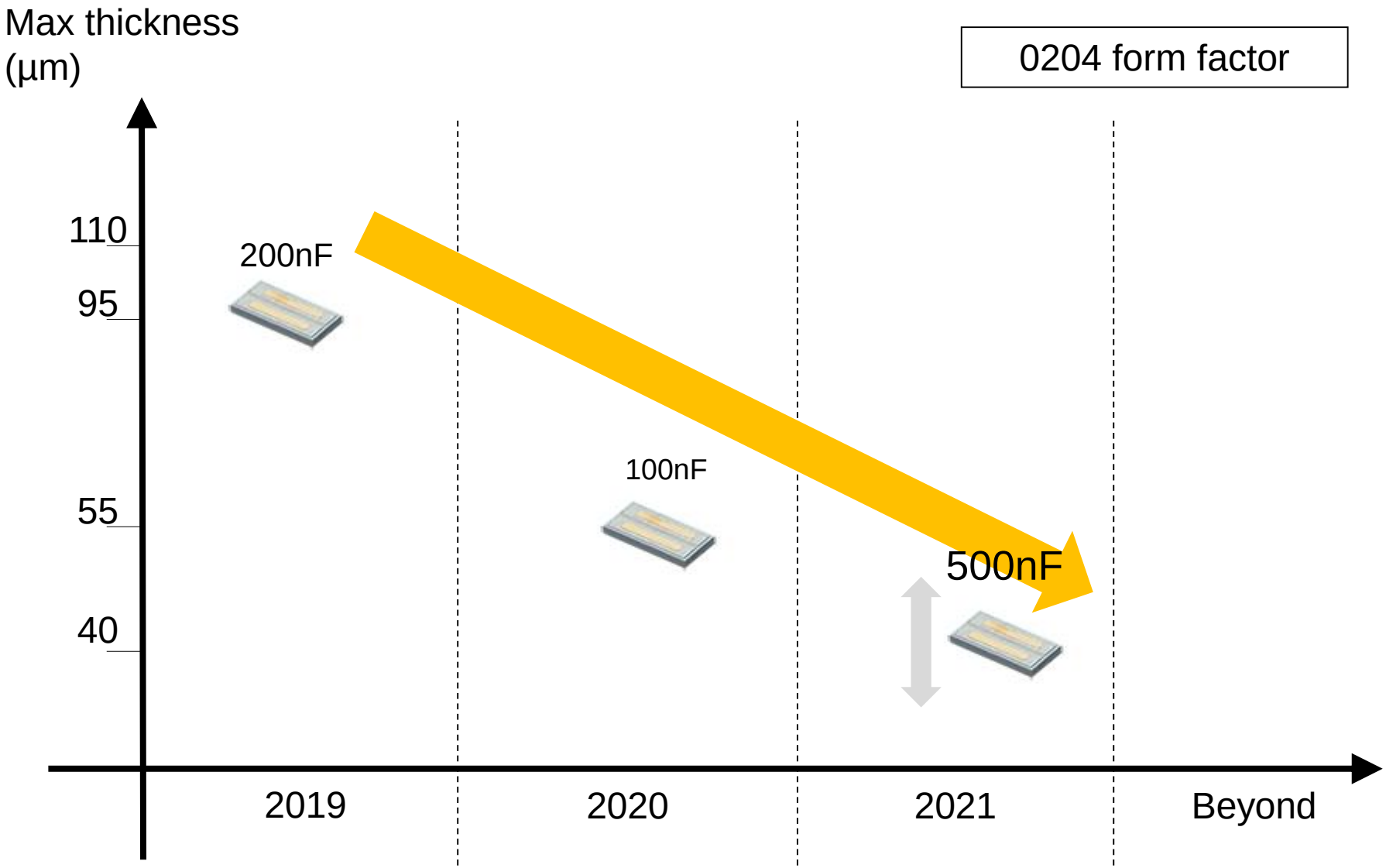
Extremely low ESL < 10pH

Silicon capacitor is good answer for PKG capacitor!

Low voltage technology roadmap

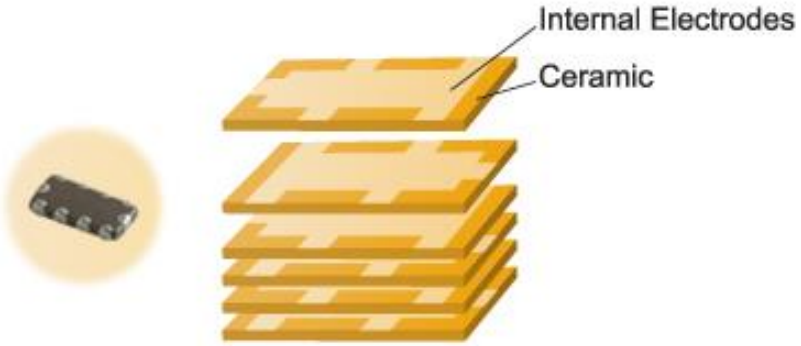


UESL Capacitor Roadmap

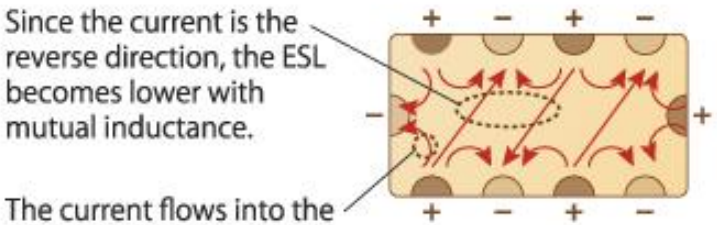


Murata Multi-term Silicon capacitors

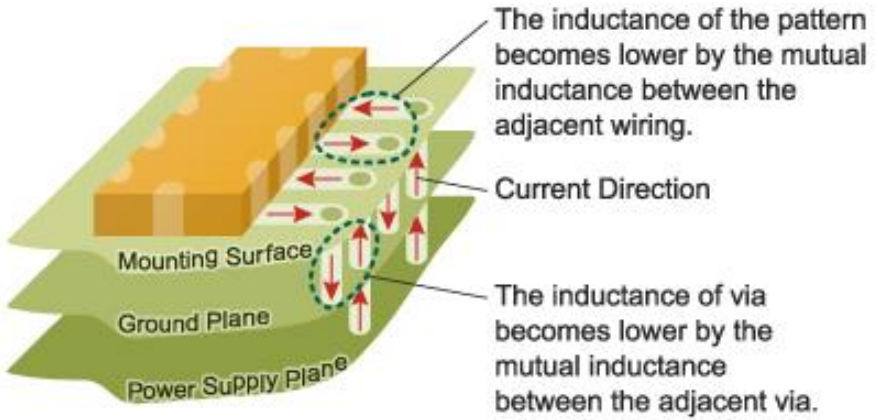
Murata Multi-term MLCC capacitor



<Example of Structure>



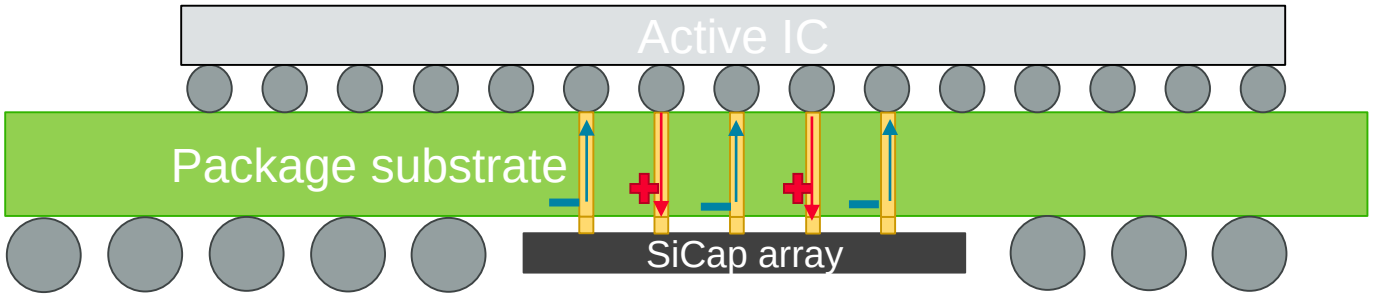
Effectiveness of Cancelling Out Inductance by Mutual Inductance



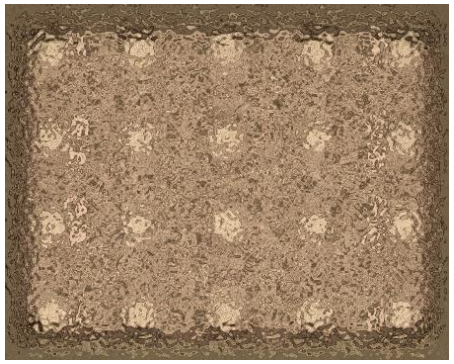
Effectiveness of Suppressing Inductance when Mounting a Multi-terminal Capacitor

The inductance for the boards also becomes lower, not only the capacitor.

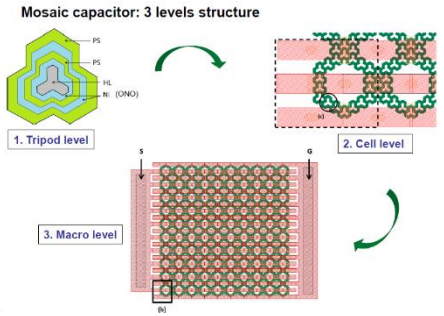
Murata's Multi-term Silicon capacitors



Typical Assembly Schema - Cross section view



Murata Multi-terminal Si Cap - Top view



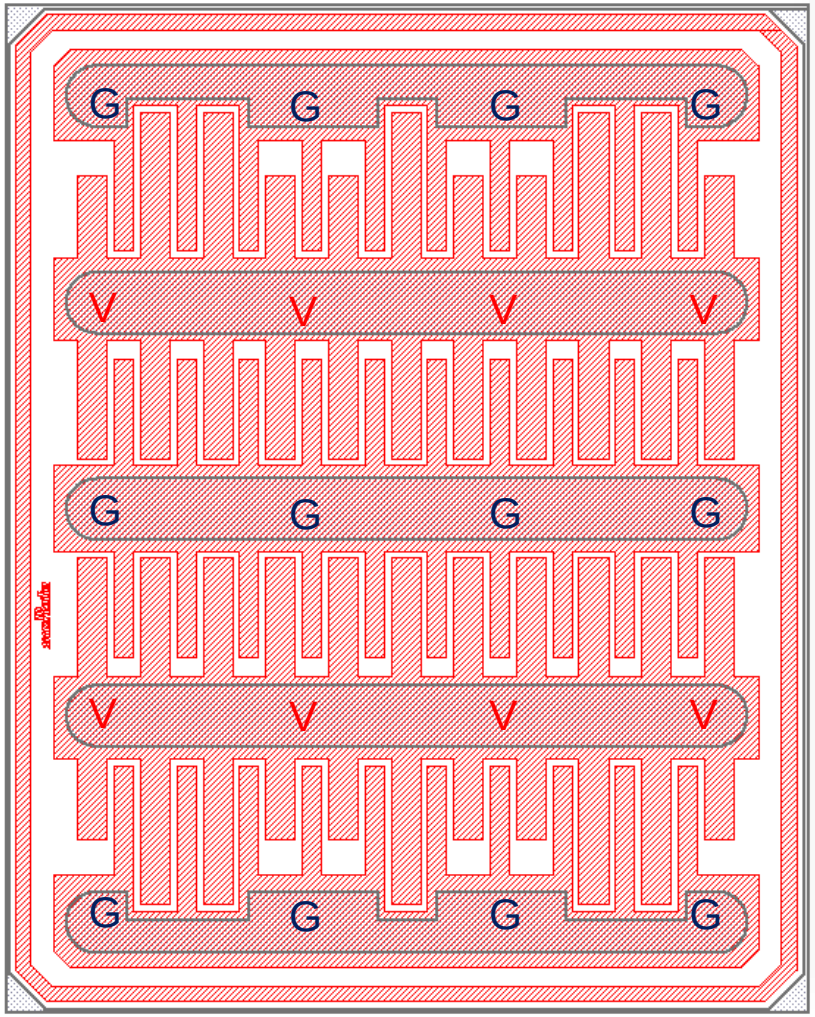
EP 3297024A1
3D Capacitor structure

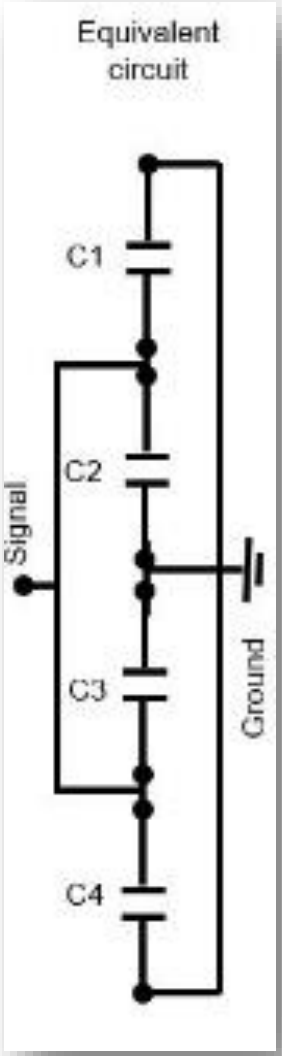
- Use of Mosaic Architecture → Lowest obtainable ESL and ESR by internal design
- Preserving the Low ESL and low ESR Through C4 solder bumps in flip-chip attachment → This offers the ultimate in low inductance since it results in many current injection points.
- This reduces the mutual inductance and minimizes the effective path length of the charging current.

Structure overview

- 20-pads Silicon cap
- 2 Signals rows
- 3 Ground rows

➔ 4 caps in //





ESL of Multi-terminal Silicon capacitors

ESL estimation flow

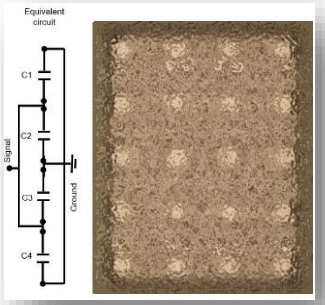
Theory

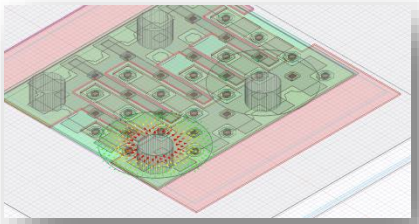
EM Simulations

Measurements

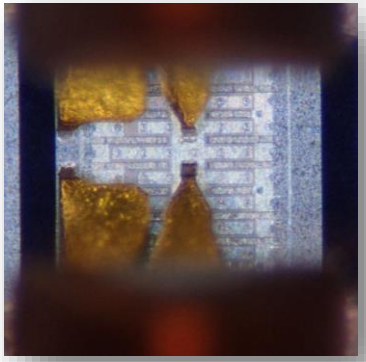
Basic calculation of ESL

$$L = 0.2 \cdot len \cdot \left(\ln\left(\frac{2 \cdot len}{(w+t)} \right) + \frac{0.223(w+t)}{len} + 0.5 \right)$$

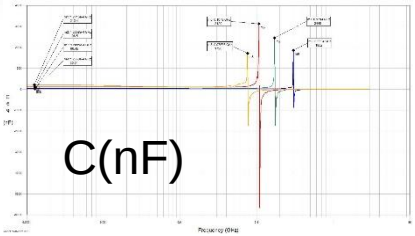


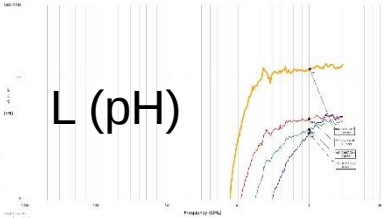


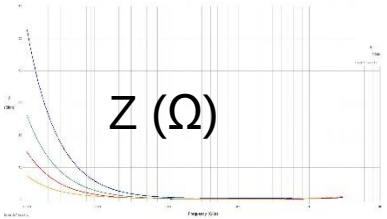
→ [S] Parameters



GS-SG Measurements





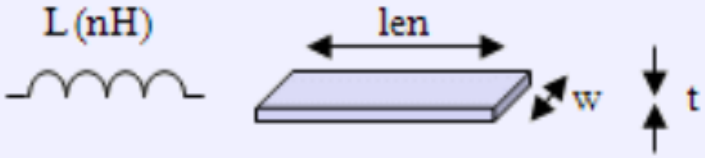


Theoretical calculation

- Basic model

Strap Inductance

Dimensional units: ◉ mm ○ mils

len (length) =	1
w (width) =	0.5
t (thickness) =	0.003
	Calculate
L (Inductance, nH) =	0.398

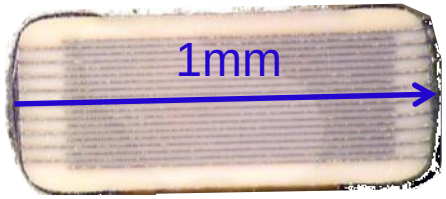
$$L = 0.2 \cdot len \cdot \left(\ln\left(\frac{2 \cdot len}{(w+t)} \right) + \frac{0.223(w+t)}{len} + 0.5 \right)$$

http://www.mantaro.com/resources/impedance-calculator.htm

ESL of 0402 & 0204 MLCC

- Typical 0402 ESL = 280pH [1]

https://product.tdk.com/info/tvcl/ecm/mlcc_commercial_general_c0402_ecm.pdf



Strap Inductance

Dimensional units: ◉ mm ○ mils

len (length) =	1
w (width) =	0.5
t (thickness) =	0.5
L (nH) len w t	Calculate
L (Inductance, nH) =	0.283

$$L = 0.2 \cdot len \cdot \left(\ln\left(\frac{2 \cdot len}{(w+t)} \right) + \frac{0.223(w+t)}{len} + 0.5 \right)$$

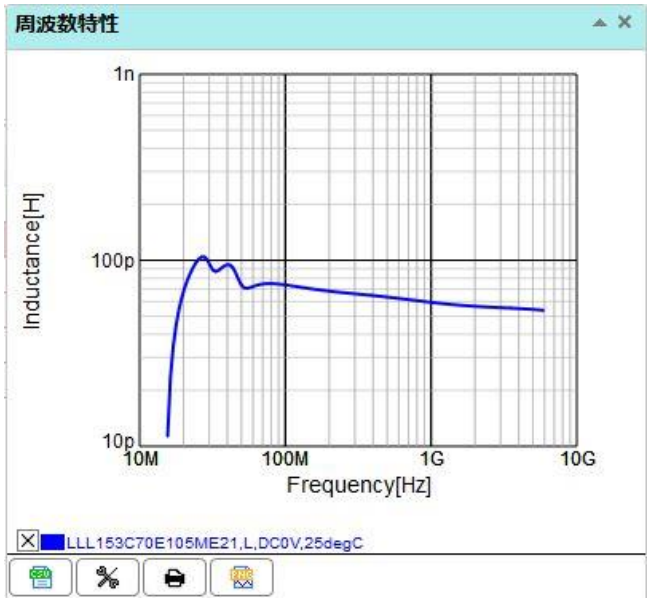
- 0204 ESL T=0.35mm

Strap Inductance

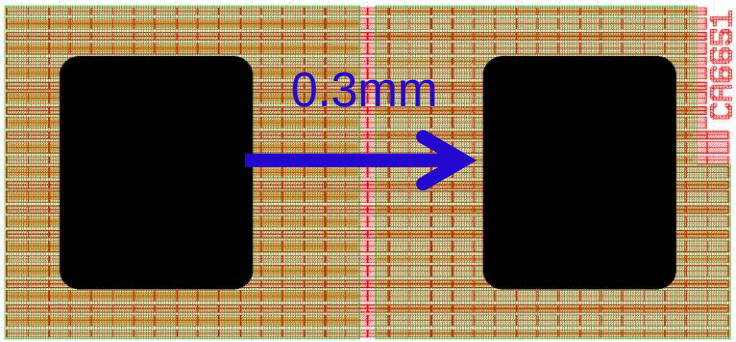
Dimensional units: ◉ mm ○ mils

len (length) =	0.5
w (width) =	1.0
t (thickness) =	0.35
L (nH) len w t	Calculate
L (Inductance, nH) =	0.080

$$L = 0.2 \cdot len \cdot \left(\ln\left(\frac{2 \cdot len}{(w+t)} \right) + \frac{0.223(w+t)}{len} + 0.5 \right)$$

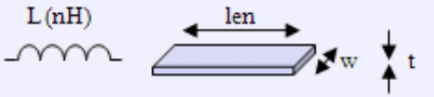


ESL of 0402 & 0204 SiCap



Strap Inductance

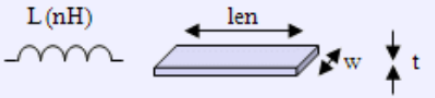
Dimensional units: ◉ mm ○ mils

len (length) =	0.3
w (width) =	0.5
t (thickness) =	0.003
L (nH) 	Calculate
L (Inductance, nH) =	0.063

$$L = 0.2 \cdot len \cdot \left(\ln\left(\frac{2 \cdot len}{(w+t)} \right) + \frac{0.223(w+t)}{len} + 0.5 \right)$$

Strap Inductance

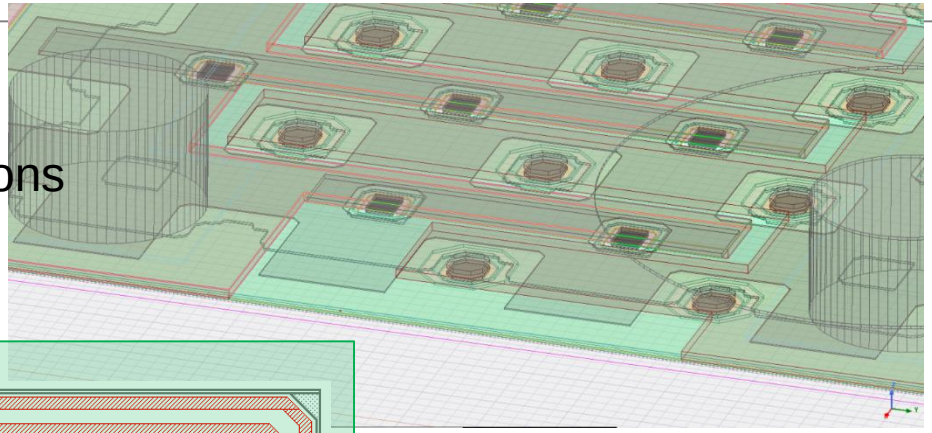
Dimensional units: ◉ mm ○ mils

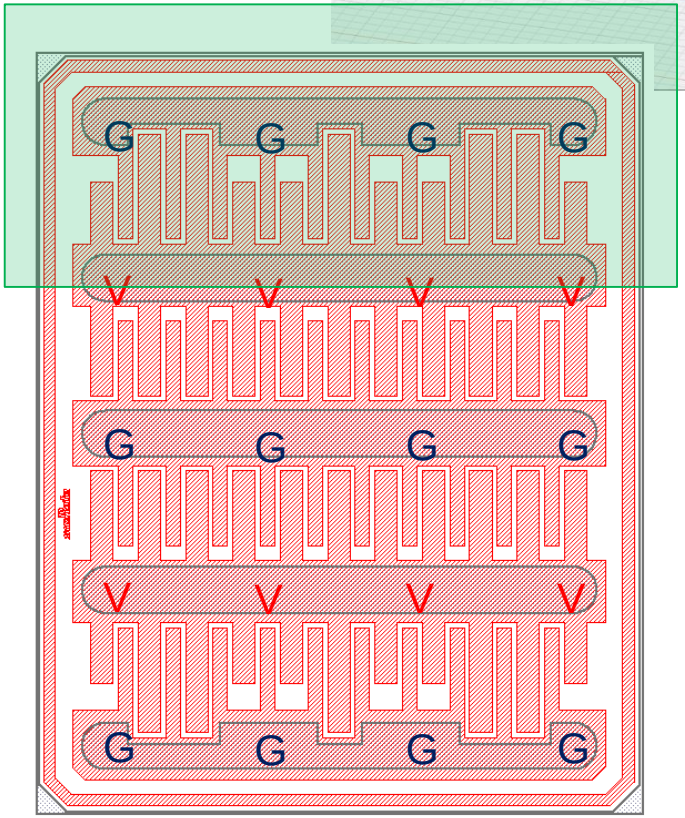
len (length) =	0.2
w (width) =	1
t (thickness) =	0.003
L (nH) 	Calculate
L (Inductance, nH) =	0.028

$$L = 0.2 \cdot len \cdot \left(\ln\left(\frac{2 \cdot len}{(w+t)} \right) + \frac{0.223(w+t)}{len} + 0.5 \right)$$

ESL of multi-term SiCap (on-going work)

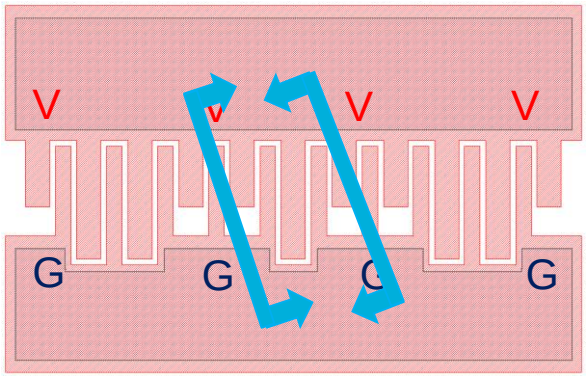
1/4 structure
HFSS Simulations





Simulated
[S] param

GS-SG 1/4 structures
measurement



Measured
[S] param

GS-SG
1/4 structure

MATCH

If ok

x4

Product
[S] param

Summary

Silicon Capacitors addressing market trends

- Increased density
- Low thickness

0204 500nF 40um

- Multi-terminals Silicon Capacitors
  - Development on-going

  - ESL computation
  - Comparison *on elementary cell*
    HFSS simulation + Measurements
  - Generating product [S] param

Thank you!

www.murata.com