A 100MHz IVR PMIC with On-silicon Magnetic Thin Film Inductors

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## Current State of Inductor Based IVR Technology

- **Very small pool of participants (publically)**
  - Large funding & patience
  - Wafer fabrication infrastructure
  - Cross-discipline engineering team

- **Limited progress being reported since 2010**

- **Magnetic Thin-film Inductor IVR saves power, space and cost?**
  - Still a hypothesis to be proven

- **Efficiency— the biggest hurdle to convince customer**
  - 2 stage conversion vs. single stage
  - Thin film inductor efficiency @high frequency?

### Technology and Performance Parameters

<table>
<thead>
<tr>
<th>Core Material</th>
<th>Inductor Quality Factor</th>
<th>Fsw(MHz)</th>
<th>L(nH)</th>
<th>Vin(V)</th>
<th>Vout(V)</th>
<th>Peak Efficiency</th>
<th>Iout_max(A)</th>
<th>Conversion Ratio (Vout/Vin)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni80Fe20</td>
<td>NA</td>
<td>100</td>
<td>17</td>
<td>NA</td>
<td>NA</td>
<td>76%</td>
<td>&gt;4</td>
<td>NA</td>
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<tr>
<td>NiFe</td>
<td>~1.2*</td>
<td>75</td>
<td>5.9</td>
<td>1.8</td>
<td>1.1</td>
<td>74%</td>
<td>&gt;4</td>
<td>0.61</td>
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<tr>
<td>Air Core</td>
<td>NA</td>
<td>140</td>
<td>1.5</td>
<td>1.7</td>
<td>0.88</td>
<td>90%</td>
<td>700</td>
<td>0.50</td>
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<tr>
<td>NA</td>
<td>~3.8*</td>
<td>100</td>
<td>1.5</td>
<td>1.5</td>
<td>1.15</td>
<td>84%</td>
<td>0.42</td>
<td>0.66</td>
</tr>
<tr>
<td>NA</td>
<td>20</td>
<td>100</td>
<td>1.8</td>
<td>1.8</td>
<td>0.9</td>
<td>~78%</td>
<td>3A</td>
<td>0.5</td>
</tr>
</tbody>
</table>

### Process Technology

- **Inductor Technology**
  - Monolithic Strip-line Inductor
  - Interpose r /Strip-line Inductor
  - Package Inductor Air Core
  - Monolithic/ Solenoid Inductor
  - Monolithic/ Solenoid Inductor

### References

Integrated Power Delivery from More Moore Perspective

- Processor core counts continue scale up
- Supply voltage scaling down plateaued
- Thermal constrained power density limit → dark silicon
  - Portion of cores would be turned off at any given time
  - Dynamic and heterogeneous power/thermal management needed
  - Super-threshold and near-threshold domain coexist
- IVR becomes a must-have technology
  - Conventional VR is ill-suited for variety and granularity of voltage domains.
  - Minimizing voltage variation for timing convergence, i.e. thinking 50mV’s impact at 0.8V and 0.4V supply voltage, respectively.

### YEAR OF PRODUCTION

<table>
<thead>
<tr>
<th>2017</th>
<th>2019</th>
<th>2021</th>
<th>2023</th>
<th>2025</th>
<th>2027</th>
<th>2030</th>
</tr>
</thead>
<tbody>
<tr>
<td>P6M36</td>
<td>P6M28</td>
<td>P4K624</td>
<td>P3M621</td>
<td>P3M144</td>
<td>P2M41T2</td>
<td>P2M11T4</td>
</tr>
</tbody>
</table>

**Process Technology Node (nm):**

- Logic density: "Node Range" Labeling (nm)
  - 16/18
  - 14/15
  - 12.4/13.5
  - 11.5/11.8
  - 11.8/11.8

**KMD-Foundry node labeling:**

- 16/17, 17/15

**Logic device structure options:**

- finFET, FinFET
- LGA, LGA
- VGA, VGA

**Logic device mainstream device:**

- finFET, FinFET
- LGA, LGA
- VGA, VGA

**DEVICE STRUCTURES:**

- Logic device mainstream device
  - Power Supply Voltage (V)
  - Clock Rate (GHz)

**Core count needs for computing performance target:**

Due to thermal constraint, @fixed Vdd number of active cores = clock rate

2017 IRDS report
IVR from Power Delivery Perspective

- Conventional VR regulation bandwidth has no effect to PDN impedance above 500KHz
- Reducing Supply voltage variation largely depends on power integrity design: passive decoupling capacitors for die/package/PCB
  - Passive decoupling always leads to several resonance peaks in PDN impedance profile
- With limited room to further lower PDN impedance, future processor’s supply voltage variation is expected to worsen
- IVR is among limited options to further lower PDN impedance
  a) eliminating PDN bottleneck due to PCB/package
  b) active PI decoupling from ~100MHz regulation bandwidth

![Diagram of Power Delivery Network (PDN)]

Ideal Power delivery: $V_{cc}(f) = I_{cc}(f) * Z_{PDN}(f) \approx 0$

Realistic PD: $V_{cc}(f) = I_{cc}(f) * Z_{PDN}(f) \gg 0$

Decoupling capacitors to lower impedance at specific frequency
Can We Live with Inductor-less IVR?

- On-die LDO and switched capacitor converter have been favorite subjects in PowerSoC community
  - Implementation and efficiency challenges of integrated buck converter are difficult to overcome
- LDO and switched capacitor VR cannot replace buck converter as POL VR in case of high power density applications.

LDO is equivalent to a variable resistor.
Peak current and load transient challenge is passed to input VR stage of LDO.
Trade-off between load regulation and efficiency.

Switched capacitor converter difficult for good load regulator under high current load.

Fundamental model of buck converter IVR is closest to an integrated voltage source!!
100MHz IVR PMIC with Integrated Magnetic Inductors

Key Features

- Process technology: 40nm CMOS
- Operating frequency: 80~140MHz
- Input voltage: 1.4V ~ 2.2V
- Output voltage: 0.5V ~ 1.2V
- Number of VR cells: 8 (2-phase coupled buck VR)
- Total number of phases: 16
- Maximum output current: 1.25A/phase
- Peak efficiency: 82% @1.8V to 0.85V
- Inductor technology: coupled strip-line inductor
- Inductance: 6~8nH
- Coupling coefficient: 0.8
- Package technology: WLCSP
- Chip size: ~15mm²

Master controller/Common analog circuits/DFT circuits

2-phase VR cell with integrated magnetic thin film inductor
Strip-line Magnetic Thin Film Inductor

Magnetic film properties:
- laminated CoZrTaB alloy
- $H_k = 15\text{Oe}$
- $H_{c\_hard} = 0.27\text{Oe}$
- Saturation flux density $\sim 1.0\text{T}$
- Resistivity $= 115\, \mu\Omega\cdot\text{cm}$

Inductor properties:
- Inductance $6\text{~}8\text{nH@100MHz}$
- $R_{dc} \sim 60\, \Omega$
- $R_{ac} = 400\text{~}500\, \Omega\text{@100MHz}$
- $I_{sat} \sim 600\, \text{mA@100MHz}$

Integration technology:
- On-die
- Compatible with WLCSP

3mmx3mm laminated 4um thick CZTB film sample VSM (above) and Permeability (bottom) measurement
100MHz IVR Circuit Implementation

Key VR Controller Features

- Cascode power stage for 2V input voltage
- Input voltage: 1.4V ~ 2.2V
- Output voltage: 0.5V ~ 1.2V
- 2-phase coupled inductor buck converter as basic VR unit; total 8 VR cells
- Fast transient control scheme: hysteresis (fast loop)+conventional voltage mode (slow loop)
- UGB of fast regulation loop up to 100MHz
- Current balancing control for 16 phases ~20mA residual error

![Diagram of 100MHz IVR Circuit Implementation](image)

1.8V Vin, 0.85V Vo efficiency

4-phase efficiency measurement
System Test Setup

- Power delivery comparison between IVR and conventional PMU was carried out.
- Mobile AP is on the opposite side of PCB.
- IVR testing setup eliminates all output PCB/package decoupling capacitors.
- IVR powers 4 big ARM cores, and total output capacitance ~56nF (on AP die).

Vbat to 1.8V Converter Stage → IVR (1.8V to Vdd) → Mobile AP (4X Big Cores)

Conventional PMU (Vbat to Vdd) → Mobile AP (4X Big Cores)
IVR Improves Energy Efficiency of Power Delivery

- ~100MHz switching frequency and high regulation bandwidth can reduce supply voltage variation → less guard-banding in supply voltage, less power
- Increase output capacitance (on-die or close to die) can help further on lowering supply voltage; challenges are in how to implement more capacitance
  - Increasing die size of mobile AP
  - Implementing MIM capacitor in AP
  - Low parasitic package IPD capacitor
- IVR can relax PCB/package PDN design requirements
- Achieving substantial system energy efficiency gain to offset conversion efficiency loss due to 2 stage conversion is essential
  - Amplitude of voltage guard band reduction may be workload dependable
  - What to incentivize customer adoption?

Energy efficiency improvement from reduced guard band in supply voltage, due to IVR’s moderate load line and reduced droop
An Unexpected Catalyst for IVR’s Commercial Adoption

- Growing gap between MLCC supply and demand
- Cost (component price & PCB area) of using MLCC may become top issues for system engineers.
- Prolonged Shortage (>5yr) could ignite more interest for IVR’s less MLCC dependent nature.

MLCC demand increase is expected trend. Multiple end markets compete limited supply.

*Based on technical report from TTI, Inc.

Typical smartphone system has noticeable amount of MLCC content.

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Supply Chain Challenges of Commercializing Magnetic Inductor IVR

Where to manufacture?

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Cost</th>
<th>Cross Contamination</th>
<th>Decoupled from specific CMOS node</th>
<th>12-inch process</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>High?</td>
<td>Big concern</td>
<td>Business model?</td>
<td>yes</td>
</tr>
<tr>
<td>OSAT</td>
<td>less</td>
<td>Less sensitive</td>
<td>flexible</td>
<td>yes</td>
</tr>
</tbody>
</table>

Fabrication bottleneck from magnetic thin film deposition

- PVD deposition of 5µm and thicker laminated magnetic film
- Thick copper RDL layer deposition for inductor windings

Material cost and sourcing

- Usage amount of magnetic material can be a major challenge for cost down
- May be too susceptible to volatility in Cobalt price
- Limited sourcing channels for CoZrTa may create hurdle for high volume adoption, i.e. smartphone.

Availability of high through-put 12-inch magnetic PVD tool?

- Existing PVD tool is not optimized for this application

Cobalt price’s significant surge and plunge creates uncertainty on cost expectation of thin film inductors.
Final Thoughts

- Break-through on integrated magnetic inductor IVR must happen for future mobile and server processors.
- Improved energy efficiency from lowered supply voltage by IVR is demonstrated. How far to trigger product adoption?
- On-die strip-line magnetic inductors are compatible with high volume wafer process flow; many supply chain challenges have to be addressed before mass production.
- Productization of IVR with magnetic inductors may be sooner than we think…
- Some areas for future research:
  - Alternative core materials – saturation magnetic flux density 2T or higher, resistivity > 500\(\mu\Omega\cdot\text{cm}\)
  - High efficiency VR topologies for both IVR input stage and IVR
Thank you

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