Numerical predictions of a novel 3D stacked Power-SoC structure based on hexagonal-BN

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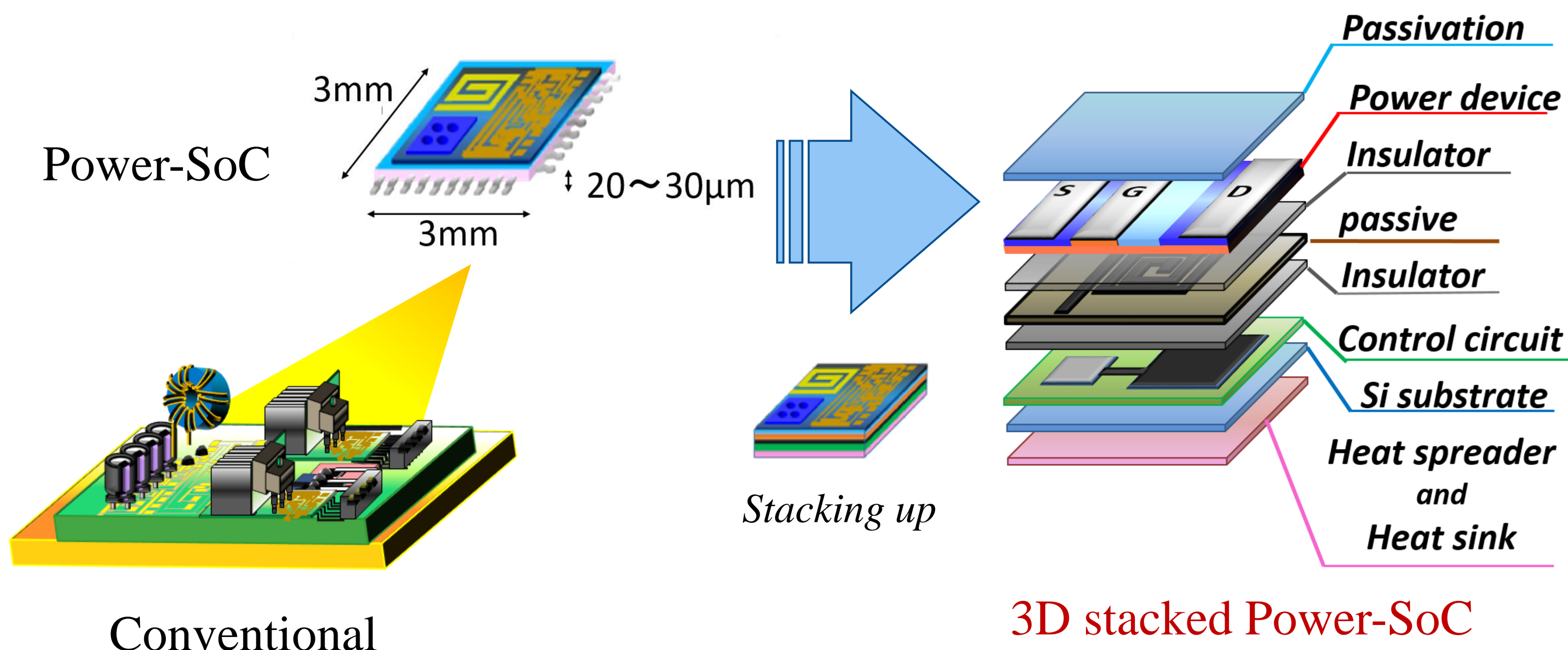
PWR SOC 18
Hsinchu, Taiwan
Oct. 17-19, 2018

AIST

INTRODUCTION

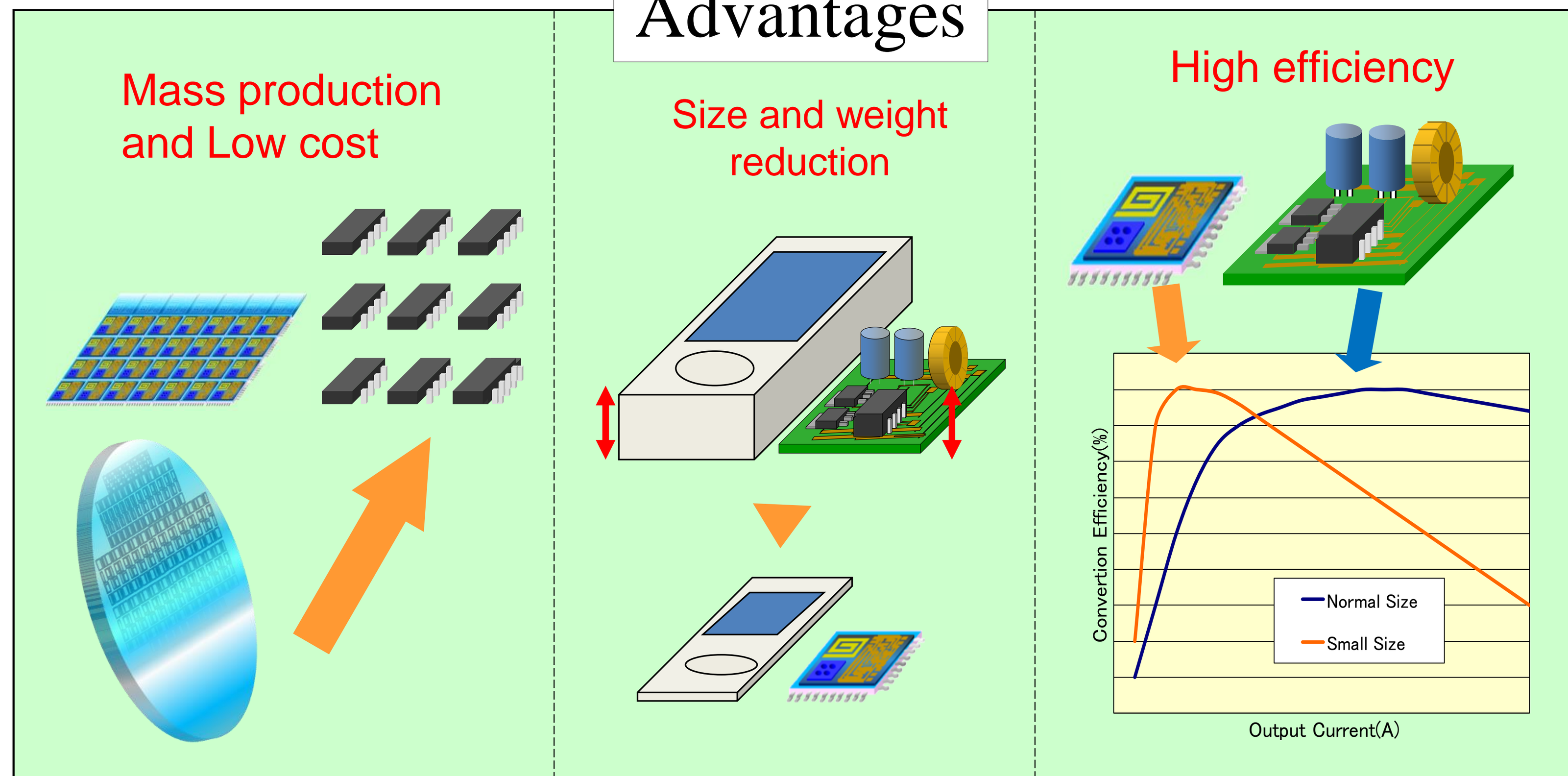
Miniaturization of power-supply



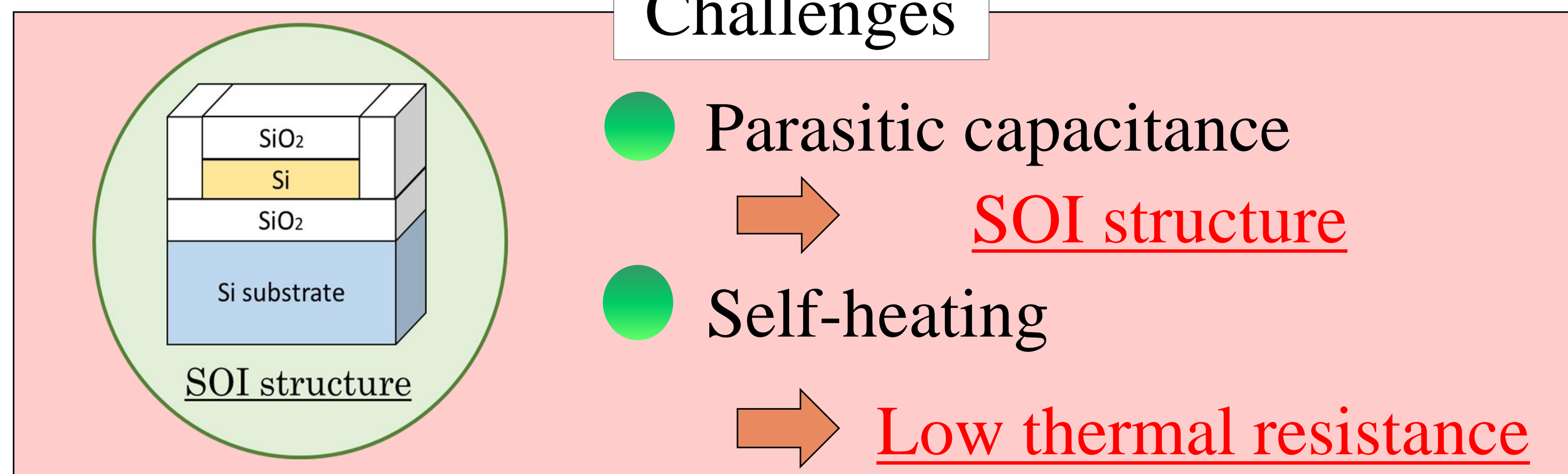
Conventional

3D stacked Power-SoC

Advantages



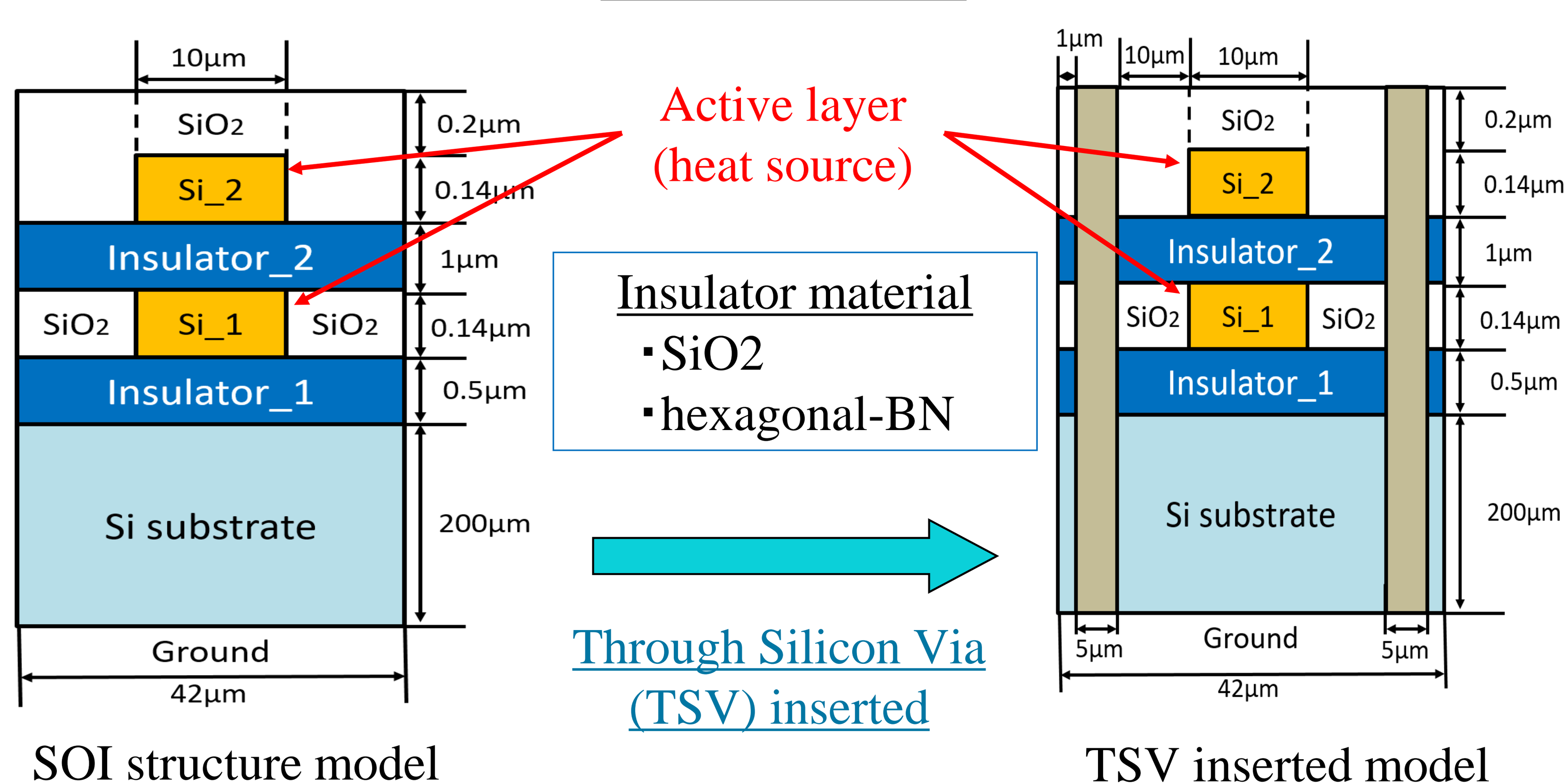
Challenges



- Parasitic capacitance → SOI structure
- Self-heating → Low thermal resistance

SIMULATION

Structure



SOI structure model

TSV inserted model

Thermal conductivity of the materials

Material	Thermal conductivity [W/(m・K)]	
Si	145	
SiO2	1.38	
h-BN *	Virtical	2
	Holizontal	390
TSV(Cu)	398	

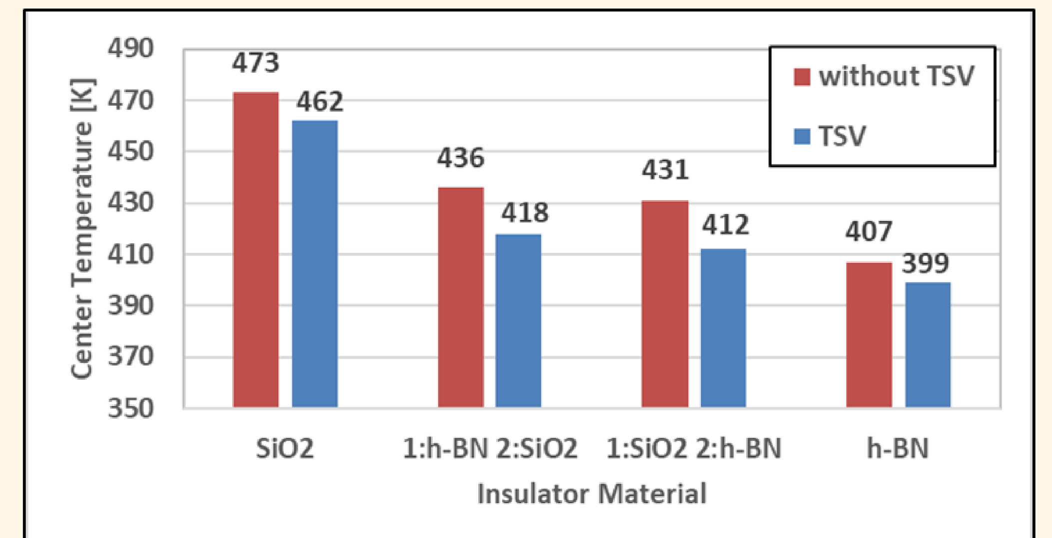
*References: [1] I. Jo, et al., Nano Lett., 13, 550-554, 2013.
[2] S. M. Kim et al., Nature communications, 6, 8662, 2015.

SIMULATION RESULTS

Impact of h-BN and TSV for heat dissipation performance

Conditions

- The heat source is *Si_1* layer
- *Si_1* layer is 473K
- The material of *Insulator_1* and *Insulator_2* is SiO_2

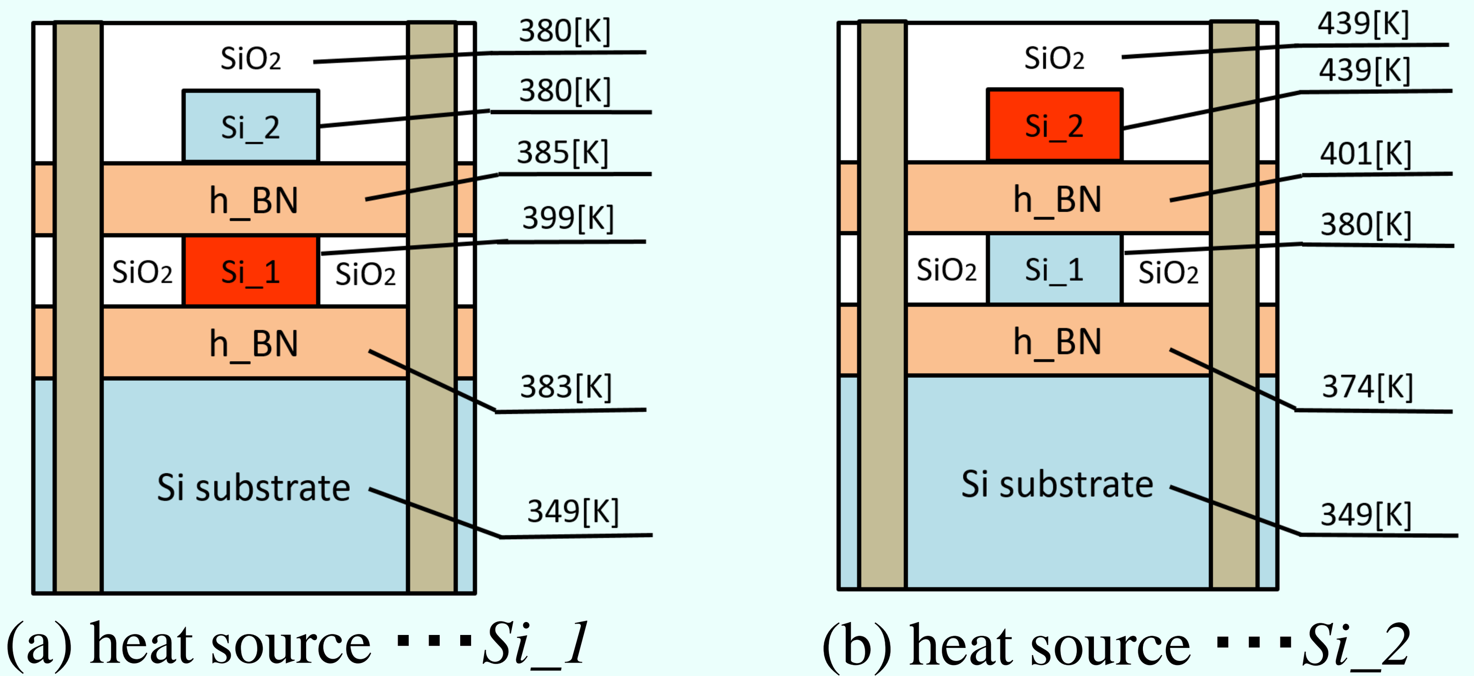


The temperature of heat source is about 70K lower.

Center temperature of heat source (*Si_1*)

- Heat exhaust is the most improved when h-BN is used as both insulators.
- TSV can suppress temperature increase 10-20K.

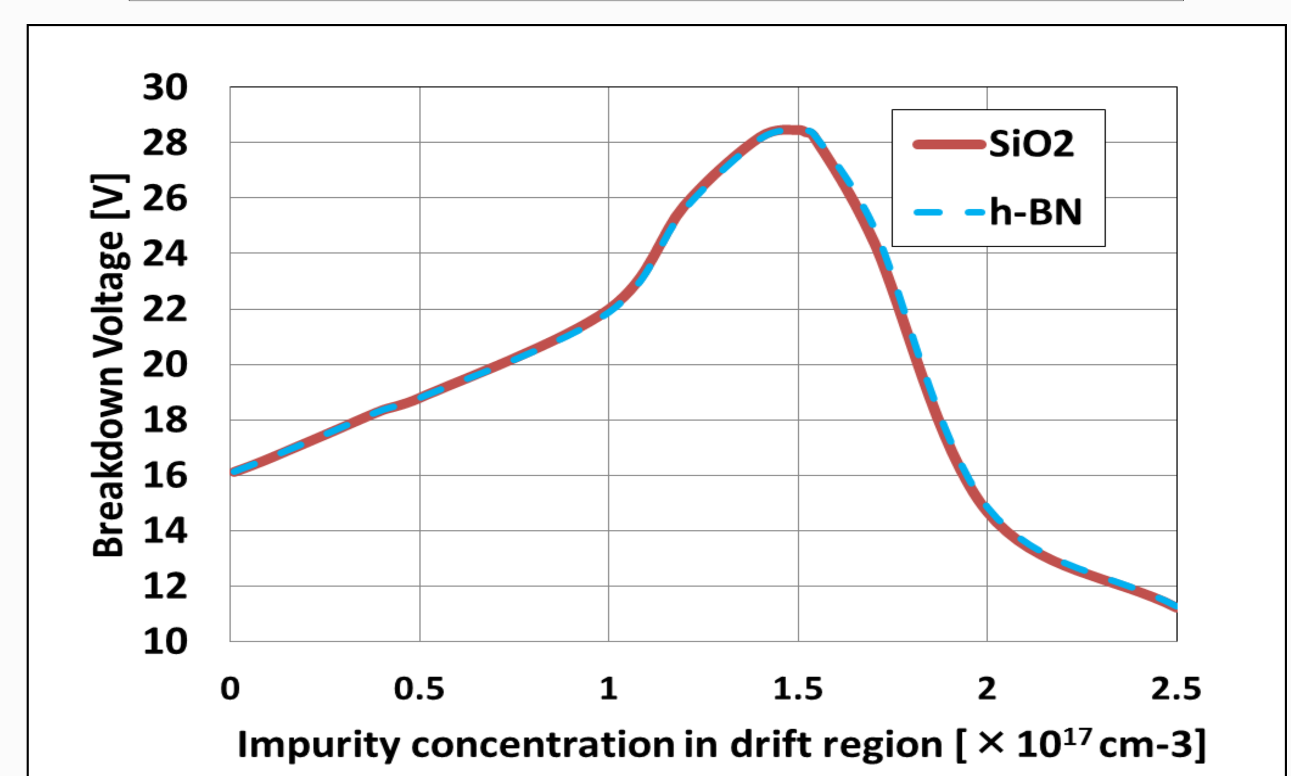
Dependence of the temperature of the 3D power-SoC on position of the heat source



(a) heat source ･･･*Si_1*　(b) heat source ･･･*Si_2*

- Temperature of (b) is higher because Si_2 layer as a heat source is covered with SiO_2.

Dependence of the breakdown voltage on the impurity concentration in drift region



→ The same breakdown voltage and on-resistance

- The relative permittivity → SiO_2:3.9　h-BN:4.0
- Using h-BN does not degrade the breakdown voltage and on-resistance

CONCLUSIONS

- Heat dissipation performance is improved by h-BN based 3D stacked power-SoC with TSV.
- Heat source should implement lower Si layer.