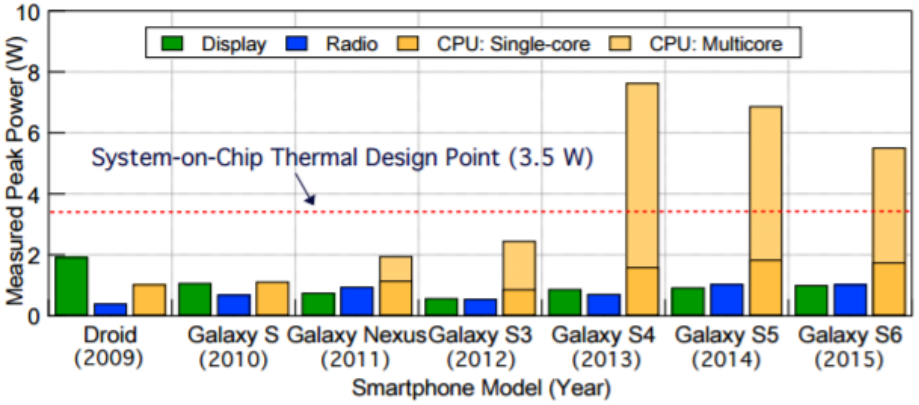
Hybrid switching converter architectures for powering processors and SoCs

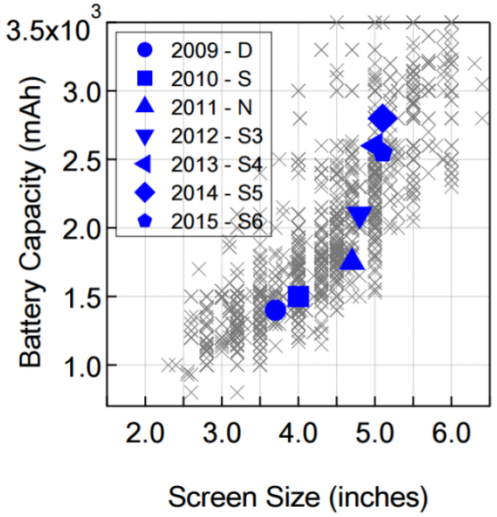
Yogesh Ramadass

Kilby Labs

Texas Instruments, Santa Clara

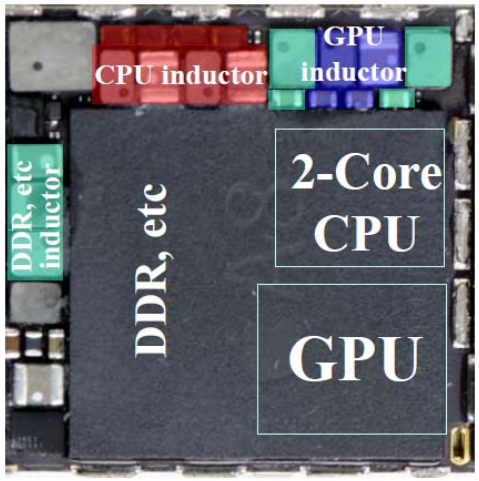
Mobile applications





M. Halpern, HPCA, 2016

- Higher charging currents
- Processors with more power
- Thin profile, Heavily space constrained

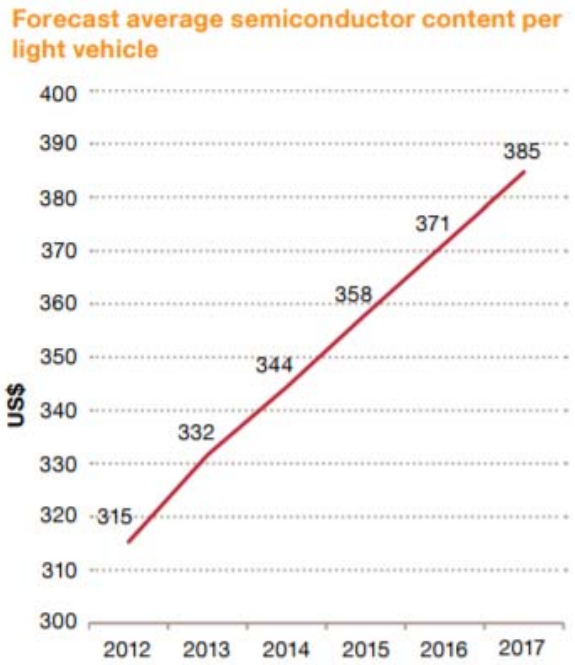


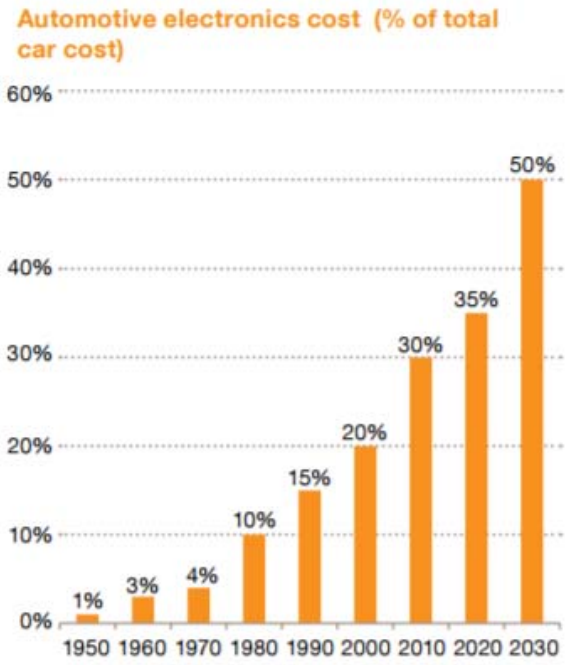
~8A

~4A

Dongbin Hu, CPES, 2016

Automotive applications



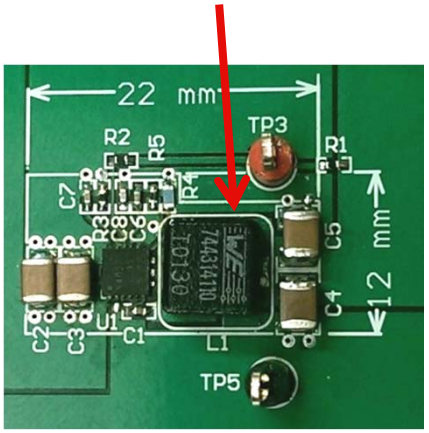


Source: PwC analysis

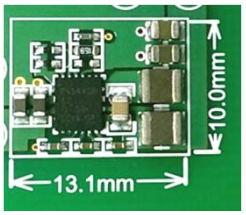
- Electronics heavy
- Higher current demands with low EMI
- 3V - 42V input support

Increasing switching frequency

Inductors are usually the largest component.



1) Smaller size



Converter volume: 1,270 mm^3

Inductor volume: 232 mm^3

Converter volume: 157 mm^3

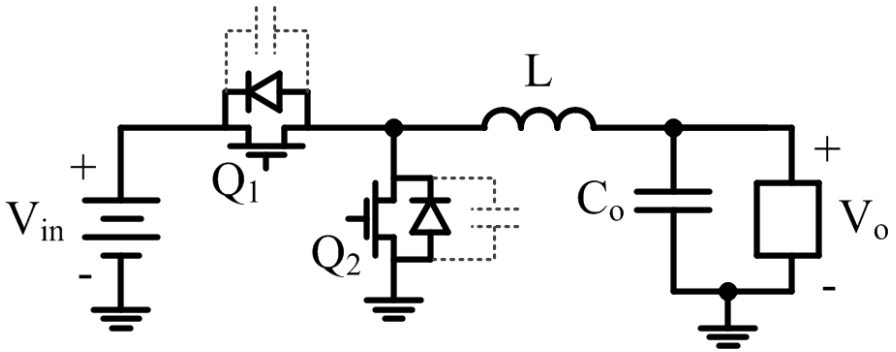
Inductor volume: 19.2 mm^3

2) Faster response

3) Lower BOM cost

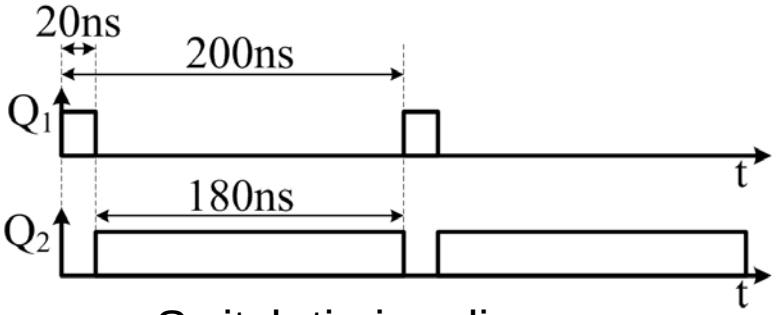
High frequency operation → 15 times smaller inductors!

High frequency (HF) buck converter limitations



Hard-Switched Buck FET Losses

Conduction	$I_{rms}^2 R_{DS}$
Switching	$Q_{OSS} V_{IN} f_{SW}$
Reverse Recovery	$Q_{RR} V_{IN} f_{SW}$
IV-Overlap	$I_{L,AV} V_{IN} t_{ov} f_{SW}$
Gate Drive	$2 Q_G V_{DRV} f_{SW}$

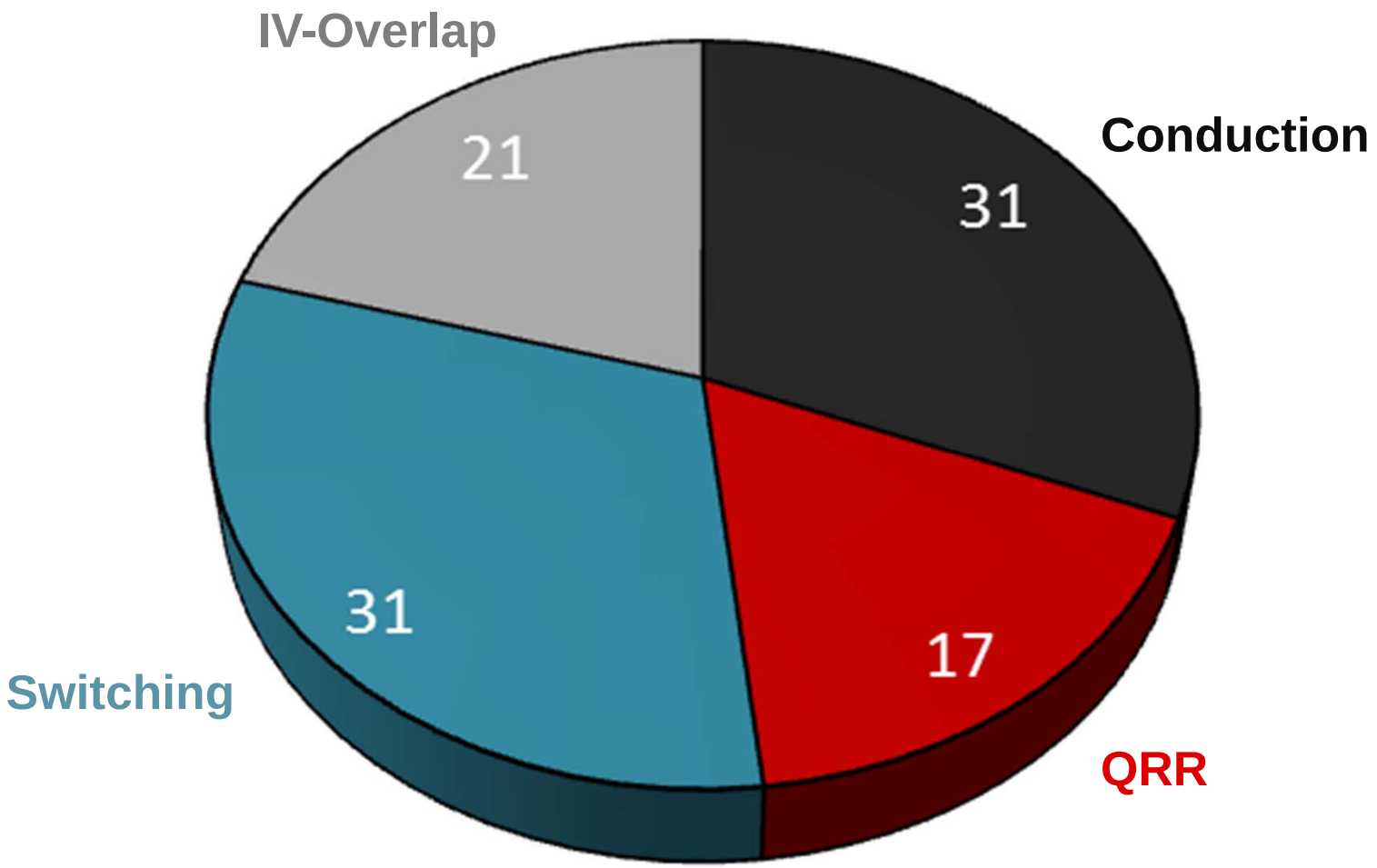


Switch timing diagram

- High side switch (Q_1) on-time is very short at HF
  - 5 MHz → 200ns period
  - 10-to-1 voltage ratio →20ns high side on-time

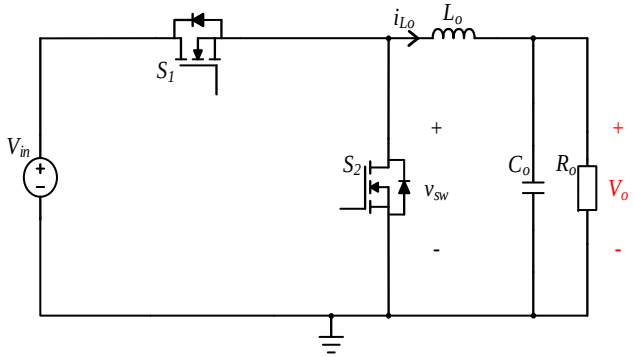
HF converters on the market today have low conversion ratios (<5-to-1) and low current (<1A)

Buck converter loss breakdown

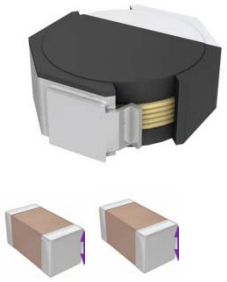


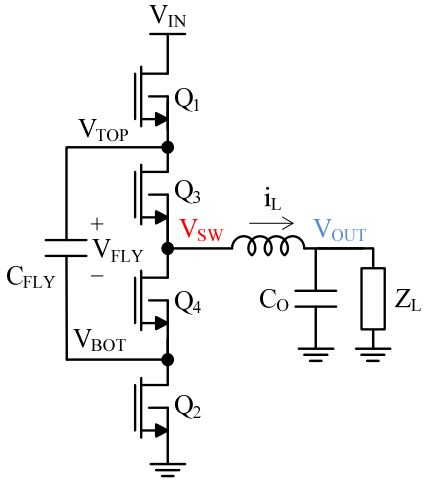
Topology Options

BUCK

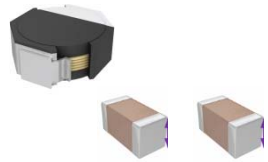


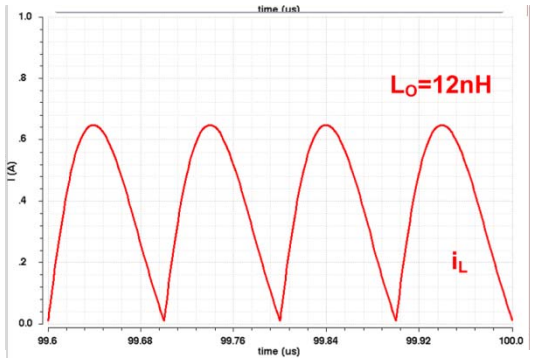
HYBRID



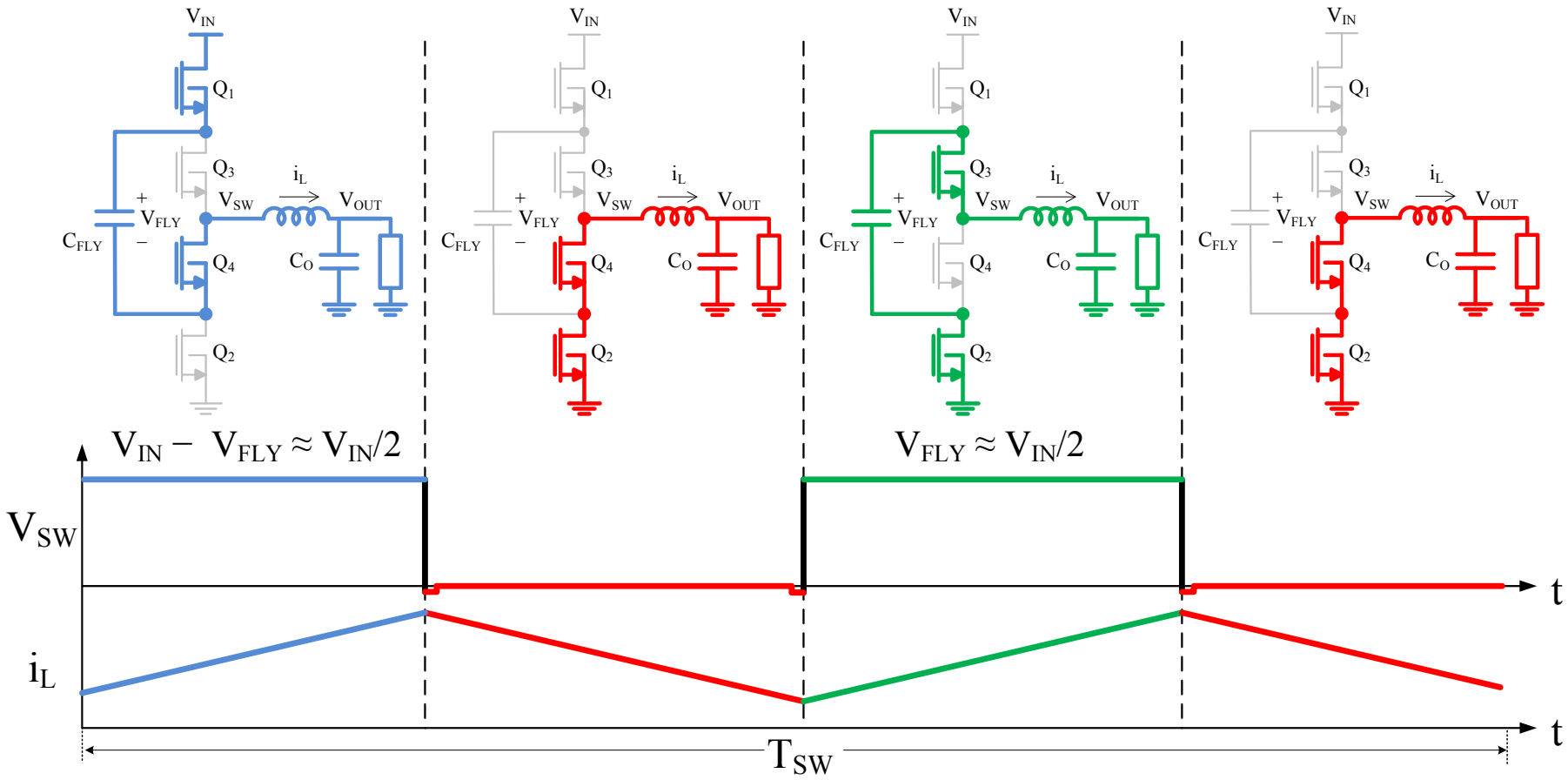


RESONANT

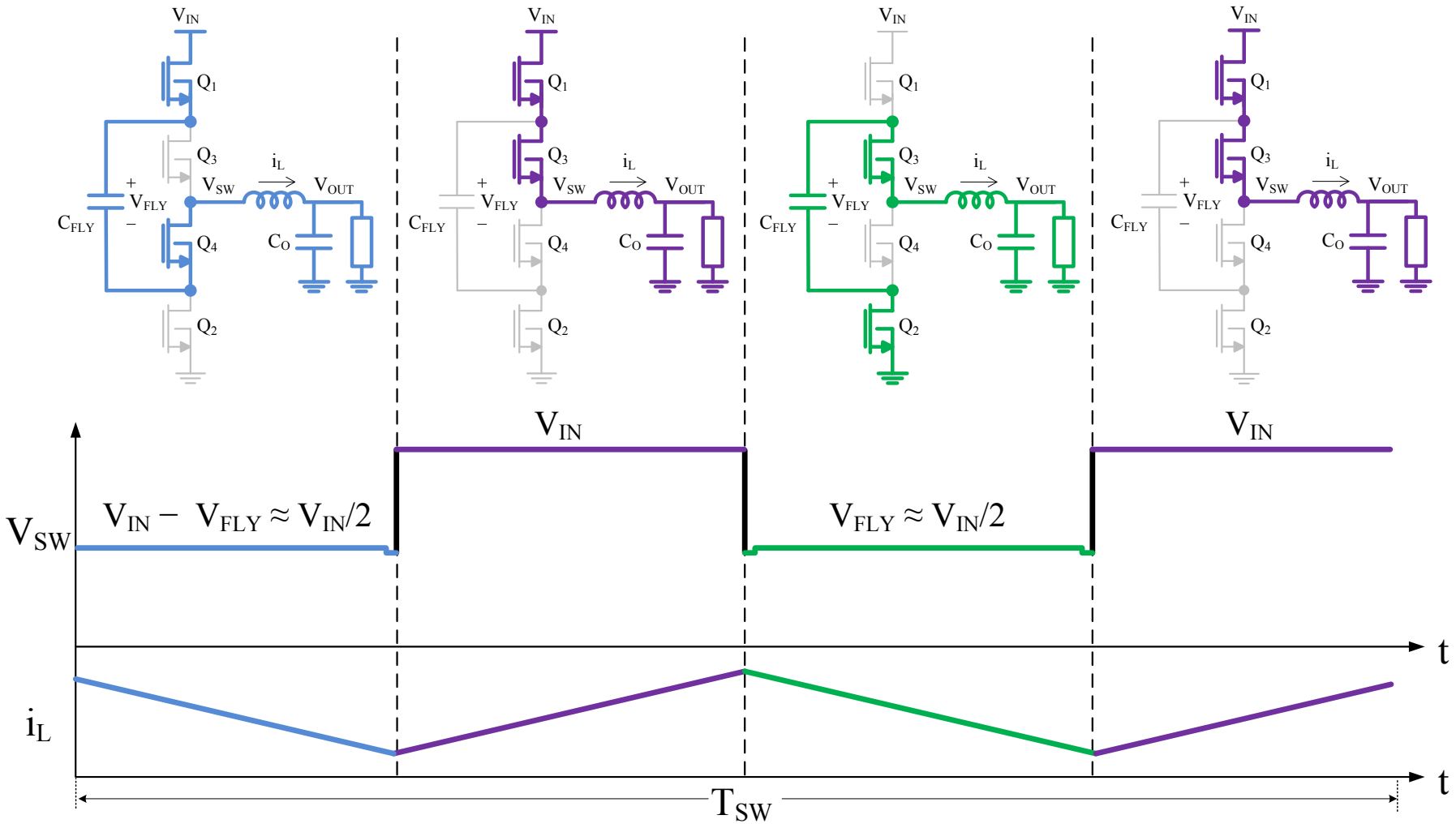




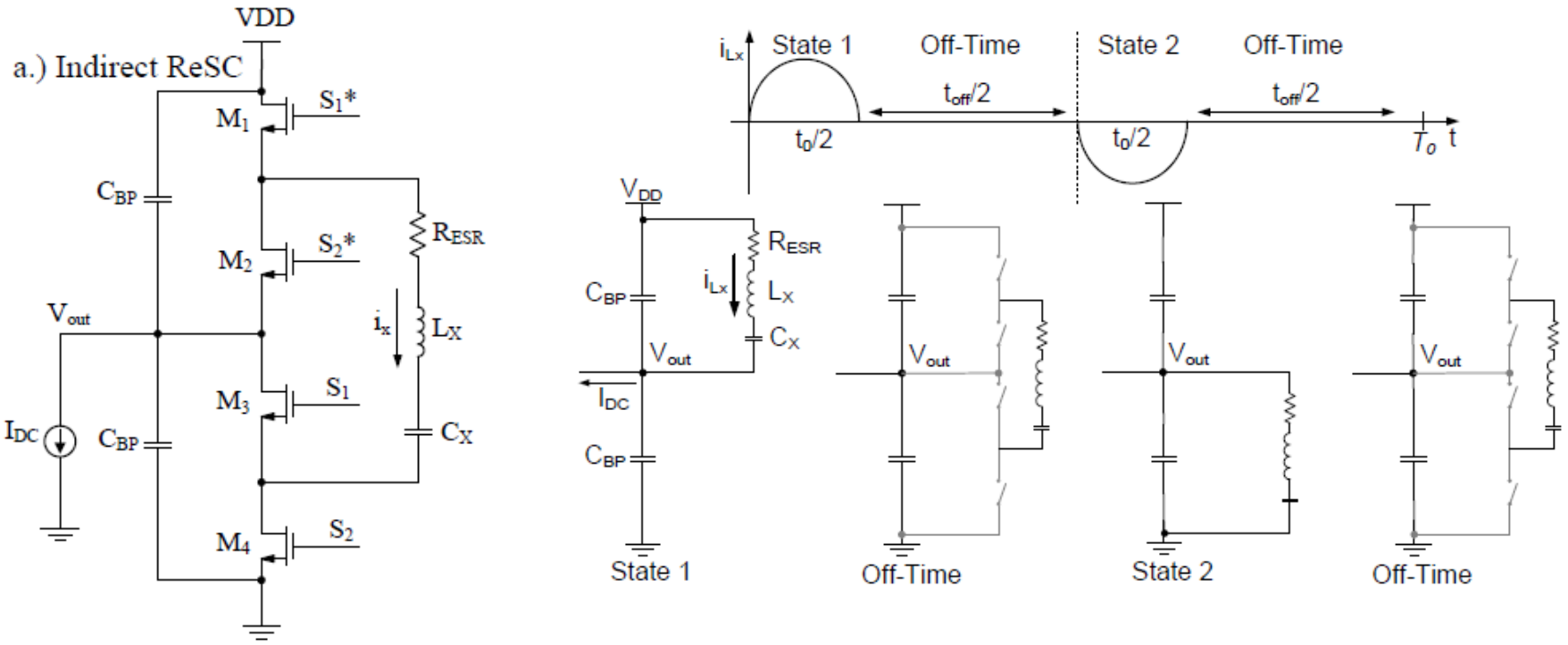
Three-Level Buck Converter (D < 0.50)



Three-Level Buck Converter (D > 0.50)



Resonant Switched Capacitor Converter



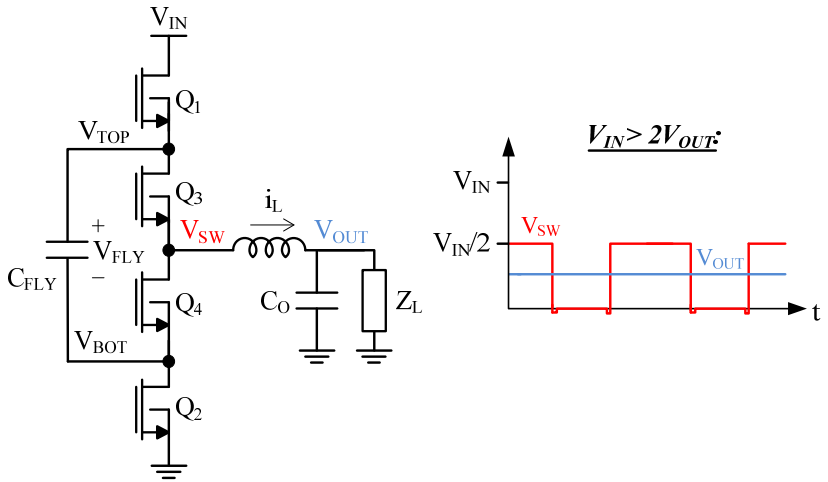
K. Kesarwani, APEC 2015

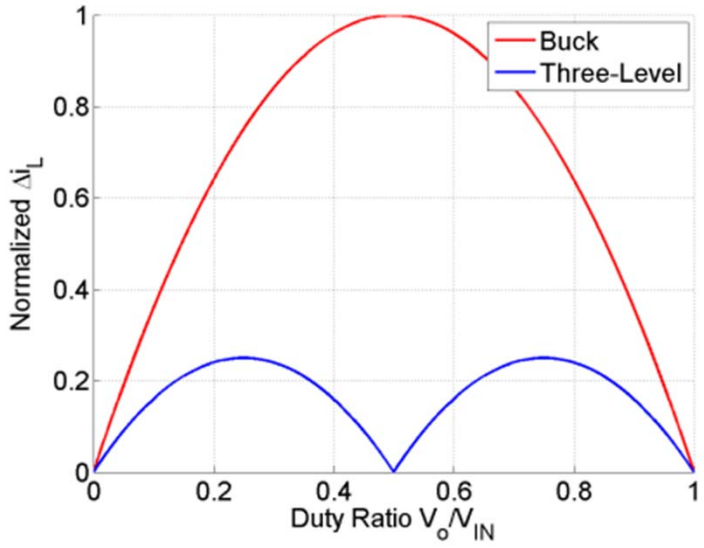
- Extension of 3-level converter with very low inductance
- Constant inductor current traded off for small form factor

3-level converter advantages

- Q1, Q3 gate-drives interleaved and 180^{o} out of phase. 2X switching frequency

- Peak inductor ripple current is ¼ of 2L converter



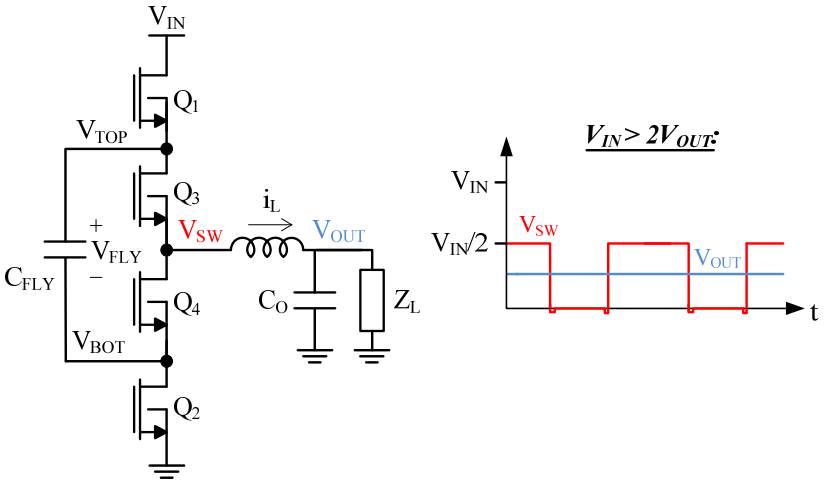


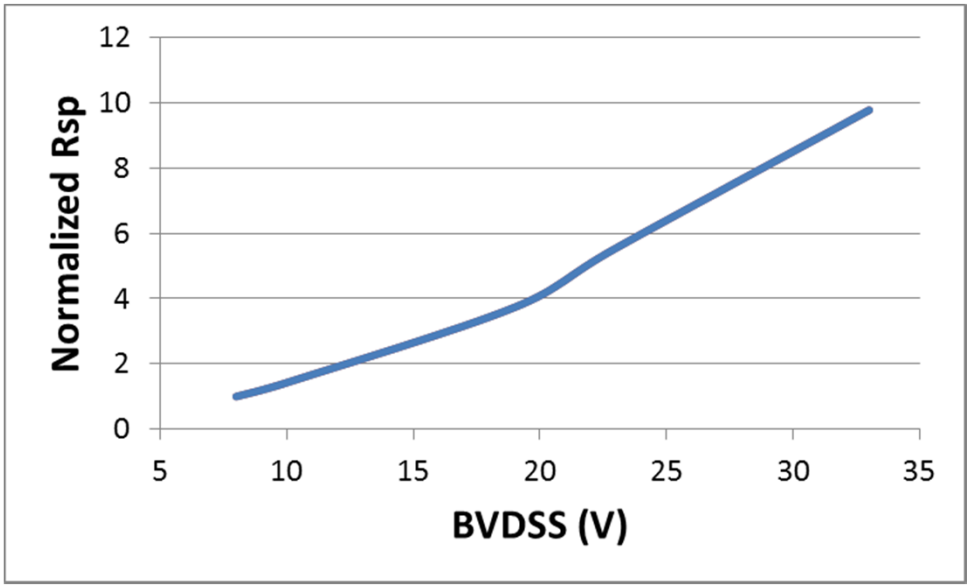
Power density improvements

Figure removed for public release

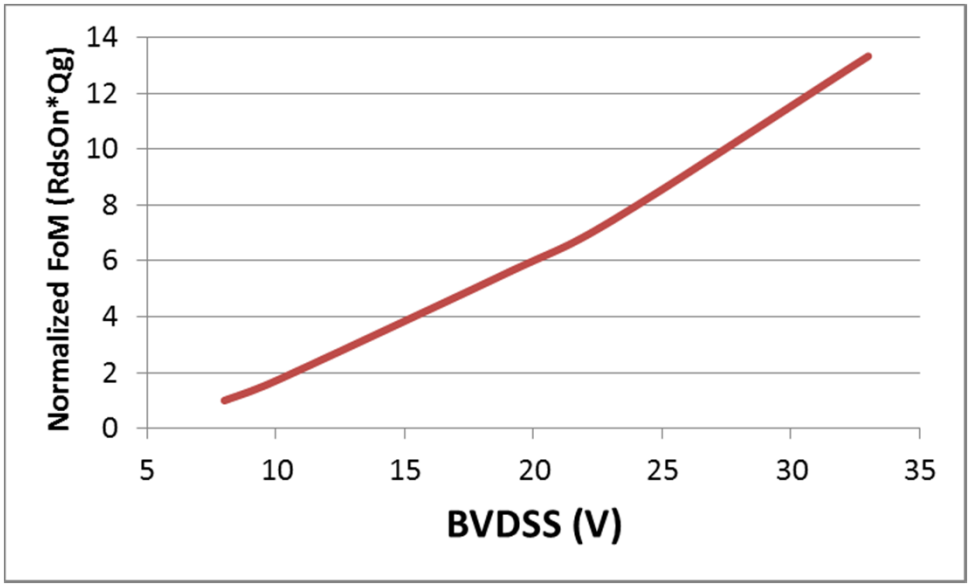
- >2.5X area density and >5X volume density benefits
- Reduction in height and ability to handle larger currents with smaller inductors

Switch Rsp and FoM

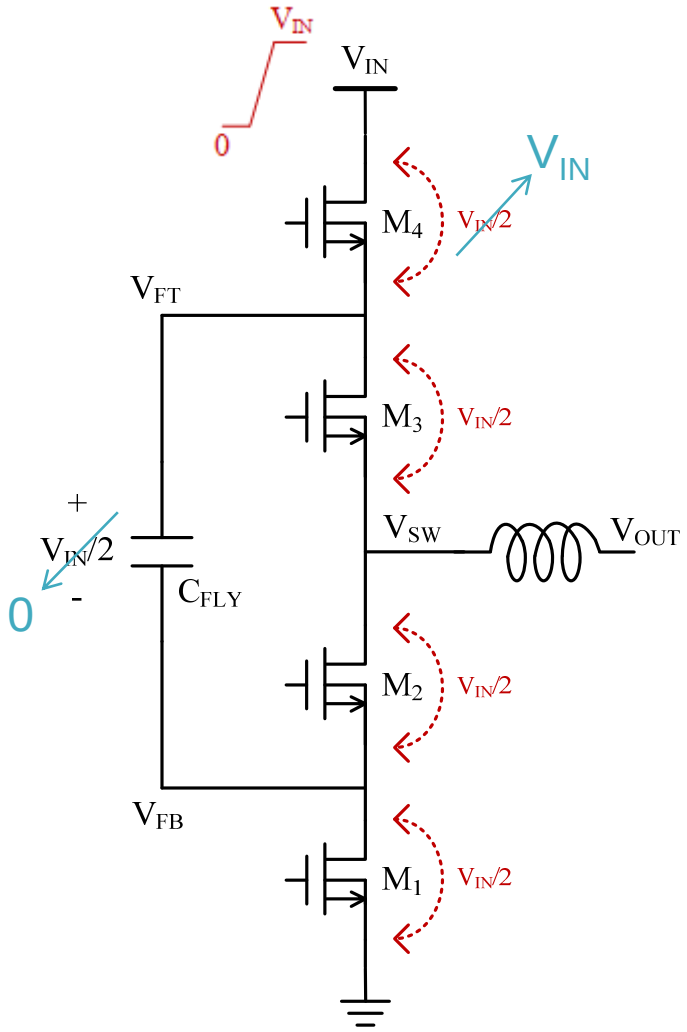




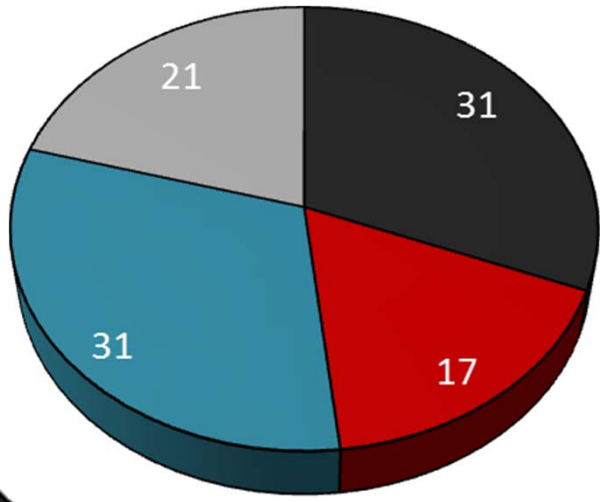
- Lower voltage switches have inherent Rsp and FoM benefits
- Ability to use lower voltage rated FETs crucial in nano-meter scale CMOS processes

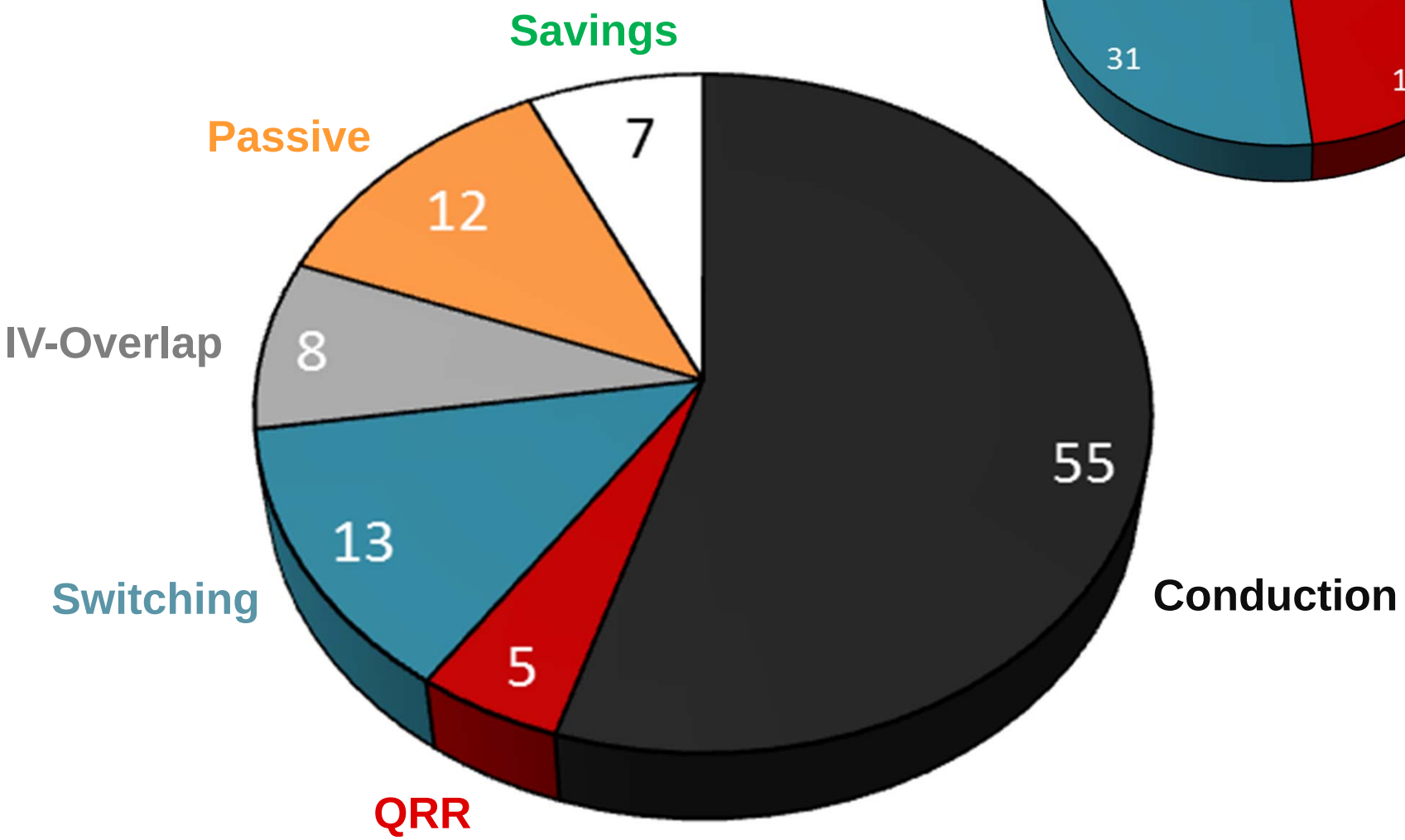


Device Voltage Ratings

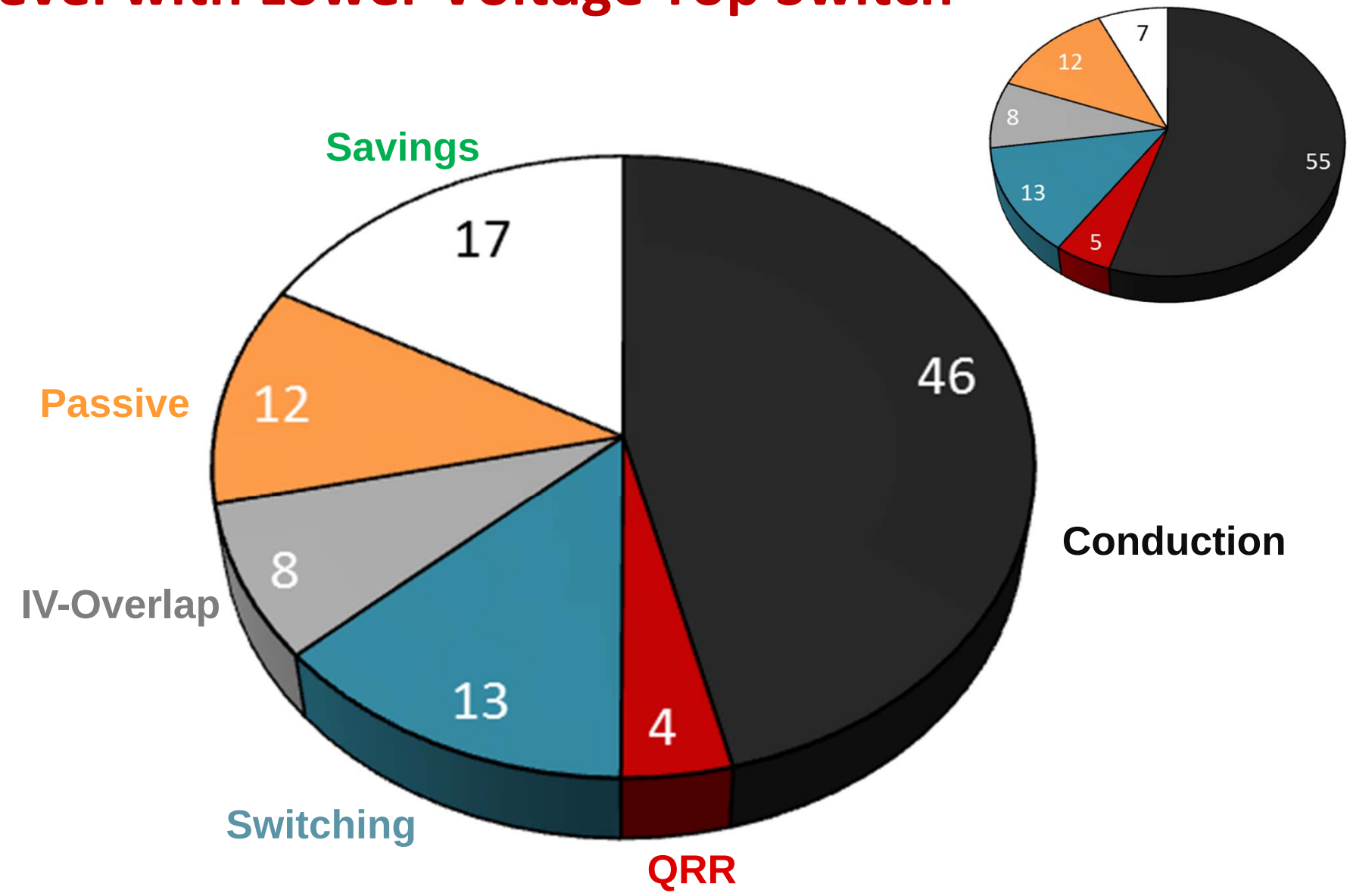


3-Level Loss Breakdown

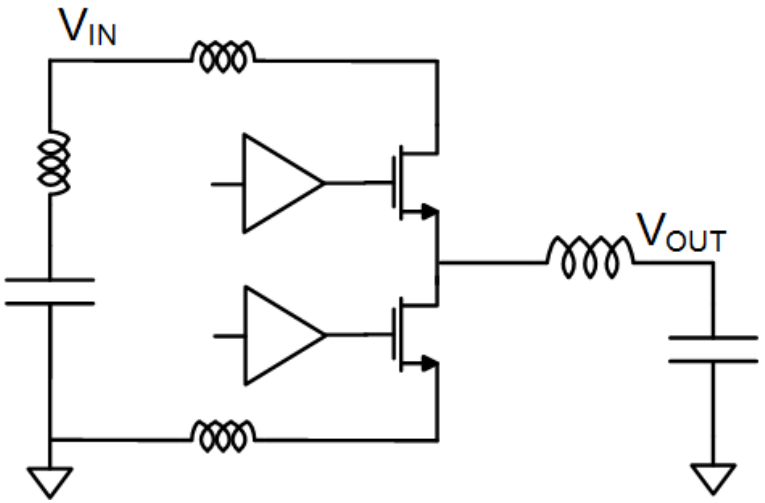


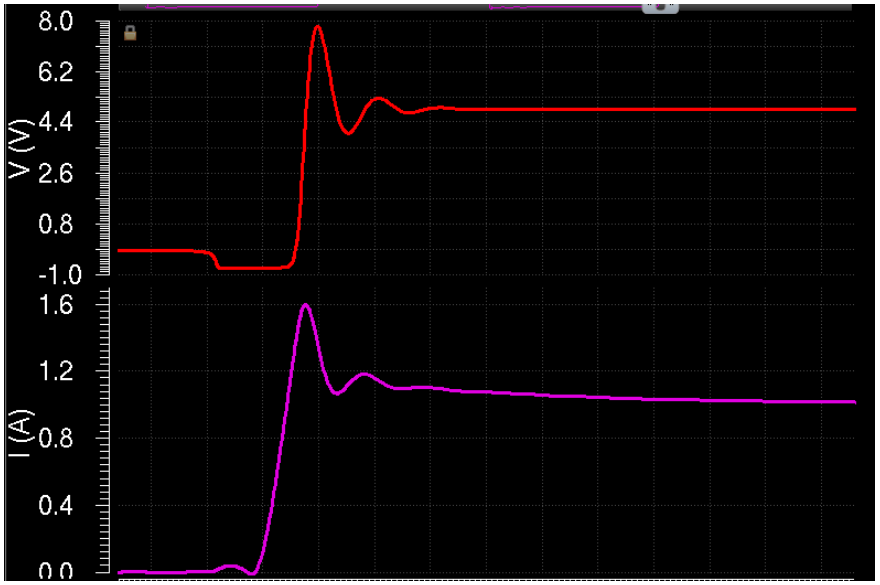


3-Level with Lower Voltage Top Switch



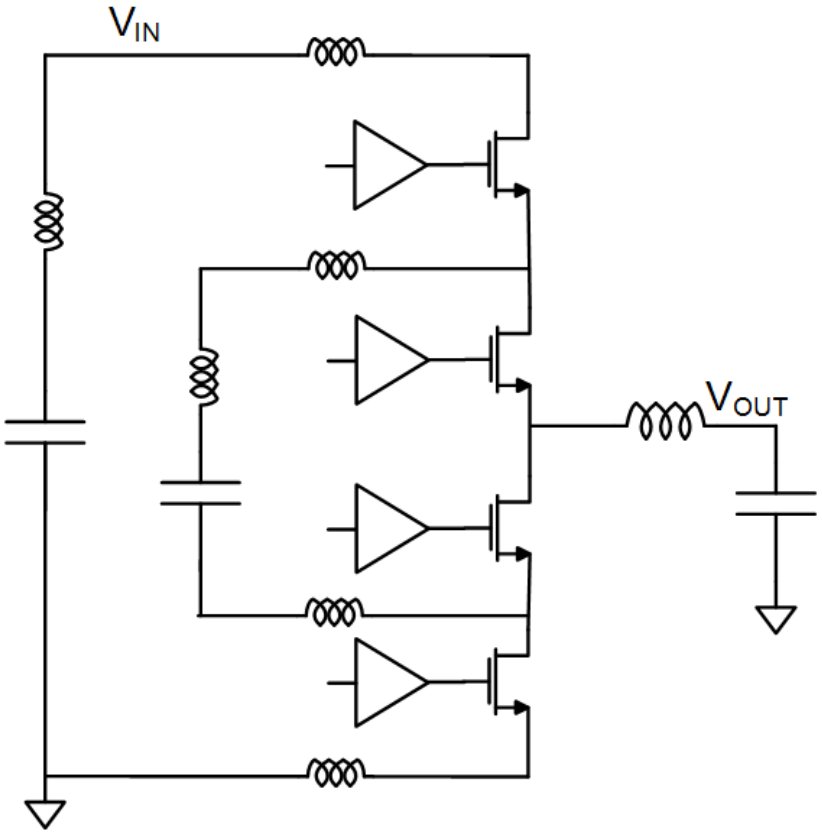
Power Loop Inductance - Buck

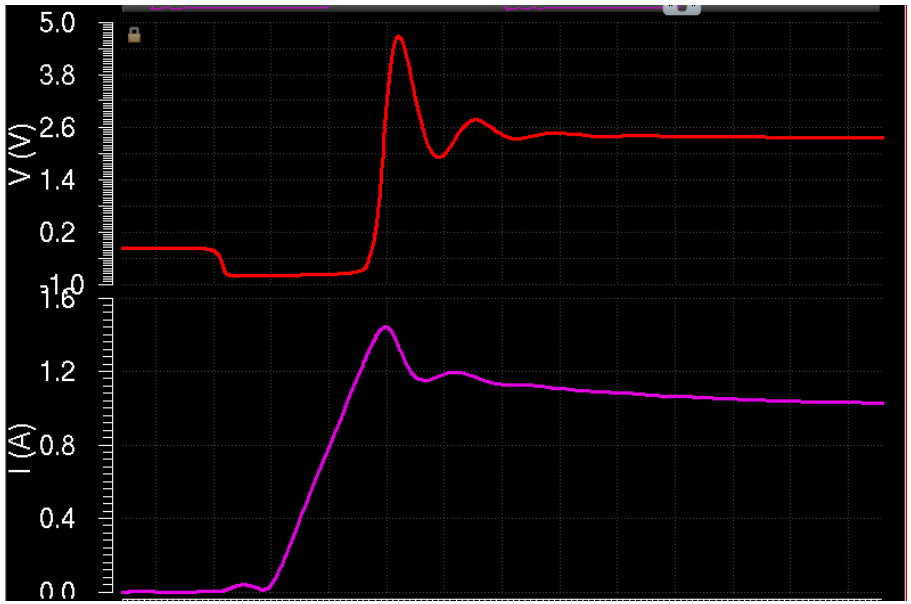




- Loop parasitics cause ringing forcing the slowdown of drives and increasing overlap losses

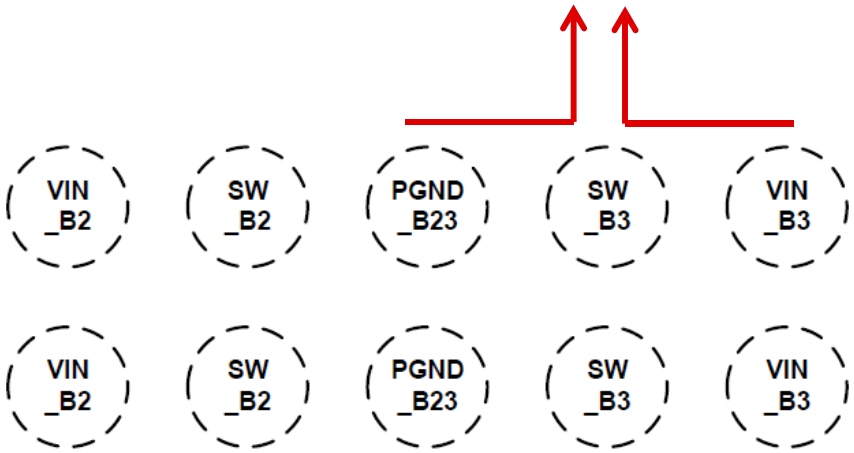
Power Loop Inductance – 3-Level



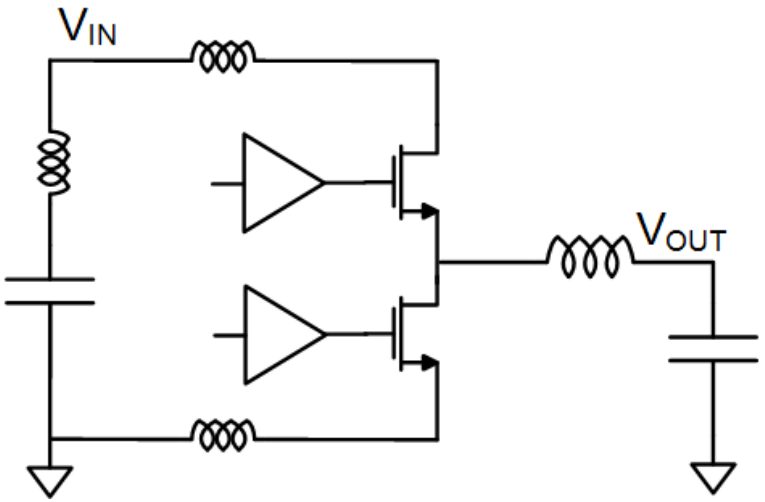


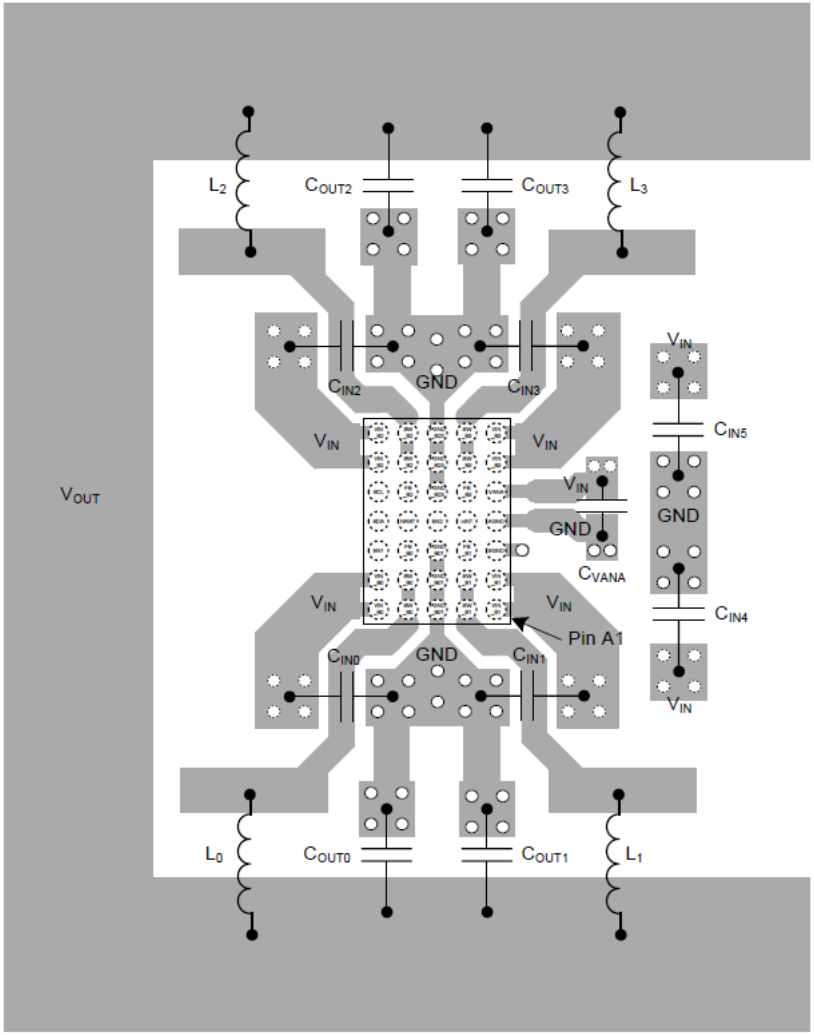
- Increased number of switches and external passives – increase in loop inductance
- Effective on-chip passives needed to take peak currents

Board routing - Buck

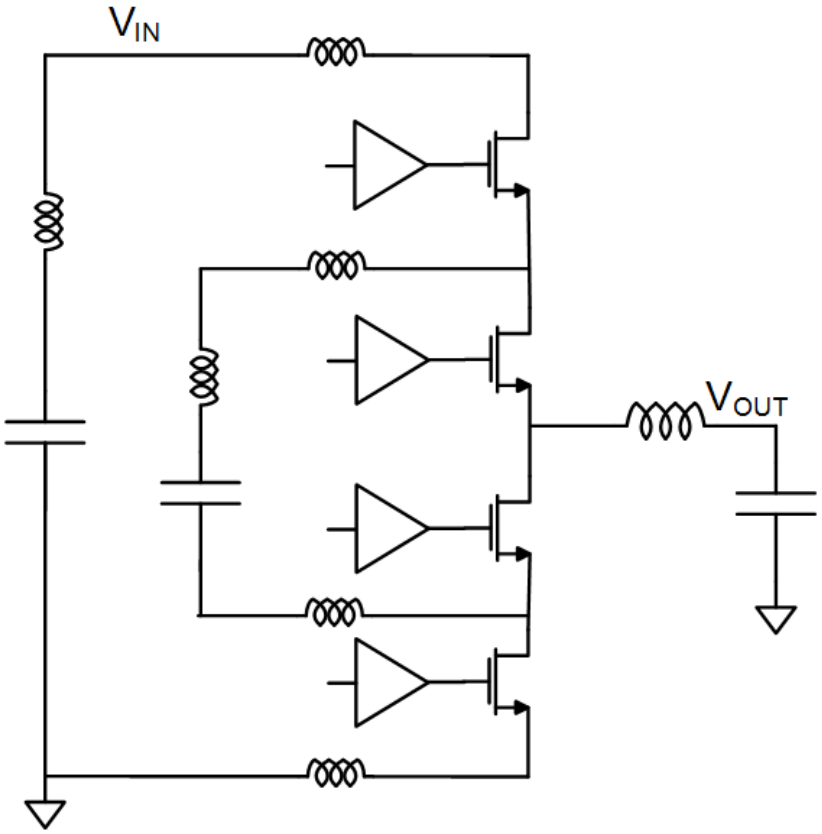


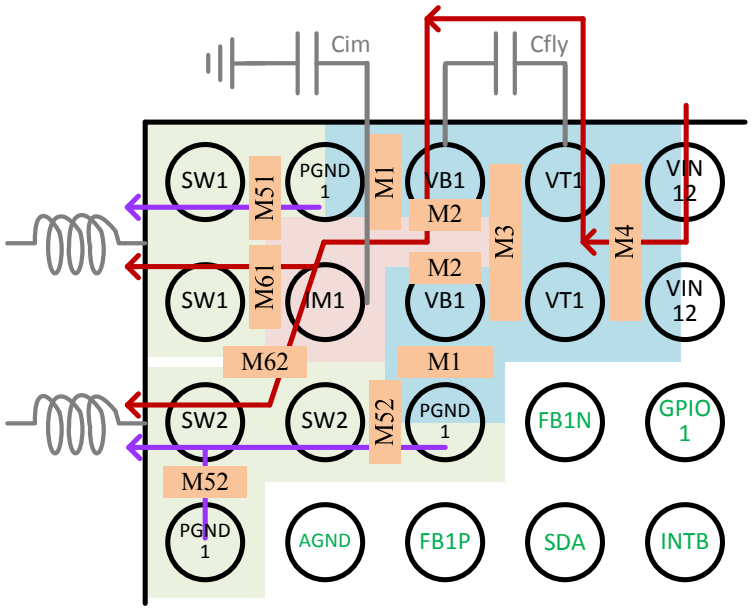
LP8758





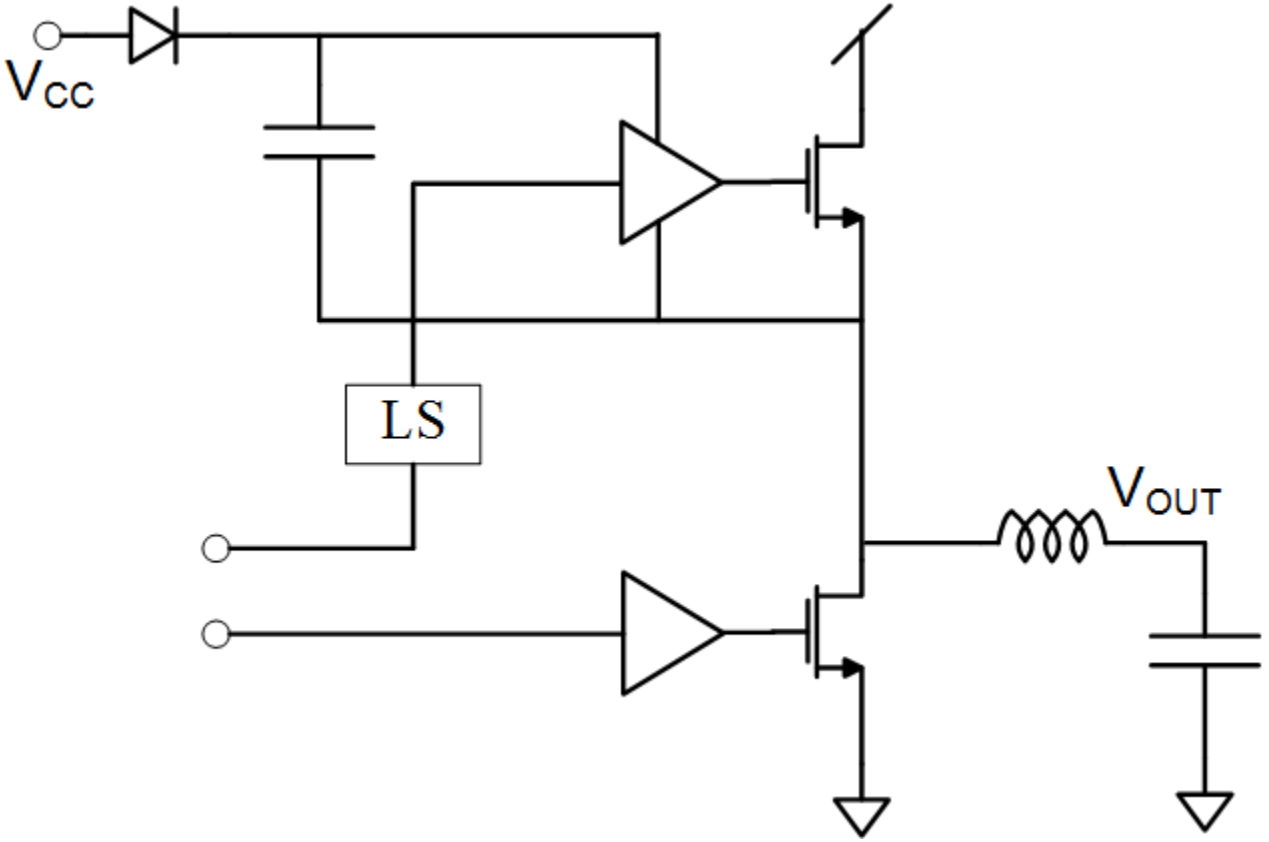
Board routing – 3-Level





- Increased number of switches and external passives – complicated floor planning and board routing
- Effective on-chip passives needed to take peak currents

Gate drive and boot capacitor management



Gate drive and boot capacitor management

Figure removed for public release

- Complicated boot-capacitor management
- Increased level shifting complexity

Conclusions

- Power density and efficiency becoming ever more crucial in automotive and consumer systems
- Hybrid and Resonant topologies provide distinct advantages in reducing magnetics size and improving efficiency
- Increased device/passive/pin count and control complexity
- Provides opportunities to circuit and system designers to come up with innovative circuit architectures and control techniques to mitigate problems