Ring-Shaped Multiphase Switched-Capacitor DC-DC Converters

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Outline

• Motivations of the DC-DC Converter-Ring
• Discussion on Unity Gain bandwidth Extension
• Layout-Oriented Converter-Ring Design
• Measurement Results
• Extended Possible Solutions
• Conclusions
Multi-Interleaving-Phase DC-DC Converters

- Reduce output voltage ripple
- Reduce input current ripple

- Fully-on-chip, multi-phase
- Efficiency (like linear regulator)
- First-order power stage

- One L for each phase
- Efficiency (ideally 100%)
- LC second-order filter
On-Chip IR Drops and $dI/dt$ Variations

- On-chip power delivery suffers from **IR drops** and **supply variations**.
- Supplying the load from **all directions** can significantly alleviate such problem.

![Diagram](image_url)
Conceptual Layout of the Converter-Ring

Top edge: – 30 Phases
Other 3 edges: – 31 Phases
In total: – 123 Phases

No. of Phase is flexible.

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Prior Art Achieving Fast Transient

• Achieved fast transient response with additional 3.3GHz Clock.

H.-P. Le, et al., ISSCC, 2013
Prior Art Achieving Fast Transient

• Achieved fast transient response with 4GHz Clock and feedforward control.

T. M. Andersen, et al., ISSCC, 2015
Unity Gain Frequency (UGF) Extension

- Using the following configurations for the switched-capacitor power converter (SCPC) for UGF extension:
  - Set the dominant pole at \( V_{\text{OUT}} \),
  - Employ a high speed error amplifier (EA),
  - Tune the oscillator frequency through its supply (\( V_{\text{DD,CO}} \)).
Proposed System Architecture

Centralized Oscillator, Distributed Clock Phase

Conventional

Proposed

Distributed Oscillator, Localized Clock Phase

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Pseudo-Continuous-Time SCPC

- Increasing the phase number also enables the control-loop to respond at every fraction of the switching period ($T$), which is $T/123$ in our case.

- The discrete-time SCPC approaches a pseudo-continuous-time power stage. Thus, UGF of the control-loop could be designed to be higher than the switching frequency of the SCPC.

Achieve fast response without using additional GHz clock.
Error Amplifier and $V_{DD}$ Controlled Oscillator

$$A_{EA} = \frac{g_{m2}}{g_{m4}} \cdot \frac{g_{m5}}{g_{m6}} \cdot g_{m7} r_{o7} \cdot A_8 \cdot A_{NC}$$

$\approx 8 \cdot g_{m2} r_{o7}$
Internal Rails for Low Voltage Devices

- Voltage domain \([V_{IN} : V_{SSH}] = [V_{IN} : \frac{V_{IN}}{3}]\)
- Voltage domain \([V_{DDL} : \text{Gnd}] = [2\frac{V_{IN}}{3} : \text{Gnd}]\)
- \(V_{IN}: 1.6\text{V} \text{ to } 2.2\text{V}\)
Level Shifter (LS)

- Effectively convert the input signal from the $[V_{DDC} : \text{Gnd}]$ domain to the domains of $[V_{IN} : V_{SSH}]$ and $[V_{DDL} : \text{Gnd}]$, simultaneously, through one single conversion.

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The conversion ratio (CR) can be reconfigured into $1/2$, $2/3$, $3/4$. 

(N-1)/N Switched-Capacitor Power Converter
(N-1)/N Switched-Capacitor Power Converter
12 Switches and 3 Capacitors for Each Unit Cell
3-Transistor Based Inverters
CR=3/4. S₃ and S₇ are Constant Off.
CR=2/3. $S_{3,10,11}$ Constant Off, $S_{9,12}$ Constant On.
CR=1/2. $S_{6,7,10,11}$ Constant Off, $S_{5,8,9,12}$ Constant On.
Chip Micrograph

- 65nm CMOS
- 1.2V LL Devices
- Stacked MOS, MOM, MIM capacitors
- Effective area: 0.84mm²
Measured Transient Results

Load Transient

$V_{OUT}$

Load

10mA $\leftrightarrow$ 110mA

1$\mu$s

500mV

$F_{OUT}/2$

Reference Tracking

$V_{OUT}$

2.5V/μs

0.9V/μs

$V_{REF}$

0.6V $\leftrightarrow$ 1.1V

1$\mu$s

500mV

$F_{OUT}/2$

CR=1/2

CR=2/3

V$_{OUT}$ Steady State

$V_{OUT}$

Ripple=3.5mV

@ I$_{Load}$=100mA

10ns

100mV

Ripple=2.5mV

@ I$_{Load}$=50mA

10ns

100mV

On-chip edge-time is 100ps

10ns

100mV
Measured Power Conversion Efficiencies

78% @ $I_{Load}=50\,mA$
75% @ $I_{Load}=100\,mA$
65% @ $I_{Load}=150\,mA$
## Comparison Table

<table>
<thead>
<tr>
<th>Publication</th>
<th>Le, JSSC '11</th>
<th>Piqué ISSCC '12</th>
<th>Le, ISSCC '13</th>
<th>Jain, JSSC '14</th>
<th>This work '15</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Process</strong></td>
<td>32nm SOI</td>
<td>90nm</td>
<td>65nm</td>
<td>22nm Tri-gate</td>
<td>65nm</td>
</tr>
<tr>
<td><strong>Conv. Ratios</strong></td>
<td>2/3, 1/2, 1/3</td>
<td>1/2, 2/3</td>
<td>1/3, 2/5</td>
<td>1/2, 2/3, 4/5, 1</td>
<td>1/2, 2/3, 3/4</td>
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<tr>
<td><strong>Phase No.</strong></td>
<td>32</td>
<td>41</td>
<td>18</td>
<td>8</td>
<td>123</td>
</tr>
<tr>
<td><strong>V&lt;sub&gt;IN&lt;/sub&gt;</strong></td>
<td>2</td>
<td>1.2-2V</td>
<td>3-4V</td>
<td>1.225V</td>
<td>1.6-2.2V</td>
</tr>
<tr>
<td><strong>V&lt;sub&gt;OUT&lt;/sub&gt;</strong></td>
<td>0.5-1.2V</td>
<td>0.7V</td>
<td>1V</td>
<td>0.45-1V</td>
<td>0.6-1.2V</td>
</tr>
<tr>
<td>F&lt;sub&gt;S&lt;/sub&gt; @η&lt;sub&gt;Peak&lt;/sub&gt;</td>
<td>300MHz*</td>
<td>50MHz</td>
<td>N/A</td>
<td>250MHz</td>
<td>33MHz</td>
</tr>
<tr>
<td>η&lt;sub&gt;Peak&lt;/sub&gt;</td>
<td>79.8%</td>
<td>81%</td>
<td>74.3%</td>
<td>82.7%</td>
<td>80.0%</td>
</tr>
<tr>
<td><strong>Power Density</strong></td>
<td>860mW/mm²</td>
<td>39mW/mm²</td>
<td>190mW/mm²</td>
<td>250mW/mm²</td>
<td>180mW/mm²</td>
</tr>
<tr>
<td>P&lt;sub&gt;OUT,Max&lt;/sub&gt;</td>
<td>600mW*</td>
<td>10mW</td>
<td>162mW</td>
<td>25mW</td>
<td>152mW</td>
</tr>
<tr>
<td><strong>Ripple Range</strong></td>
<td>N/A</td>
<td>3.8mV-N/A</td>
<td>N/A</td>
<td>43mV-125mV*</td>
<td>2.2mV-30mV</td>
</tr>
<tr>
<td>ΔV&lt;sub&gt;OUT&lt;/sub&gt; @T&lt;sub&gt;Edge&lt;/sub&gt;</td>
<td>N/A</td>
<td>N/A</td>
<td>76mV @50ps</td>
<td>N/A</td>
<td>58mV @100ps</td>
</tr>
<tr>
<td><strong>DVS Speed</strong></td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>2.5V/μs</td>
</tr>
</tbody>
</table>

*Estimated from figure.
Multiple $V_{DD}$ Domains in Converter-Ring

- Cascade NMOS LDO for multiple $V_{DD}$ domains.
- Only $\mu$A of $I_Q$ is drawn from $V_{IN}$.
- Main $I_{LOAD}$ provided by $V_{DCDC}$.

Power Converter Grid?

- On-chip power converter grid with flip chip or through silicon via (TSV) in 3D IC?

Flip Chip

TSV in 3D IC

Converter Grid

- V_{IN} Ball/Via Grid
- Gnd Ball/Via Grid

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Conclusions

• A Ring-Shaped Multiphase Switched-Capacitor DC-DC Converter is proposed for on-chip power delivery.

• Unity gain bandwidth is designed to be a few times higher than the switching frequency of the DC-DC Converter, enabled by
  1. Setting the dominant pole at $V_{OUT}$;
  2. Designing a high speed EA;
  3. Tuning the $V_{DDCO}$ frequency through its supply voltage.

• Possible solutions (NMOS-LDO regulation, power converter grid) are proposed.
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