Foundry WLSI Technology for Power Management System Integration


R&D, TSMC

Outline

● Motivation
  ■ PMIC system integration trends
  ■ Foundry WLSI technology Portfolio

● High Performance Computing System (HPC) on CoWoS
  ■ VR on CoWoS
  ■ Impact of Si interposer

● Mobile AP and PMIC System (MAPS) on InFO
  ■ Power Delivery Network
  ■ PVR on InFO

● Summary & Outlook
Motivation: High Efficiency Power Management System

- **PMIC System Trend:**
  - System on PCB → System on SoC/Package
  - Shared Voltage → Per-core Voltage Control
  - $V_{dd}$ Scaling → Low PDN Impedance Needed
  - Long Battery Life → High Efficiency Voltage Regulator

- **System on PCB → System on SoC/Package**
Motivation: High Efficiency Power Management System

- Shared voltage → Per-core voltage control

- V$_{dd}$ Scaling → 0.74V → Low PDN Impedance

- Long Battery Life → High Efficiency VR → Low Ohmic Loss

Source: 2013 ITRS & JEDEC
System Integration from PCB to Package

Benefits from System on Package

- PDN path: Long → Short
- Discrete component number: Dozen → Several
- Switching frequency: 10 MHz → 100 MHz
  - L: μH → nH
  - C: μF → nF
- Form factor: Large → Small
TSMC WLSI Technology Platforms
from low cost to high performance

**InFO**
- Multi-chip integration
- 3D integration
- Smallest form factor
- Cost competitive

**CoWoS**
- High performance and bandwidth
- Multi-chip integration
- Flexible integration

* WLSI: Wafer Level System Integration
SoC and VR(M) System Design on CoWoS

- **System 1:** VRM on board, SoC on substrate (FCBGA)

- **System 2:** VRM on board, SoC on Si interposer

- **System 3:** VR and SoC on Si interposer
SoC and VR(M) System Design on CoWoS

1. System 1: VRM on board, SoC on substrate
   - PDN path: VRM → PCB → Substrate → SoC
   - PDN L/W: PCB/50/5 mm, Substrate/12/4 mm
   - PDN metal layer: PCB/2, Substrate/10

2. System 2: VRM on board, SoC on Si interposer
   - PDN path: VRM → PCB → Substrate → Si Interposer → SoC
   - PDN L/W: PCB/50/5 mm, Substrate/12/4 mm, Si interposer/12/4 mm
   - PDN metal layer: PCB/2, Substrate/8, Si Interposer /2

3. System 3: VR and SoC on Si interposer
   - PDN path: VR → Si Interposer and Substrate → SoC
   - PDN L/W: Substrate/12/4 mm, Si interposer/12/4 mm
   - PDN metal layer: Substrate/8, Si Interposer /2

FOM: PDN impedance, voltage drop and voltage variation
**PDN Impedance Reduction from Si Interposer**

1. VRM on board, SoC on Substrate
2. VRM on board, SoC on Si interposer
3. VR and SoC on Si interposer

**Interposer mitigates anti-resonance at high frequencies**

**Short interconnect reduces PDN impedance: DC and AC**

Numbers of De-cap to be decreased
Si Interposer Reduces Voltage Drop and Voltage Variation

- DC voltage drop
- Voltage variation (@ 2GHz switching freq.)

- The voltage drop and voltage variation from VR to SoC \( \propto \) PDN Impedance
- The VR and SoC on Si interposer system
  - DC voltage drop: 23% of VRM on board, SoC on substrate system
  - Voltage variation: 80% of VRM on board, SoC on substrate system
Capacitance of Si Interposer Suppresses PDN Z Anti-Resonances

- High conductivity Si interposer suppresses the anti-resonances
- High Si conductivity → High TSV Liner capacitance → More suppression of PDN Z anti-resonance

Cross section of TSV and equivalent circuits
SoC and VR(M) System Design on InFO for Mobile Products

- **System 1: FC and PMIC**
  - PDN path: VRM → PCB → Substrate → SoC
  - PDN routing: in millimeter scale

- **System 2: InFO and PMIC**
  - PDN path: VRM → PCB → InFO → SoC
  - PDN routing: in millimeter scale

- **System 3: InFO with partitioned VR (PVR)**
  - PDN path: VR → InFO → SoC
  - PDN routing: in micrometer scale

- **FOM:** PDN impedance, voltage drop, voltage variation, power response
PI: A measure for power supply stability; related to impedance of power distribution network (PDN)

PDN impedance is

\[ Z_{PDN} = R + j\omega L + \left( \frac{1}{j\omega C} \right) \parallel Z_{VR} \]

where \( Z_{VR} \) is the impedance of voltage regulator.

Low R & L in PDN \( \rightarrow \) Low \( Z_{PDN} \) \( \rightarrow \) Better PI performance
Low PDN Impedance in InFO Package

- PDN impedance: InFO_PoP is 16% of the FC_PoP.
- InFO_PoP: Substrate & C4 Bump eliminated and thin RDL
- Low PDN impedance → High power stability
The PDN Impedance for the InFO + PVRs system

- PDN impedance: 9% of FC & PMIC system
- Resistance: 17% of FC & PMIC system
- Inductance: 9% of FC & PMIC system
The Voltage Drop and Variation for the InFO + PVRs System

- DC voltage drop
  - The voltage drop and voltage variation from VR to AP ∝ PDN Impedance
  - The InFO with PVRs system
    - DC voltage drop: 17% of FC & PMIC system
    - Voltage variation: 25% of FC & PMIC system
Power Response for InFO + PVRs System

- Transient time: Time period for power on from 0 to 1 stable state
- The InFO with PVRs system
  - Transient time: 11% of FC & PMIC system
## Summary of the PI Results

<table>
<thead>
<tr>
<th>System specifications</th>
<th>PDN Z @10MHz</th>
<th>PDN Z @200MHz</th>
<th>Voltage drop</th>
<th>Voltage variation</th>
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<tr>
<td>System 1: VRM on board, SoC on substrate (FCBGA)</td>
<td>1x</td>
<td>1x</td>
<td>1x</td>
<td>1x</td>
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<tr>
<td>System 2: VRM on board, SoC on Si interposer</td>
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<tr>
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<tbody>
<tr>
<td>InFO with PVRs</td>
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<td>0.09x</td>
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<td>InFO &amp; PMIC</td>
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Summary and Outlooks

• Foundry WLSI technology, CoWoS and InFO, provides leading edge solutions for power management system integration.

• The technologies provide excellent PDN performance for low power consumption, low voltage drop and low voltage variation for system design.

• $V_{dd}$ scaling of SoC leads to power system design challenges → TSMC WLSI technology provides the design solution.
Thanks for your attention!