Electrical and Thermal Packaging Challenges for GaN Devices

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October 3, 2016
Outline

- Why GaN?
- Hard-Switching Losses
- Parasitic Inductance Effects on Switching
- Thermal Challenges of Surface Mount Packages
Why GaN?

- Zero reverse-recovery enables efficient hard-switched CCM converters
- Low output capacitance reduces switch charging losses enabling faster switching speeds
- Low input capacitance reduces gate drive losses enabling higher switching frequency
- Higher switching speeds reduce transformers, inductors, and capacitors size
- Lateral structure enables integration

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<table>
<thead>
<tr>
<th></th>
<th>Silicon MOSFET</th>
<th>TI – GaN (HEMT)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Device Structure</strong></td>
<td>Vertical – no integration</td>
<td>Lateral- allows integration</td>
</tr>
<tr>
<td><strong>Rds,on – Area metric</strong></td>
<td>&gt;10 mΩ-cm²</td>
<td>5-8 mΩ-cm²</td>
</tr>
<tr>
<td><strong>Gate Charge</strong></td>
<td>~ 4 nC-Ω</td>
<td>~ 1-1.5 nC-Ω</td>
</tr>
<tr>
<td><strong>Output Charge</strong></td>
<td>~25 nC-Ω</td>
<td>~ 5 nC-Ω</td>
</tr>
<tr>
<td><strong>Reverse Recovery</strong></td>
<td>Significant</td>
<td>None</td>
</tr>
</tbody>
</table>
Why GaN? - 48V to POL

- GaN enables single stage efficient hard-switched POL converter
- Single conversion
  - reduces component count in half
  - ~3x power density improvement
- Hard-switched topology improves transient response

- 48V – 12V Bus Converter
  92-97% Efficient

- 12V POL Multi-phase Buck
  85-93% Efficient

LMG5200POL EVM: 48V to 1V

Texas Instruments
Why GaN? – CCM Totem Pole PFC

• GaN enables CCM Totem Pole PFC
  – No Qrr
  – Low switching losses
• GaN enables higher switching frequency
  – Reduces inductor size
• CCM Totem
  – Lower components
  – 30% higher power density

1kW Totem Pole PFC

Note: Bias loss not included
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Hard Switching Loss

In CCM with positive inductor current, the high-side device dominates the switching losses. Turning on the high-side device faster will reduce the losses due to the inductor conducted through the high-side device during $t_1 - t_2$ and $t_2 - t_3$. $E_{oss}$ and $E_{ch}$ are determined by $C_{oss}$ and $V_{bus}$.

### High Side Loss:

$$P_{hs} = V_{bus} \cdot \frac{I_{ind}}{2} \cdot \left( \frac{t_1 - 2}{\tau} \right) + \frac{V_{bus}}{2} \cdot \frac{I_{ind}}{2} \cdot \left( \frac{t_2 - 3}{\tau} \right) + f_{sw} \cdot (E_{oss} + E_{ch})$$

### Low-Side Loss:

$$P_{ls} = V_{ds_3q} \cdot \frac{I_{ind}}{2} \cdot \frac{t_1 - 2}{\tau}$$
Hard Switching Loss

In CCM with positive inductor current, the high-side device dominates the switching losses. Turning on the high-side device faster will reduce the losses due to the inductor conducted through the high-side device during $t_1 - t_2$ and $t_2 - t_3$. $E_{oss}$ and $E_{ch}$ are determined by $C_{oss}$ and $V_{bus}$.

**High Side Loss:**

$$P_{hs} = \frac{V_{bus}}{2} \cdot \frac{I_{ind}}{\tau} \cdot t_1 - \frac{V_{bus}}{2} \cdot \frac{I_{ind}}{\tau} \cdot t_2 + f_{sw} \cdot (E_{oss} + E_{ch})$$

**Low-Side Loss:**

$$P_{ls} = V_{ds\_3q} \cdot \frac{I_{ind}}{2} \cdot \frac{t_1}{\tau}$$
Hard Switching Loss

In CCM with positive inductor current, the high-side device dominates the switching losses. Turning on the high-side device faster will reduce the losses due to the inductor conducted through the high-side device during $t_1 - t_2$ and $t_2 - t_3$. $E_{oss}$ and $E_{ch}$ are determined by $C_{oss}$ and $V_{bus}$.

High Side Loss:

$$P_{hs} = V_{bus} \frac{I_{ind}}{2} \frac{t_1 - t_2}{\tau} \frac{V_{bus}}{2} \frac{I_{ind}}{2} \frac{t_2 - t_3}{\tau} + f_{sw} (E_{oss} + E_{ch})$$

Low-Side Loss:

$$P_{ls} = V_{ds \_3q} \frac{I_{ind}}{2} \frac{t_1 - t_2}{\tau}$$
Hard Switching Loss

In CCM with positive inductor current, the high-side device dominates the switching losses. Turning on the high-side device faster will reduce the losses due to the inductor conducted through the high-side device during $t_1 - t_2$ and $t_2 - t_3$. $E_{oss}$ and $E_{ch}$ are determined by $C_{oss}$ and $V_{bus}$.

**High Side Loss:**

$$P_{hs} = V_{bus} * \frac{I_{ind}}{2} * \frac{t_1 - 2}{\tau} + \frac{V_{bus}}{2} * \frac{I_{ind}}{\tau} * \frac{t_2 - 3}{\tau} + f_{sw} * (E_{oss} + E_{ch})$$

**Low-Side Loss:**

$$P_{ls} = V_{ds_{3q}} * \frac{I_{ind}}{2} * \frac{t_1 - 2}{\tau}$$
Eoss vs Ech

- $C_{oss}$ is very non-linear for GaN and most high voltage power devices

- $E_{oss}$ is the energy stored in the $C_{oss}$ at a defined $V_{ds}$

$$E_{oss} = \int_{0}^{V_{bus}} C_{oss}(V_{ds}) \cdot V_{ds} \, dV$$

- $E_{ch}$ is the energy dissipated in the high-side when charging the low-side $C_{oss}$

$$E_{ch} = \int_{0}^{V_{bus}} C_{oss}(V_{ds_{-ls}}) \cdot (V_{bus} - V_{ds_{-ls}}) \, dV$$

- $E_{ch} > E_{oss}$ when $C_{oss}$ is larger at low $V_{ds}$

- Any parasitic SW node capacitance will sum with $C_{oss}$ of the low-side fet
  - No snubbers
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Common Source Inductance

- Common Source inductance reduces the $\frac{di}{dt}$ during turn-on and turn-off.
  - Increases power dissipated during the $\frac{di}{dt}$ ramp
- 5nH common source inductance increases turn-on loss by 60%
Gate Loop Inductance

• Gate loop inductance increases the impedance between the gate and the driver.
  – Limits the ability to hold off the GaN device during the Vds ramp
  – Shoot through increases the power dissipated in the high-side device and can cause it to fail due to SOA.

• Gate loop inductance increases ringing
  – Higher stress on gate
  – Ringing can cause the device to turn-on/off
  – Loop resistance is required to dampen ringing

Low-side hold-off versus gate-loop inductance
red = 2 nH, green = 4 nH, blue = 10 nH
# Reduction of Common Source & Gate Loop Inductance

<table>
<thead>
<tr>
<th></th>
<th>Standard Power Package</th>
<th>Kelvin Source Power Package</th>
<th>Integrated Driver Power Package</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Common Source</strong></td>
<td>2nH - 10nH</td>
<td>&lt;1nH</td>
<td>&lt;1nH</td>
</tr>
<tr>
<td><strong>Gate Loop</strong></td>
<td>5nH – 20nH</td>
<td>5nH – 20nH</td>
<td>1nH – 4nH</td>
</tr>
</tbody>
</table>
Power Loop Inductance

• Power loop inductance
  – Increases Ringing and EMI
  – Increases $V_{ds}$ voltage stress
  – Increase switching losses

• Package must be designed to enables low power loop inductance PCB layout

• GaN must be switched without snubber to have high efficiency

$V_{sw}$ ringing versus power loop inductance
red = 2nH, green = 5nH, blue = 10nH, orange = 20nH
CCM Switching Waveforms

LMG3410 HB EVM

1kW Totem Pole PFC

Slew Rate
100 V/ns

Switch Node Voltage (100 V/div)

Time (10 ns/div)

<25V overshoot
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Thermal

- Power packages need to have good thermal dissipation capability
- GaN has high $R_{ds\_on}$ temperature coefficient.
  - Lower junction temperature reduces conduction loss
- Surface mount packages do not dissipate power as well as traditional leaded packages
  - Heat dissipates through PCB
  - Typically have smaller heat spreaders
Thermal Dissipation

**Power dissipation:** ~12 W
(50°C ambient and 110°C max junction temperature)

\[
\theta_{JC} - 0.3 - 0.8 \text{ K/W} \\
\theta_{TIM} - 1.5 - 8 \text{ K/W} \\
\theta_{HS} - 1.6 - 5 \text{ K/W}
\]

**Power dissipation:** ~7 W
(50°C ambient and 110°C max junction temperature)

\[
\theta_{JC} - 0.3 - 0.8 \text{ K/W} \\
\theta_{PCB} - 3.0 - 10 \text{ K/W} \\
\theta_{TIM} - 1.8 - 10 \text{ K/W} \\
\theta_{HS} - 1.6 - 5 \text{ K/W}
\]
Package Thermal Pad

• Area of thermal pad must be large enough to reduce thermal resistance of TIM

• Thermal pad must have sufficient thickness to spread heat over TIM

\[
\Delta T_{TIM} = \frac{P_{diss} \times A_{TIM}}{d_{TIM} \times \lambda_{TIM}}
\]
## Package Comparison

<table>
<thead>
<tr>
<th>Package</th>
<th>TO220</th>
<th>QFN</th>
<th>Bumped Die</th>
<th>Embedded</th>
<th>TOLL</th>
<th>Sintered Dual Cool</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common Source Ind</td>
<td>--*</td>
<td>++</td>
<td>++</td>
<td>++</td>
<td>++</td>
<td>++</td>
</tr>
<tr>
<td>Gate Loop Ind</td>
<td>--</td>
<td>++</td>
<td>++</td>
<td>++</td>
<td>++</td>
<td>+</td>
</tr>
<tr>
<td>Power Loop Ind</td>
<td>--</td>
<td>++</td>
<td>++</td>
<td>++</td>
<td>++</td>
<td>+</td>
</tr>
<tr>
<td>Thermal</td>
<td>++</td>
<td>+</td>
<td>-</td>
<td>+</td>
<td>+</td>
<td>++**</td>
</tr>
<tr>
<td>Cost</td>
<td>++</td>
<td>++</td>
<td>++</td>
<td>-</td>
<td>+</td>
<td>--</td>
</tr>
</tbody>
</table>

* Additional kelvin source pin eliminates common source inductance

** Includes isolation
Conclusions

• GaN’s lower switching losses enables high efficiency and high density designs
  – No reverse recovery
  – Low Qoss and Qiss

• Low inductance package is required to realize GaN switching performance
  – Low common source inductance to reduce losses during di/dt phases
  – Low gate loop inductance to hold device off and reduce gate ringing
    • Integrating the driver in the package will minimize gate loop and common source inductance
  – Package must enable low power loop inductance PCB layout
    • Power loop must be designed without snubbers

• GaN package must have good thermal performance
  – Large thick power pad to spread heat and lower TIM drop
  – Direct thermal connection to heat sink eliminates PCB thermal resistance
Thank You