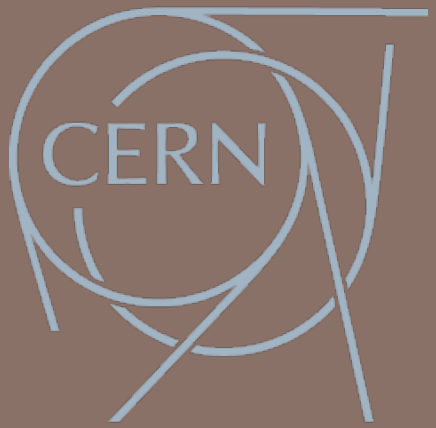
UNIVERSITY OF UDINE

Department DPIA
Via delle scienze 206
33100 Udine (UD), Italy



POWER MOS GATING OPTIMIZATION FOR BALANCING EFFICIENCY VS. RELIABILITY IN HARD-SWITCHING CONVERTERS

Michelis[1] S., Faccio[1] F., Ripamonti[1] G., Blanchot[1] G. and Saggini[2] S.
[1]CERN PH dept, ESE group, Geneva, Switzerland
[2]DPIA University of Udine

Assistant professor Stefano Saggini
PowerSoC Madrid (Spain)

Outline

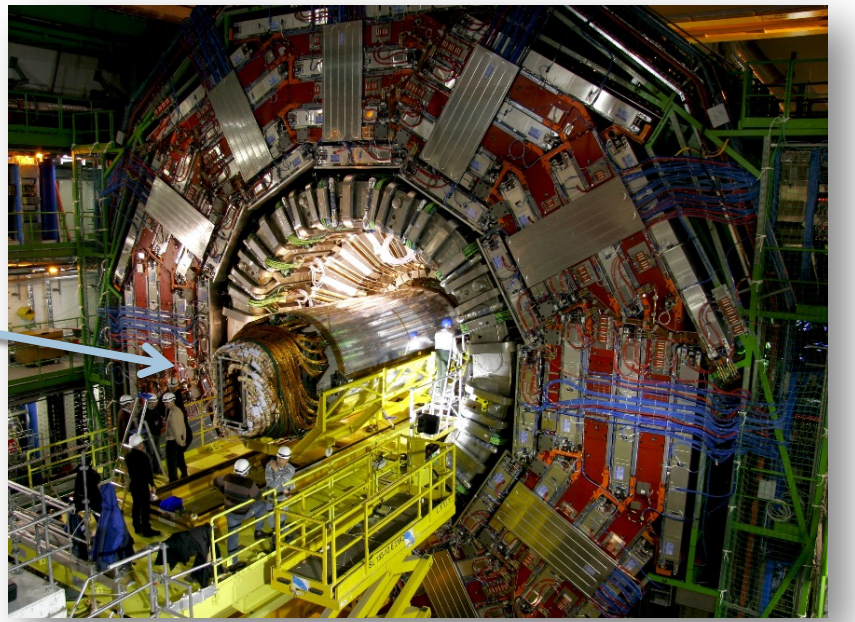
- Tracker supply application
- Integrated DC-DC power train project
- Reliability
- Proposed architecture
- Conclusions

Application

Conditions in the experiments:

- Magnetic flux density is about 8 T
- High radiation level
- Temperature: −20 to +150 °C
- Limited material budget

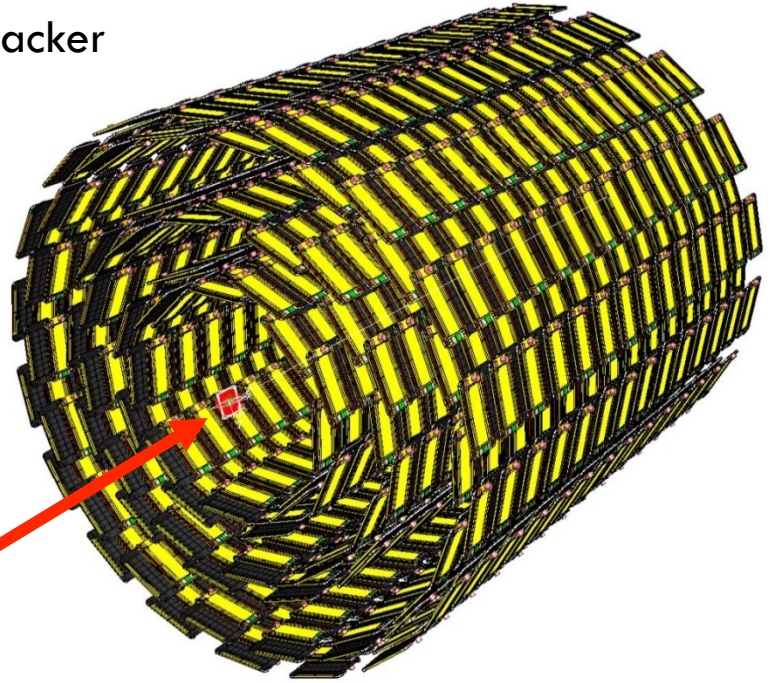
Power distribution scheme of the CMS tracker

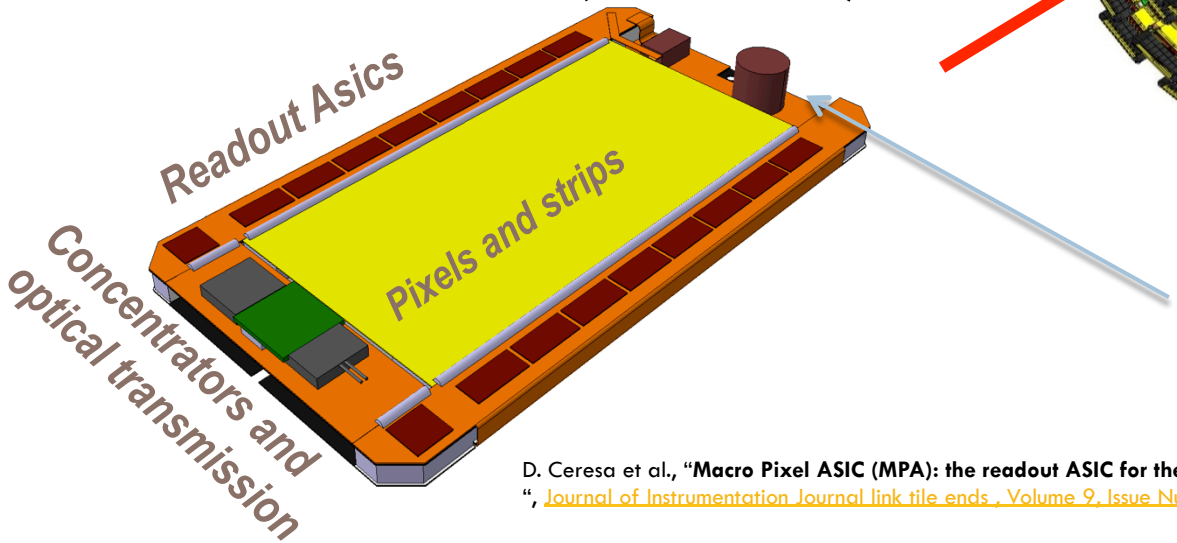


Converter specifications

- Vin=2.5V
- Vout=0.6-1.5V
- Iout= 0A- 3A
- f=4-10MHz
- L=50-100nH (Air-core)

New CMS tracker design



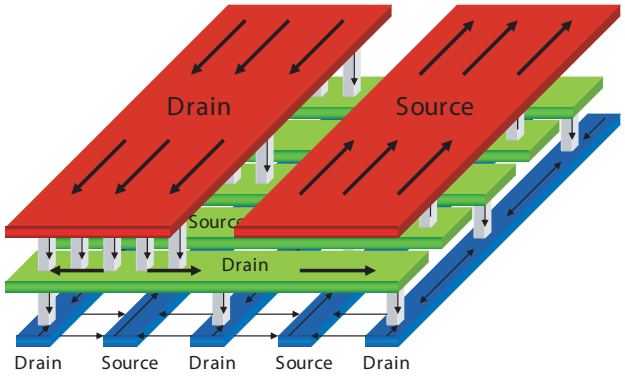


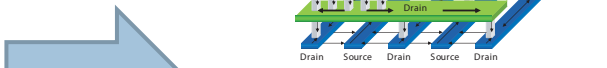
DC-DC converters

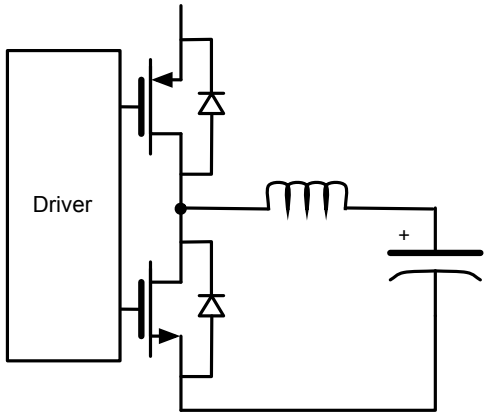
D. Ceresa et al., "**Macro Pixel ASIC (MPA): the readout ASIC for the pixel-strip (PS) module of the CMS outer tracker at HL-LHC** ", Journal of Instrumentation Journal link tile ends , Volume 9, Issue Number Tile Start November 2014

Power train design

- 130nm IO MOS
  - In low voltage CMOS R_{dsON} resistance depends on the metallization more than channel resistance







- Bump bonding to reduce the connection Impedance
- Use of a CMOS power train

CMOS power train for low voltage

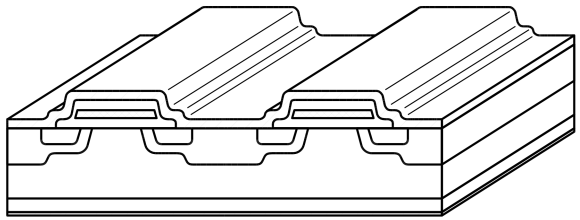
- The CMOS power train advantage for low voltage and low power application
  - Simple n-well architecture with less junction isolation problem (lower maximum n-well voltage)
  - Simplest driving system without bootstrap capacitor (external or integrated)

Theoretical Switch optimization method

- The total loss of the due to each switch can be expressed as

$$R_{DSOn} = Kr_{dsOn} / A$$

A is the Area



$$Q_{gd} = A\, Kq_{gd}$$

$$Q_g = A\, Kq_g$$

Conduction losses

Switching losses

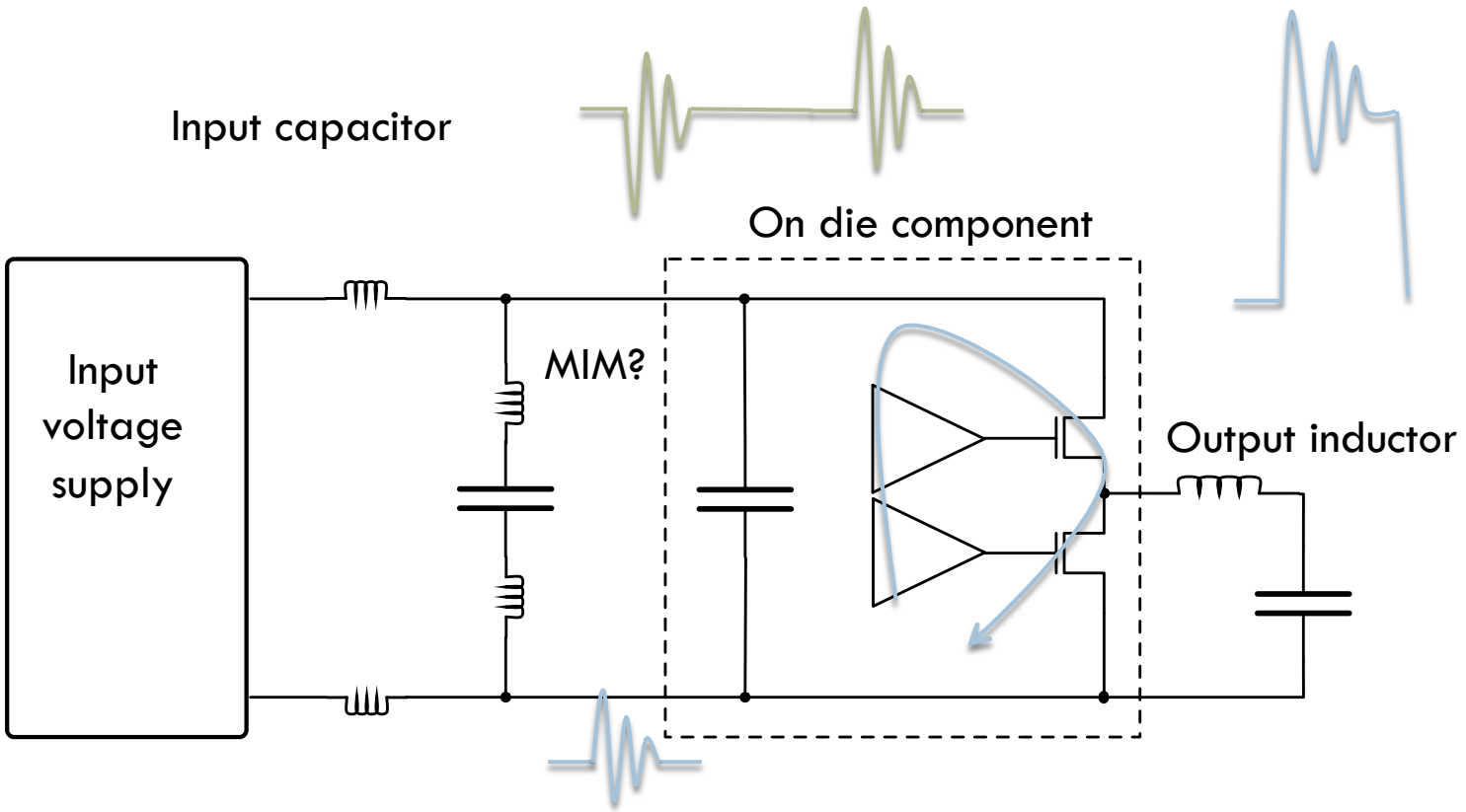
Driving losses

$$P_{lossMOS} = I_{rmsOn}^2\, Kr_{dsOn} / A + f\,(V_{Off} I_{On}\, A\, Kq_{gd} / (2 i_g) + V_{driver} A\, Kq_g)$$

i_g term is unknown

Reliable power converters

- Analysis of spikes to determine a drive current I_G in order to have a reliable power converter

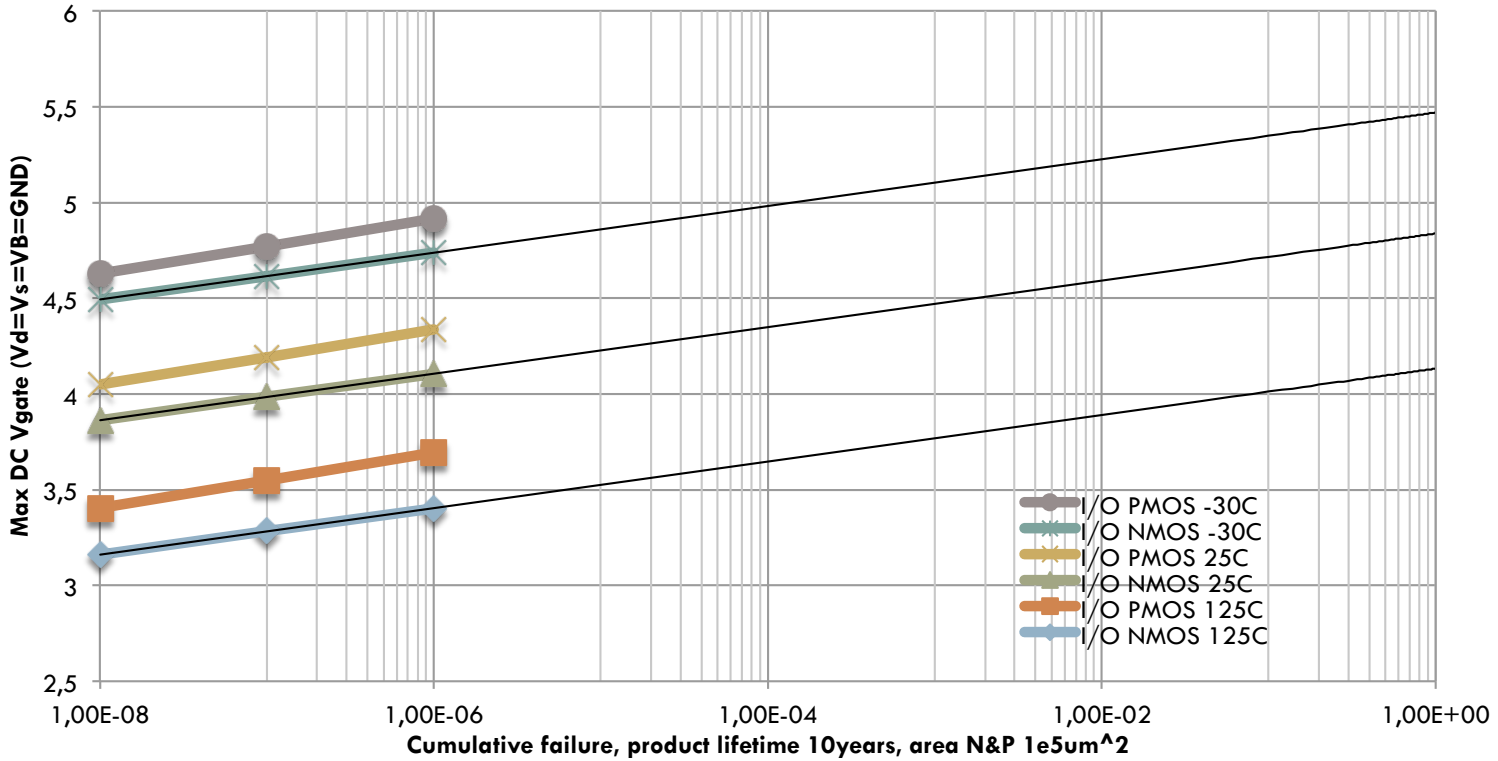


Spikes effects

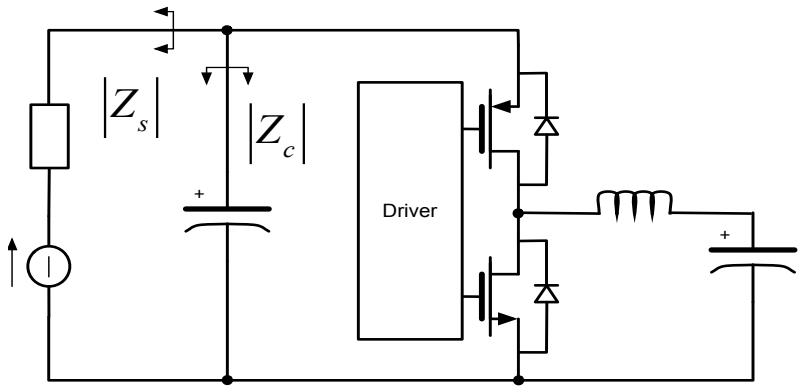
- With I_L>0 HS turn ON and OFF:
  - High voltage spikes on HS V_{ds} (For snapback issue reduction of Vds max on HS)
  - High voltage spikes on HS V_{gs} limit on the oxide voltage failure
  - High voltage spikes on LS V_{gd} limit on the oxide voltage failure and HCI degradation

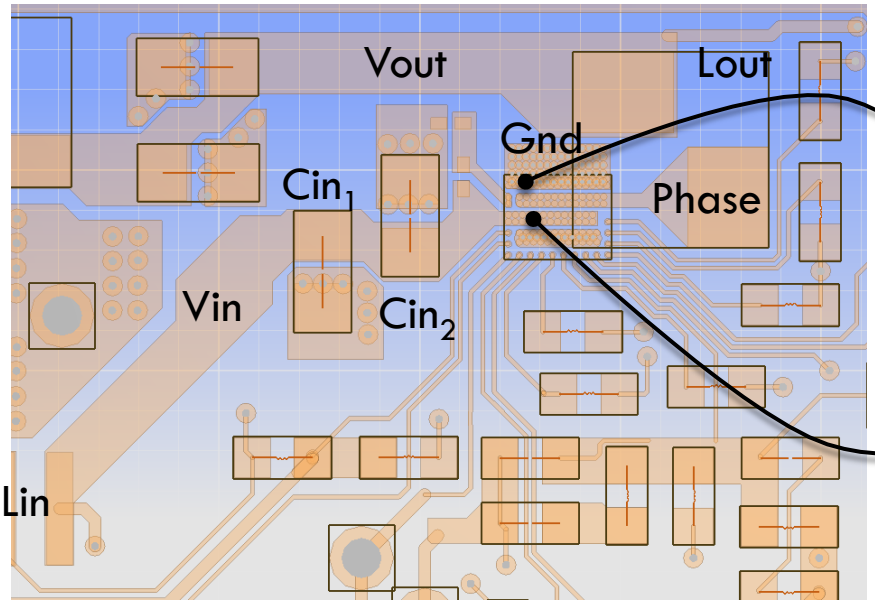
Reliability for gate oxide peak voltage

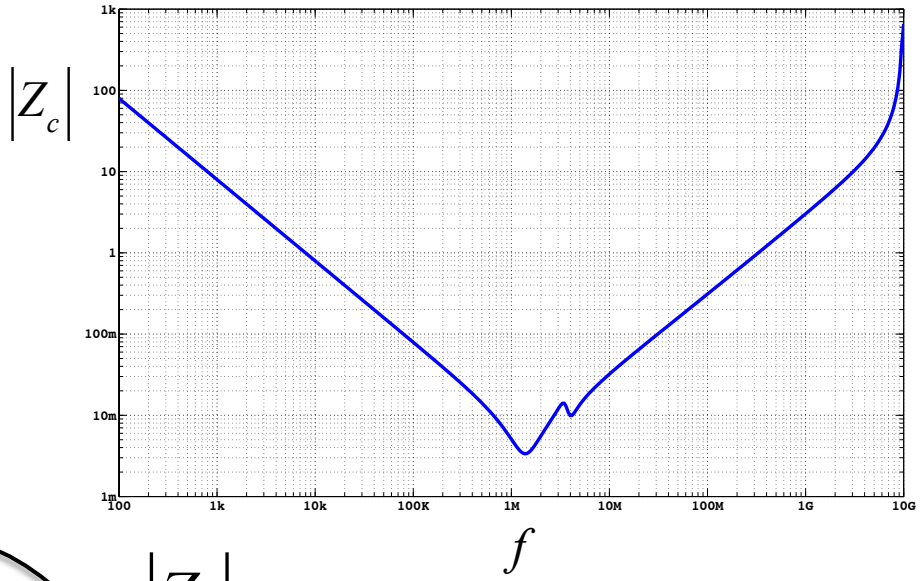
- Relation between the peak voltage on oxide and failure



Converter board impedance model





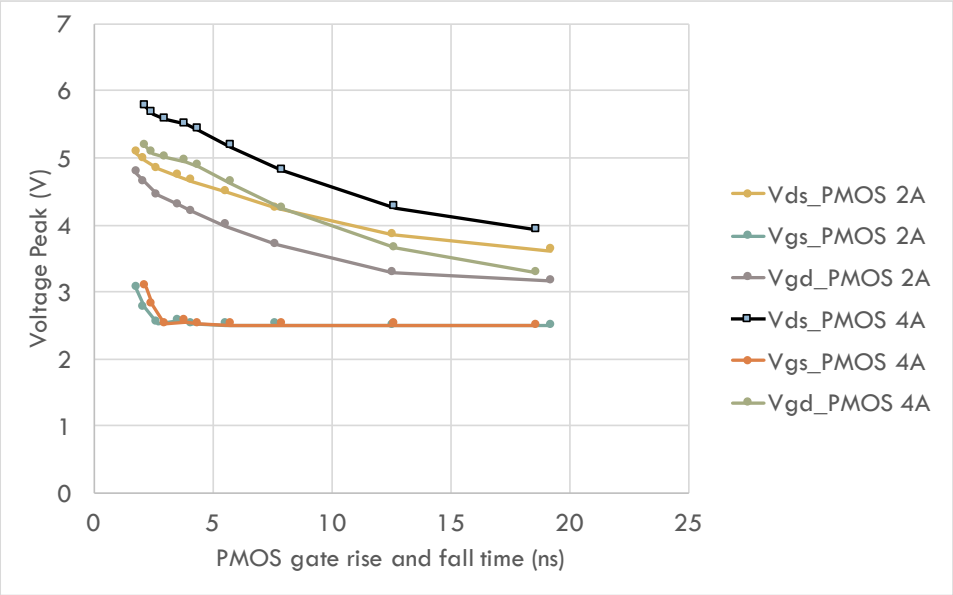


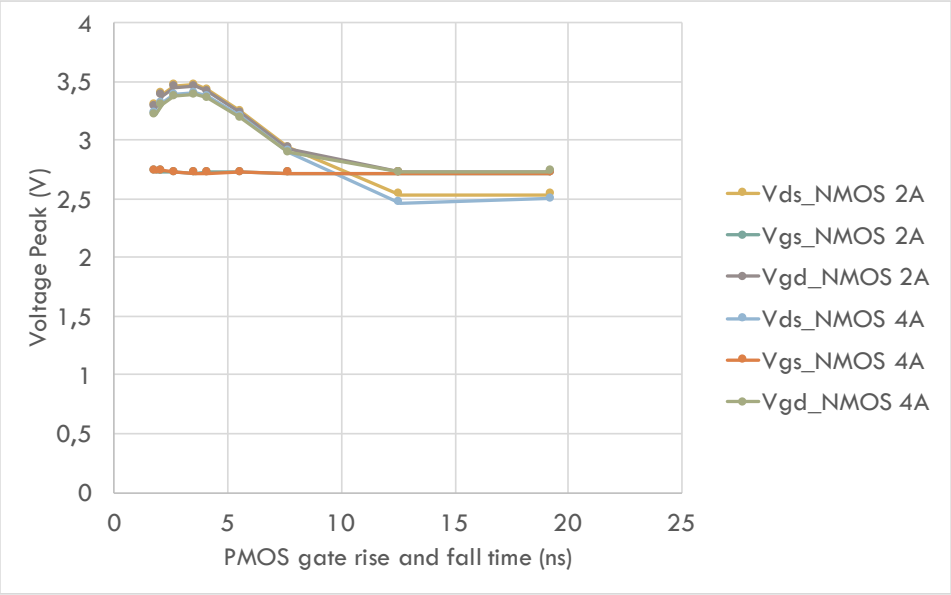
$|Z_s|$ Is dominated by the input inductor

$|Z_c|$ Impedance of the input capacitor network

Relation between spikes and I_g

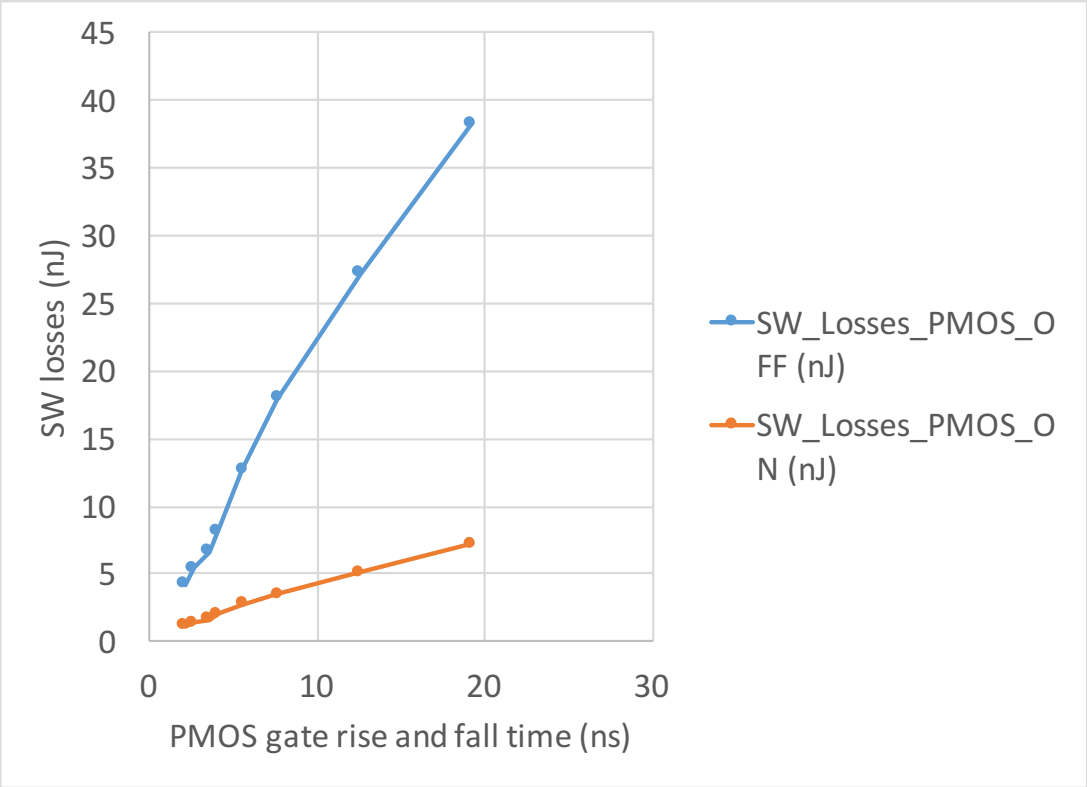
- Peak voltage as a function of the driver Current in the Power MOS Stage @ 2 A and 4 A of load current





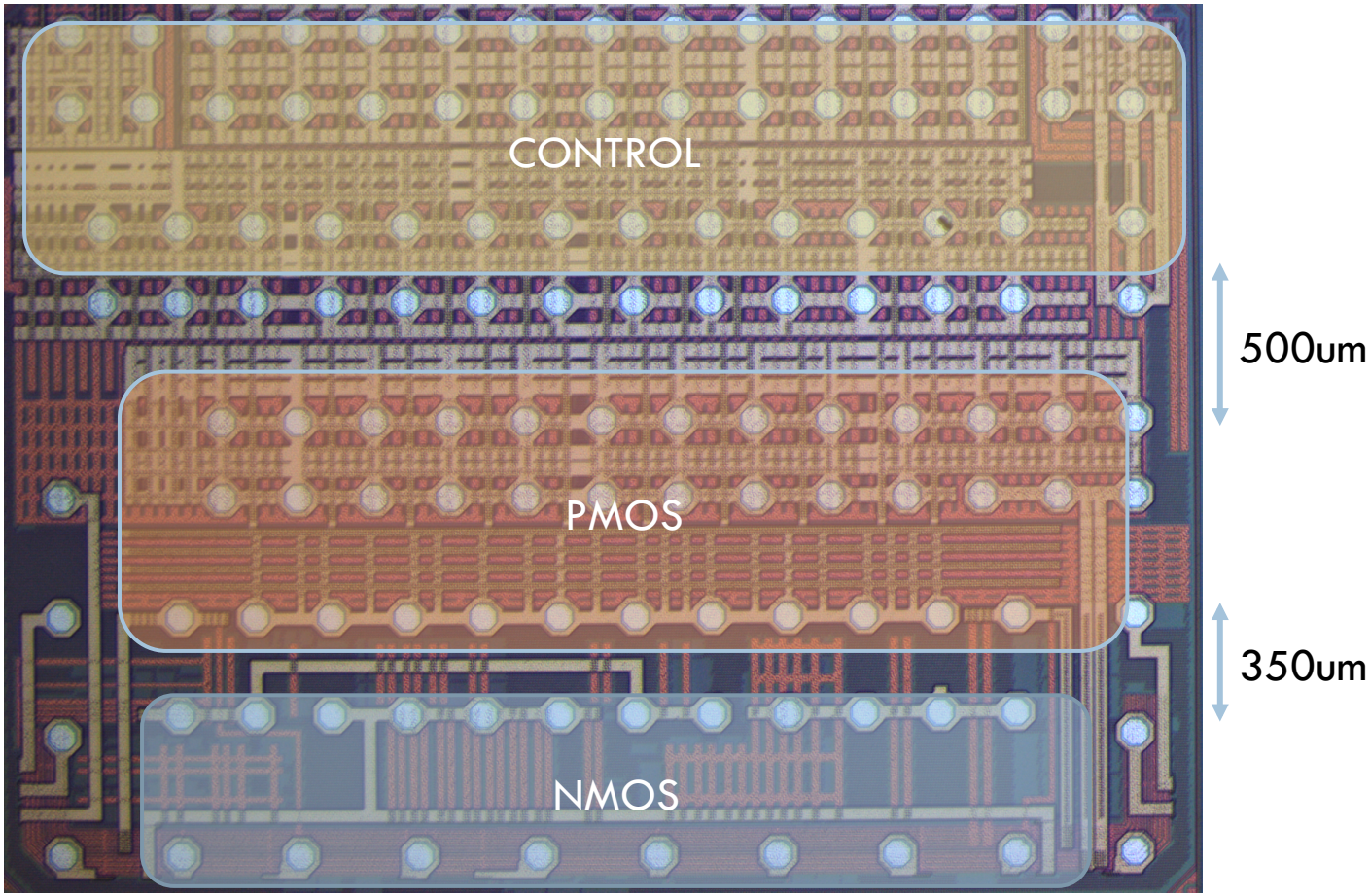
Relation between spikes and I_g

- Switching energy losses as a function of the rise and fall time of the gate voltage of the power stage @ maximum load



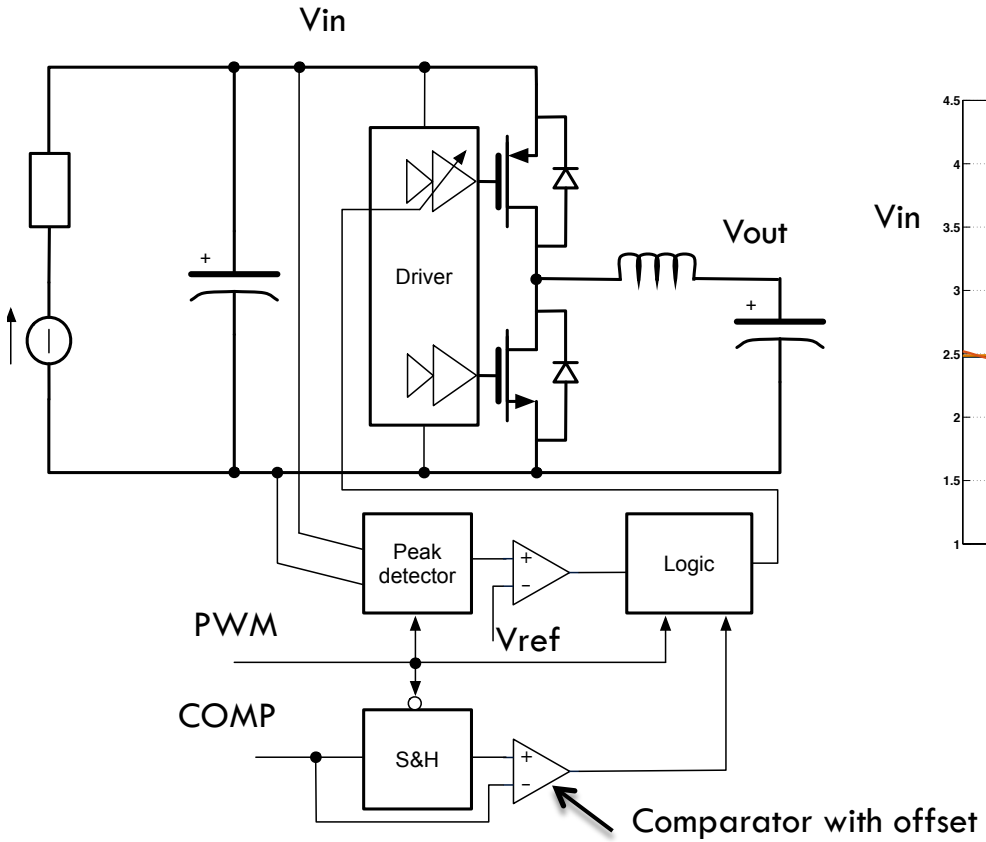
Power train optimization

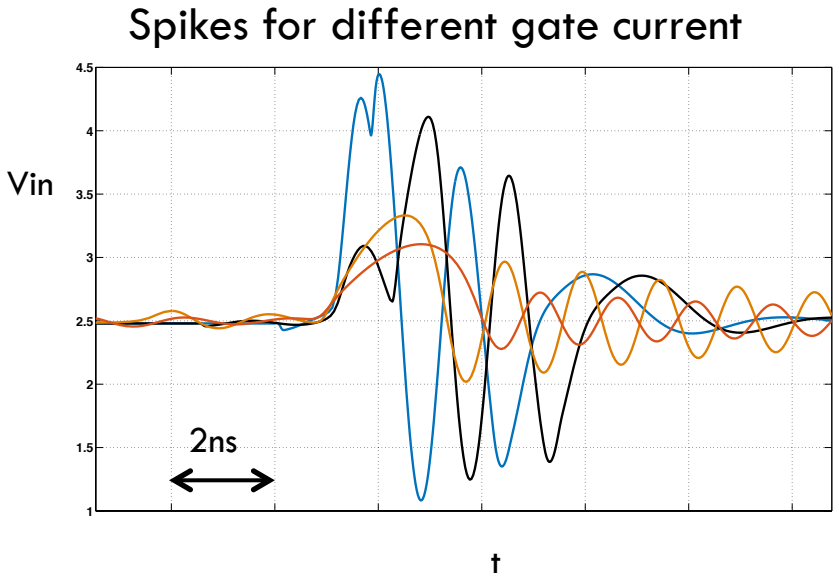
- Test chip dimension 2.78 mm X 2.1 mm



Proposed adaptive method

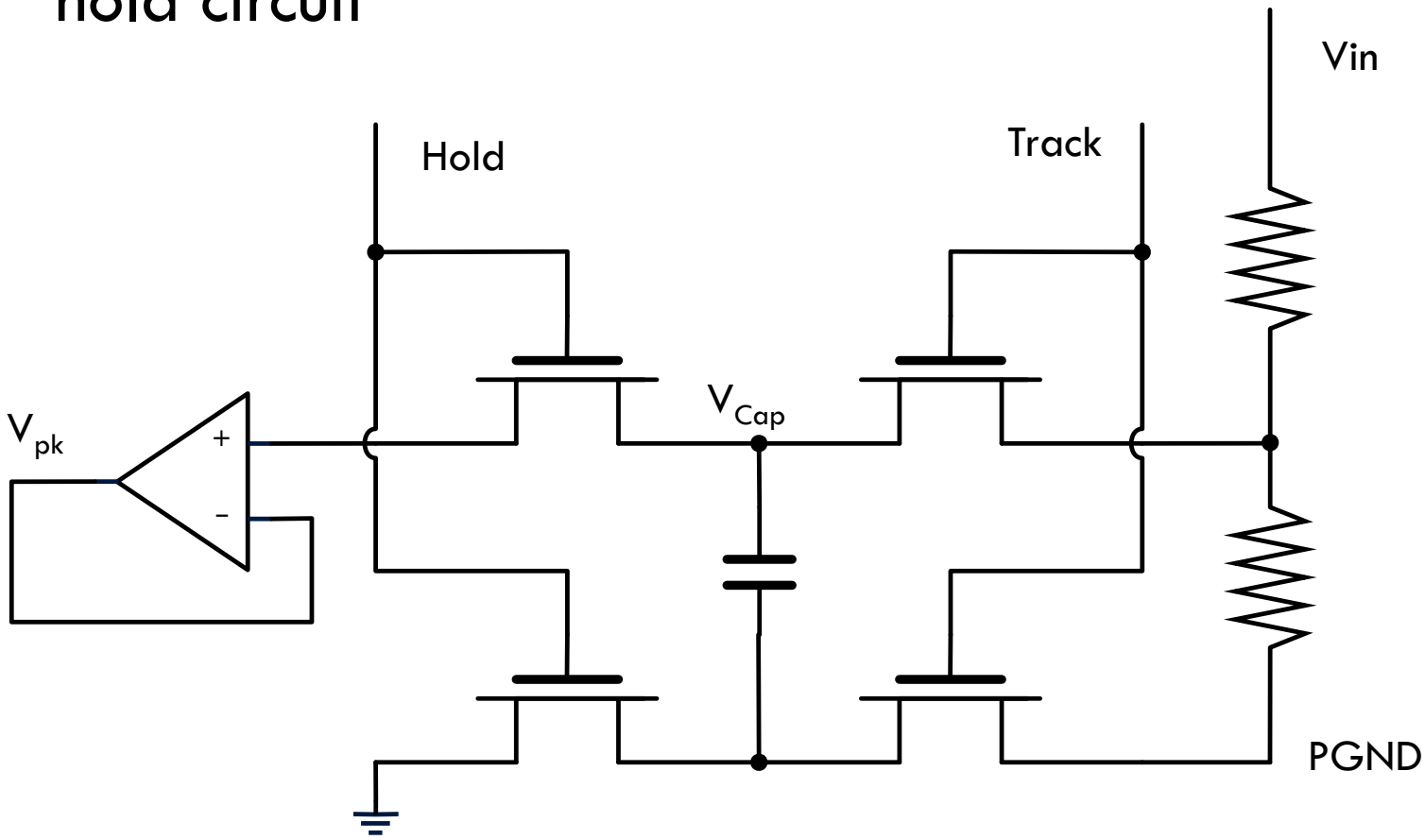
- Proposed control method for spikes on the input voltage





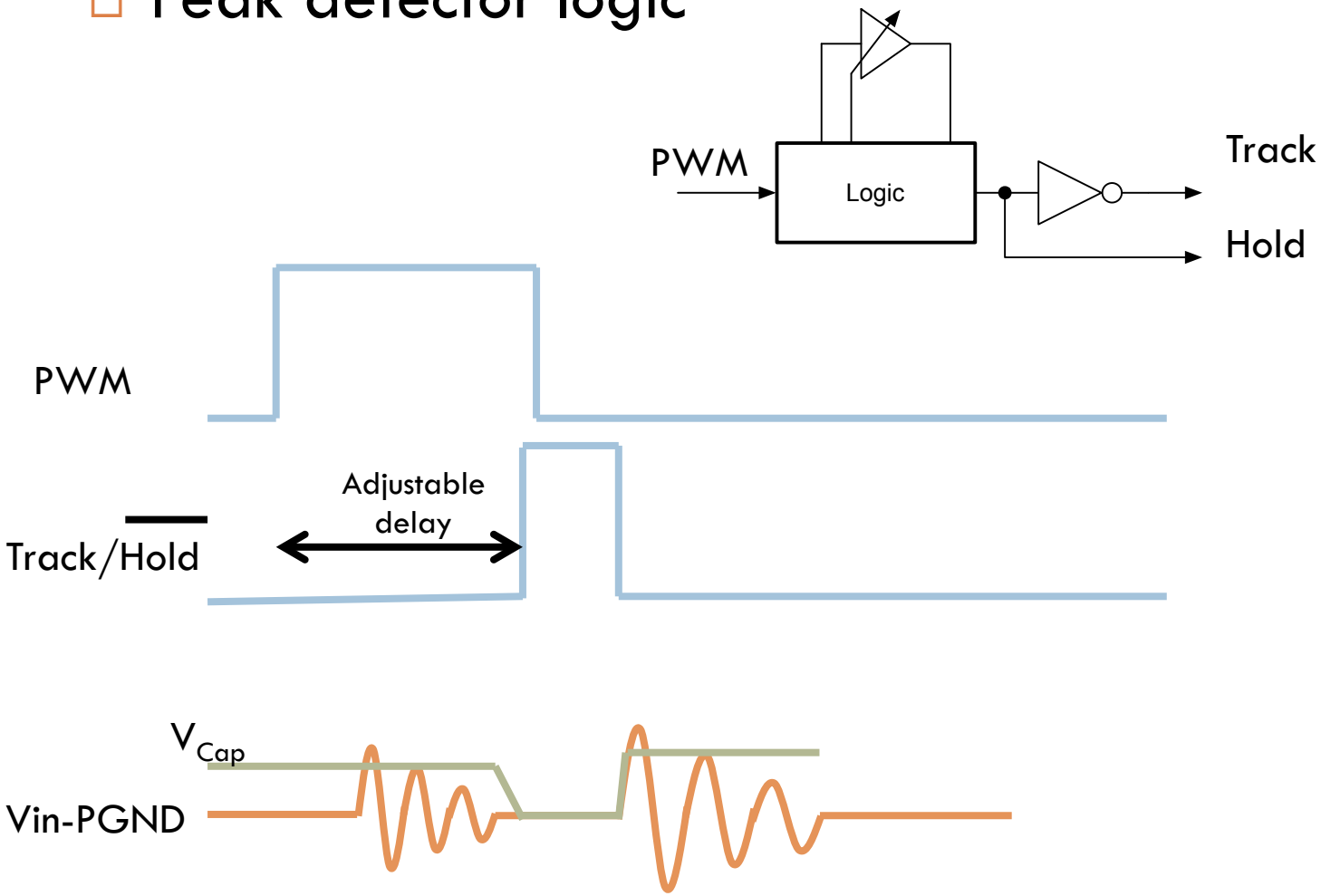
Schematic of the peak detection

- Peak detection by an High frequency sample and hold circuit

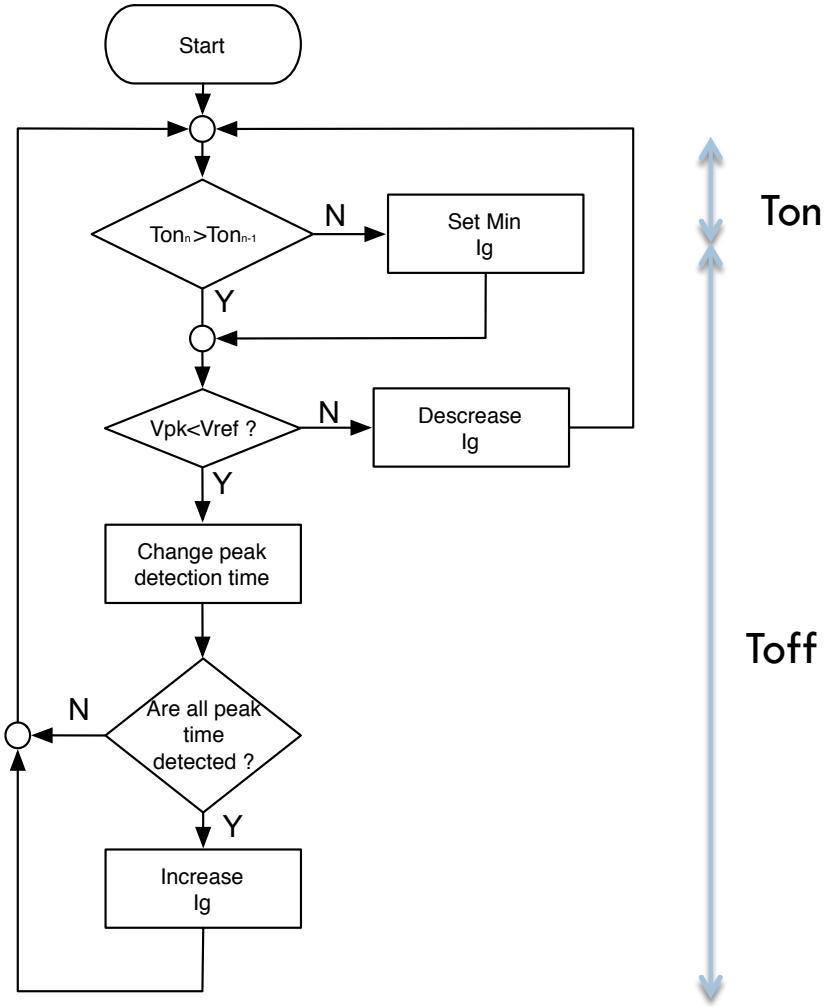


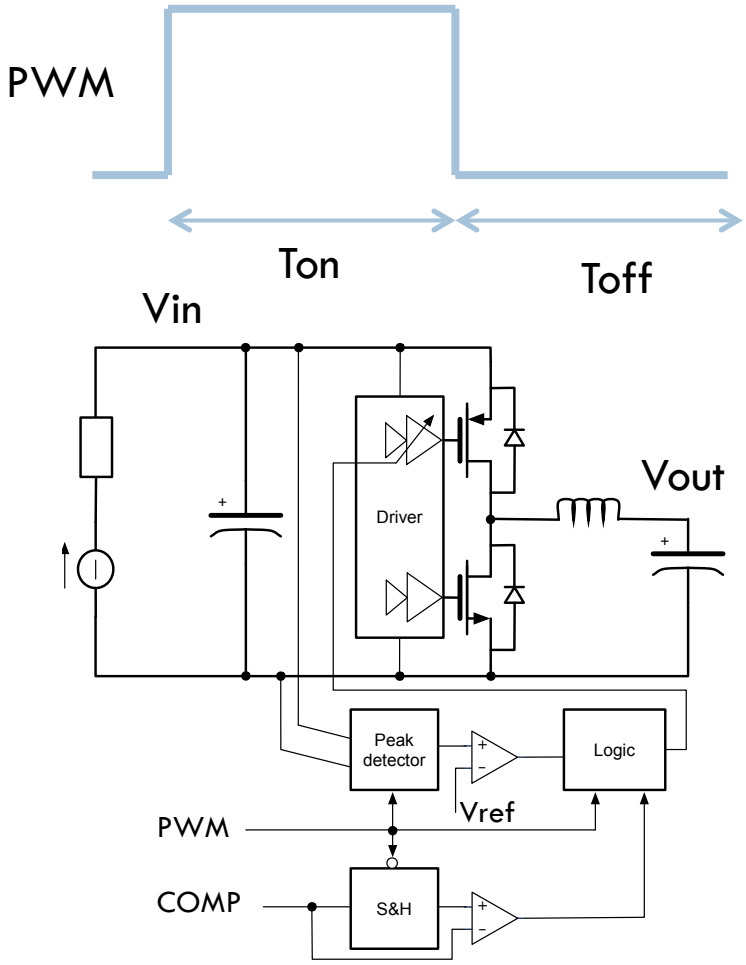
Peak detector logic

- Peak detector logic



Optimization algorithm





Conclusions

- The proposed architecture optimize the rise and fall time in order to optimize the efficiency guaranteeing the converter reliability
- Test chip with the peak voltage track and hold
- Assembly in October and Laboratory test in November