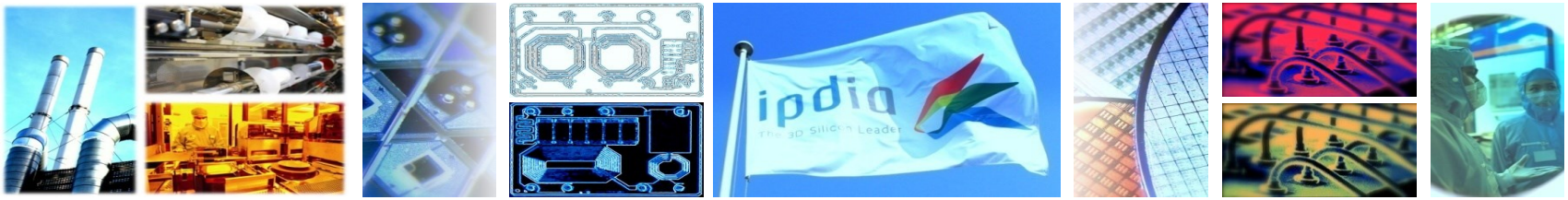
About IPDiA

- Independent High-Tech company located in Caen, Normandy, France
- Dedicated to manufacturing of leading edge Integrated Passive Devices (PICS)
- 20M$ revenue, 130 people and operating own silicon wafer fab
- Strong R&D team collaborating with leading research institutes



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Innovative Smart PICS Core LC Filter Concept for Output Filtering in high frequency DC-DC Converter Applications

Mohamed Mehdi Jatlaoui, Frederic Voiron

2014.10.04

Outline

- Silicon integrated technology
  - 3D structure
  - PICS for power conversion
- Application examples
  - Load decoupling
  - HF embedded converter
- A novel approach for LC output filter
  - Main idea
  - Model & Simulation
  - Physical implementation
- Outlook

Silicon Integrated Technology

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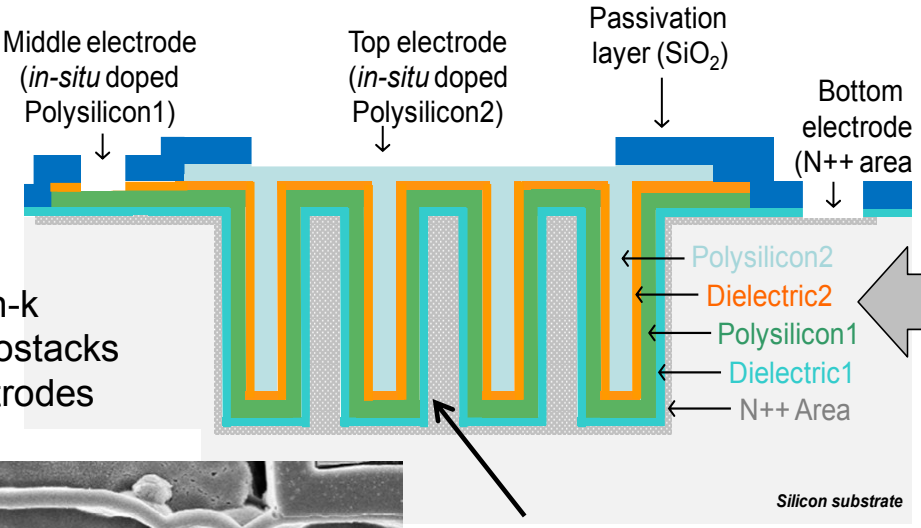
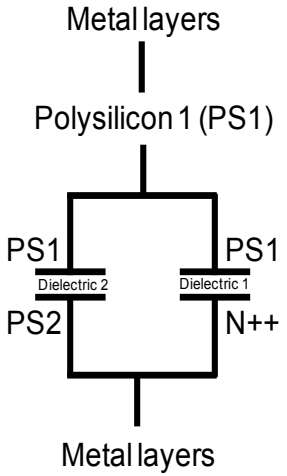
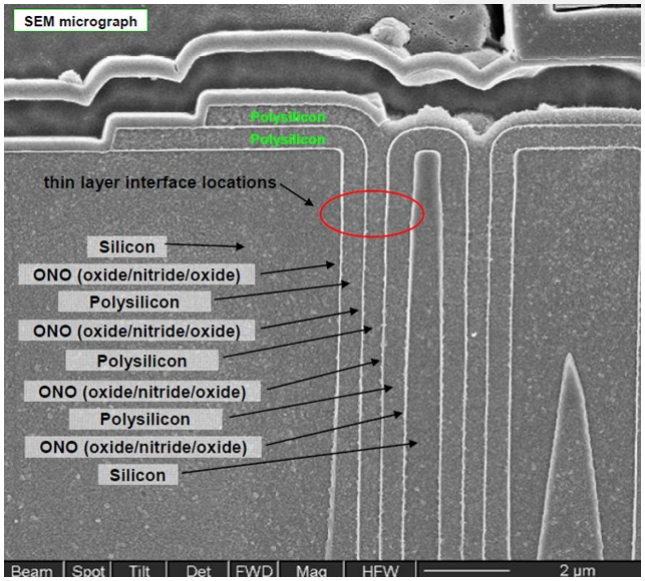
3D structure

2 parallelized capacitors in a MIMIM architecture to increase the capacitance value

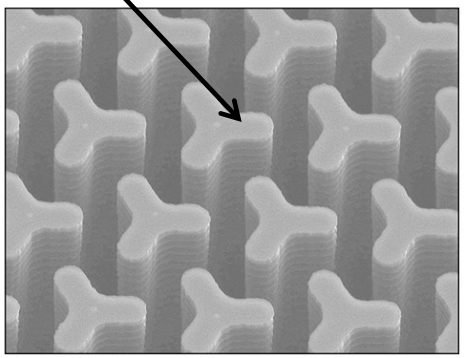


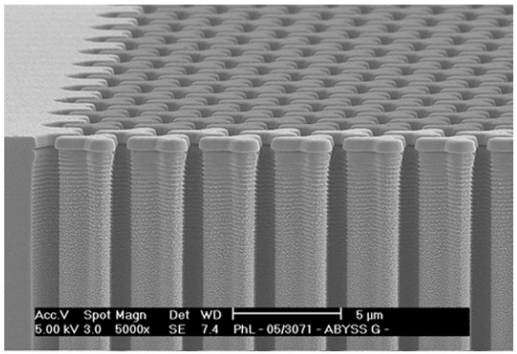


Based on high-k materials nanostacks & barrier electrodes



Tripod

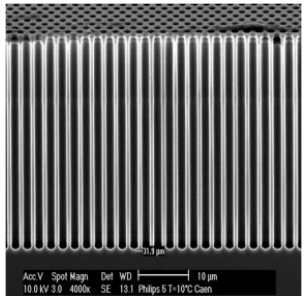
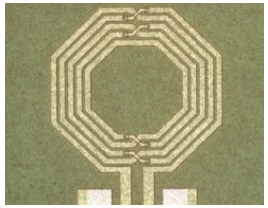
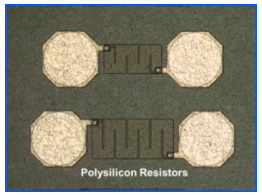


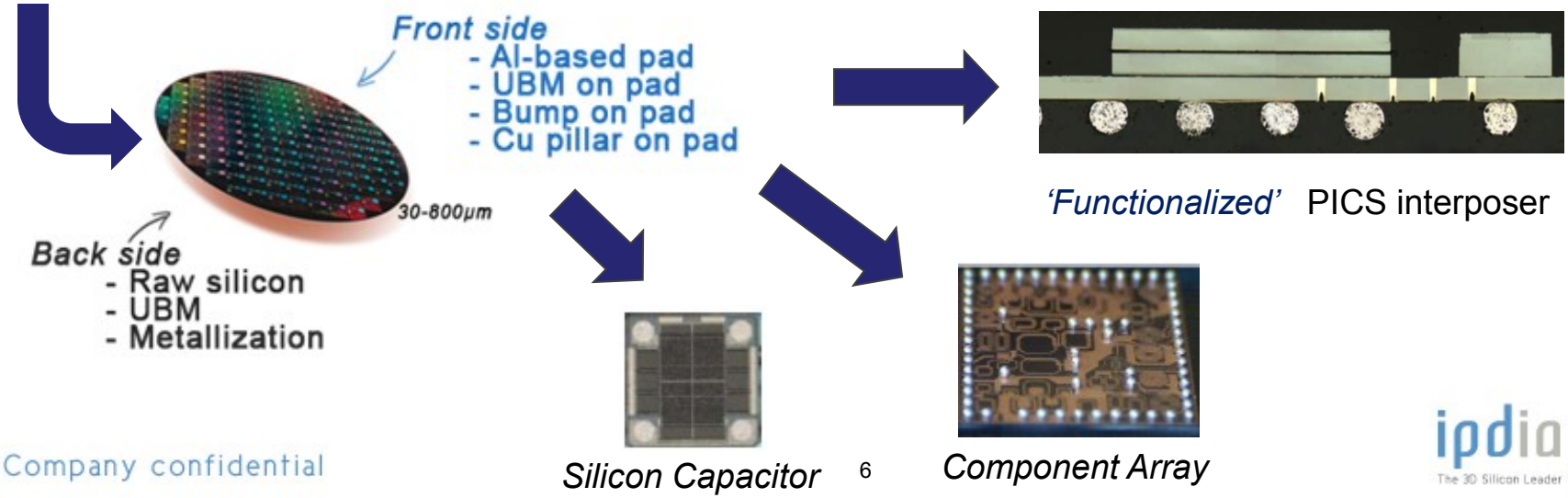


Tilted SEM view

IPDiA technology

– PICS (Passive Integrated Common Substrate) technology

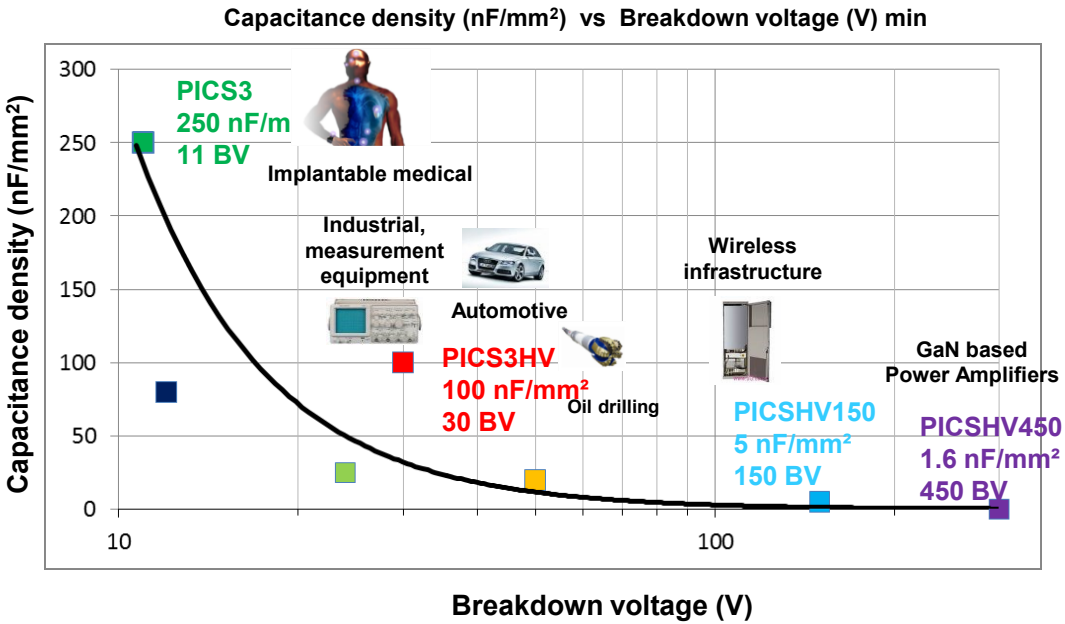
3D capacitors (trench Capacitors)	MIM Capacitors	Inductors	Polysilicon Resistors	TSVs	Diodes
	80pF/mm² Matching <1%				
		Up to 3 metal Top metal > 10um Superior Q	*Matchnig < 0.5%* *800 Ω/□* MΩ resistor / mm²		Surge protection ESD / OVS



PICS – 3D cap component overview

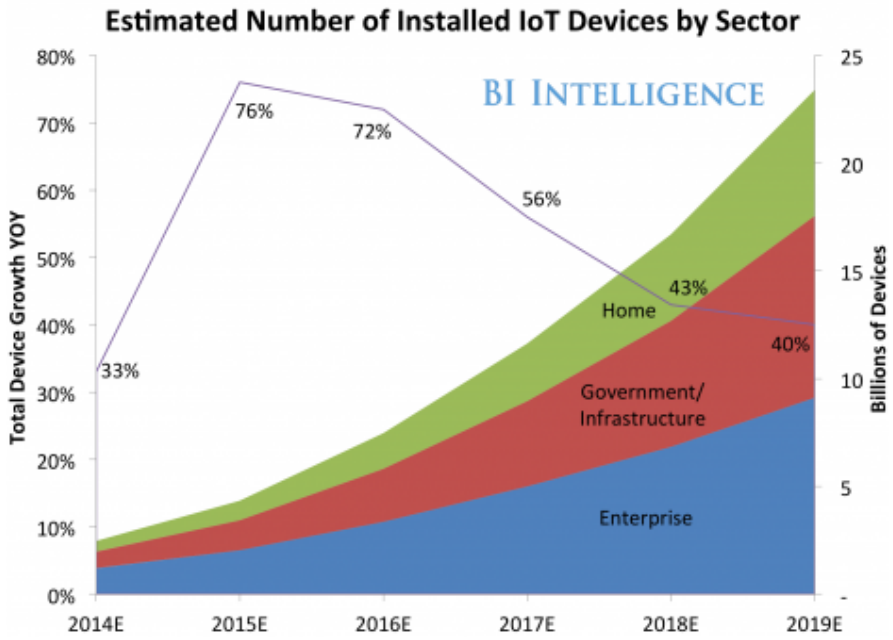
- **3D Silicon capacitors**

  - **5 PICS platforms available**
    - Capacitance density up to 500nF/mm²
    - Low Profile (down to 80µm)
    - Low ESR / Low ESL specific structures
  - **Voltage rating**
    - Breakdown voltage from 5 to 500V
    - High dielectric isolation typ. <1nA/mm² (25° C/VUse)
    - Temp linearity <100ppm/K
    - Voltage linearity <100ppm/V

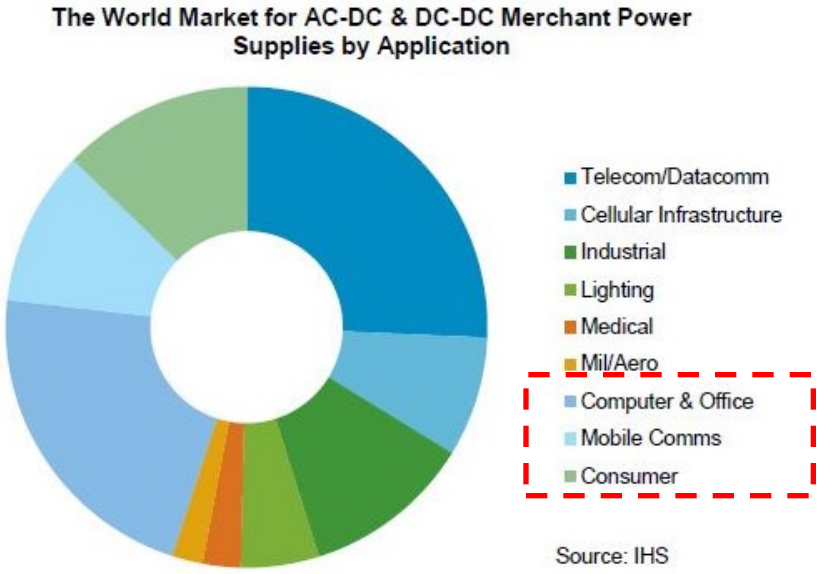


  - **Reliability**
    - > 10 yrs @ operating voltage @ 100° C
    - FIT (Failure in Time) below 1 at 225° C
    - Mechanical shock tests
    - Thermal cycling tests : up to 3000 cycles in std conditions and 330 cycles in harsh conditions

IoTs Ecosystem Sizing



Source: *BI Intelligence Estimates*



- At least one converter per device = global annual as high as 8$B revs for low power step down after 2016 → Growing market for specialized passives !

- The IoTs rely on a new paradigm of " self sustainability"

  - Highly integrated designs with very low-power functions
  - Local harvesting and compact storage
  - Outstanding power efficiency and voltage versatility
  - Ultra-thin systems - typ. < 0.4mm

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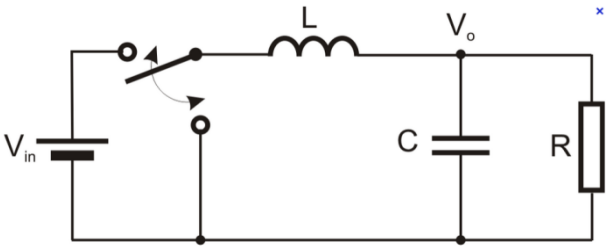
PICS for power conversion

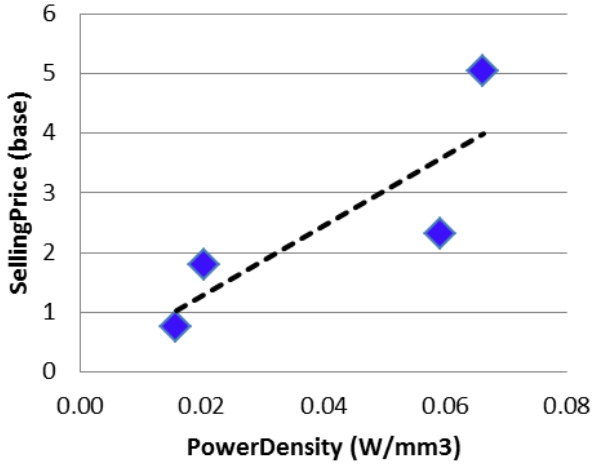
Confidential

+ advanced assembly options ...

Switch-mode conversion

- Every electrical device requires a power supply… so every tablet, or smartphone or IoT requires capacitors
- For high efficiency / voltage versatility, LDOs are not an option: i.e. resistive losses linear with conversion ratio !!
- Switch-mode DC-DC converter "Brick Modules" require capacitor smoothing for the input filters and the output filters.
- Most of the power density lost in the passives:
  - **40nm PMIC@100Mhz → 20Wmm²**
  - **<1W/mm² when combined with passives**
- Making converters smaller and more efficient requires break through on passives !





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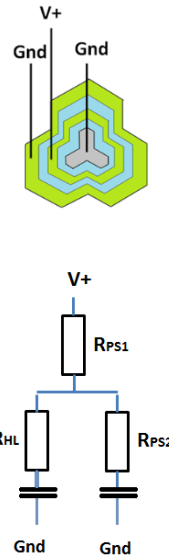
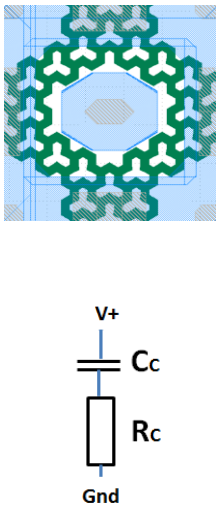
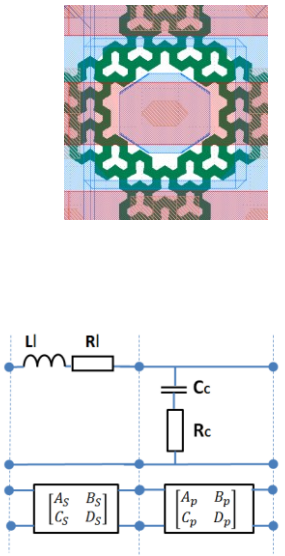
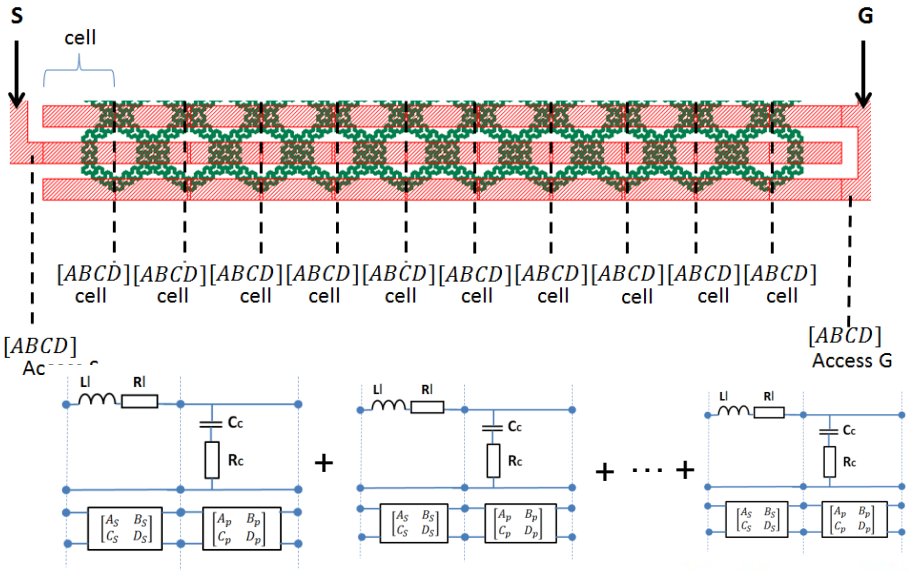
PICS Mosaïc architecture

- Natural design in PICS yield a distributed capacitor
  - Microstrip like propagation structure co-implementing S/GND paths
  - Field confinement / controlled propagation in broadband
  - Impedance tuning including R/L cancelling for power shaping

Micro → Macro

Tripod with double SIS	Cell	Interconnects + cell	Cascaded cells
			

Application examples

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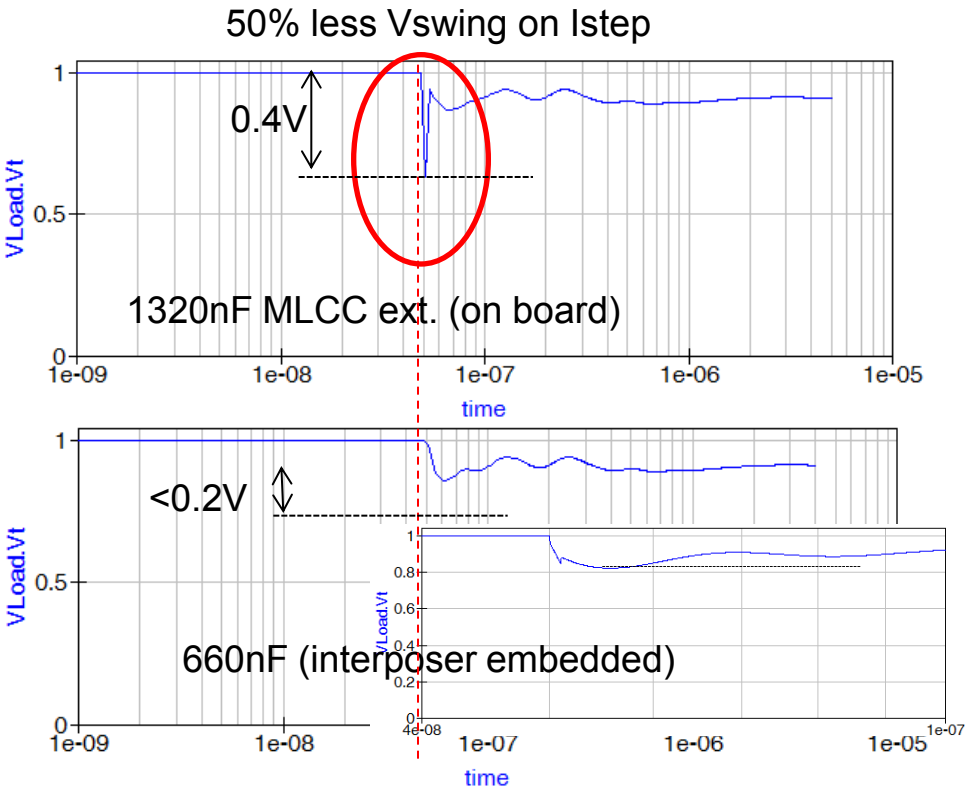
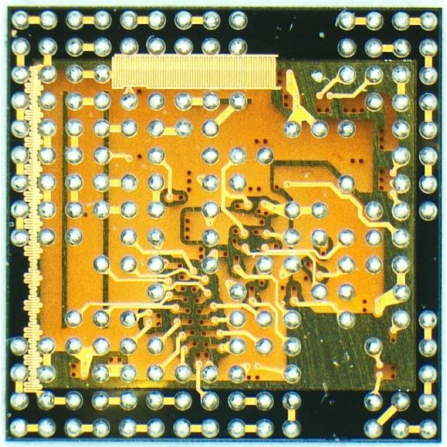
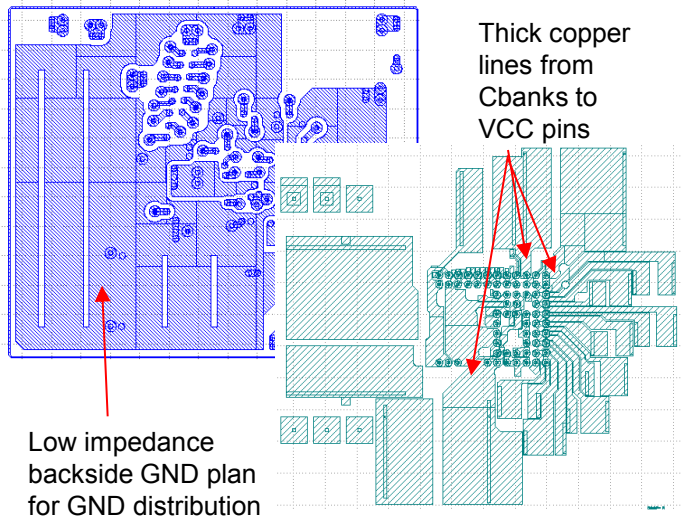
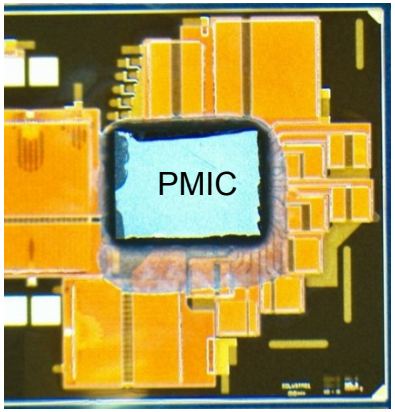
Load decoupling

- PDN local decoupling for embedded µC
  - 1V grid
  - Load = 3mOhm/3nH
  - 10A step / 1ns
  - Bulk decoupling stays on board
- PICS C_interposer to catch fast transient
  - 3 x 220nF capacitor banks
  - Optimized ESL < 10pH
  - Reduced stray inductance <50pH (TSV + PADs)



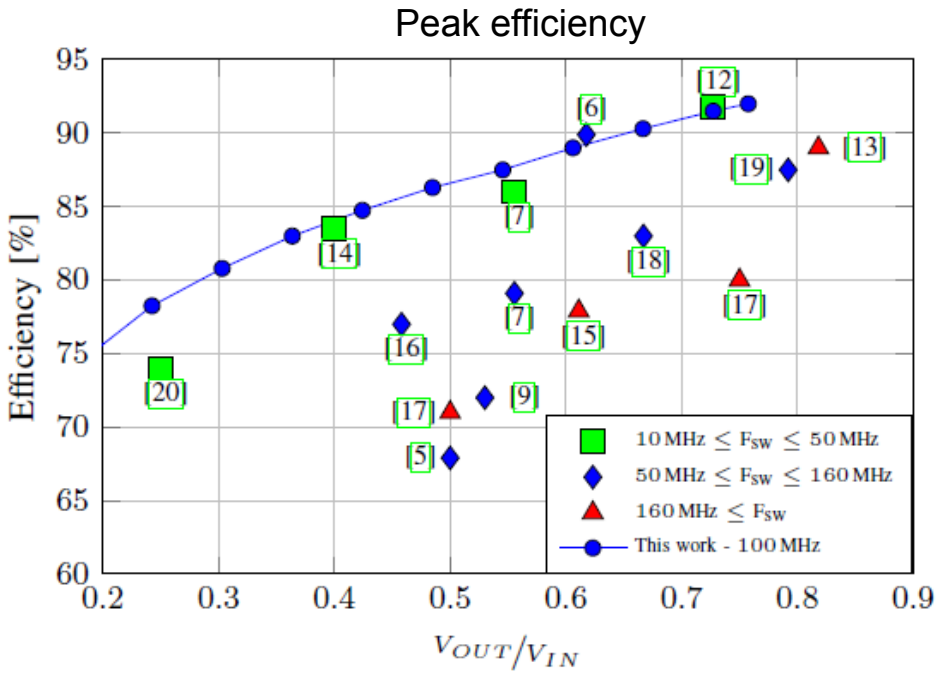




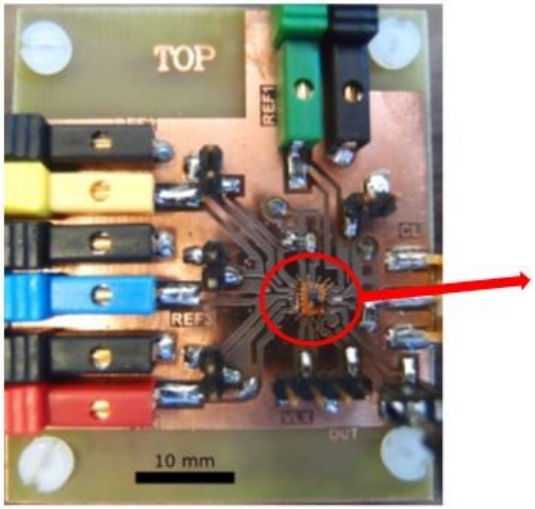


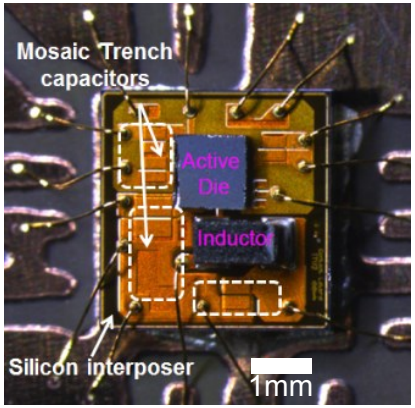
HF embedded converter

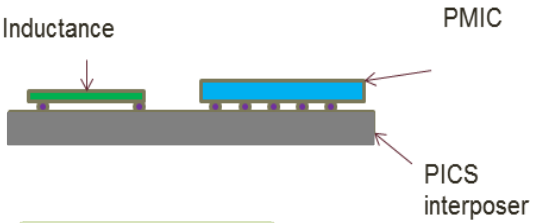
- Embedded buck converter
  - P~0.5W / 1 Φ
  - Frq=100Mhz
  - Variable VOut=1.2-2.4V, Ripple <2%
- Interposer setup
  - Cout=30nF / ESR<30mOhm
  - Cin=15nF / ESR<50mOhm
  - ESL <10pH
  - Minimized Stray inductance on GND/VIn/VLoad loops <20pH



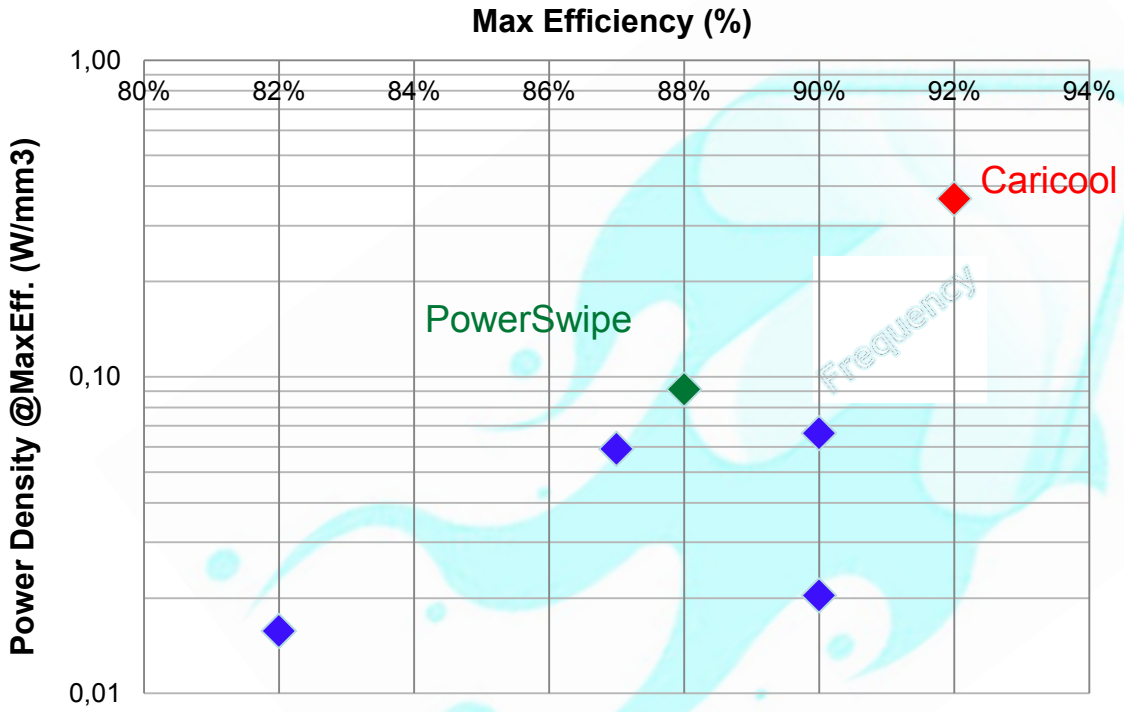
A 100 MHz, 91:5% Peak Efficiency Integrated Buck Converter With a three-MOSFETs Cascode Bridge
Florian Neveu & Al., IEEE TRANSACTION ON POWER ELECTRONICS





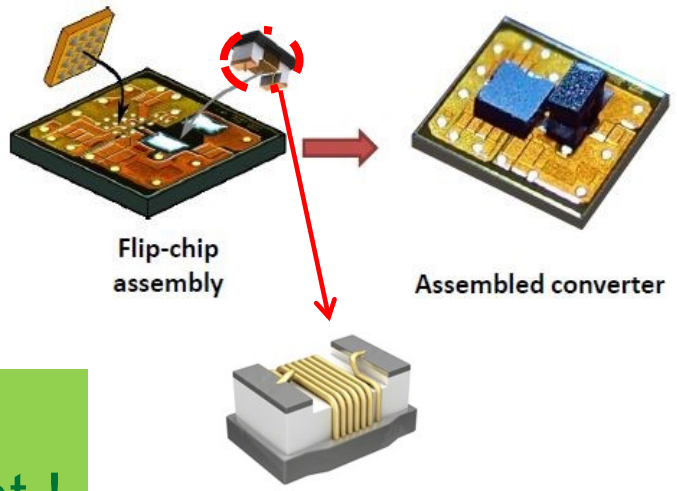


Beyond SOA



Integrated passives

- ✓ Small form factor
- ✓ Less parasitic
- ✓ Enhanced thermal



Need to go beyond SMD solutions for integration !

New filtering component integrating a distributed LC filter ISO localized element !

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A Novel Approach For LC Output Filter

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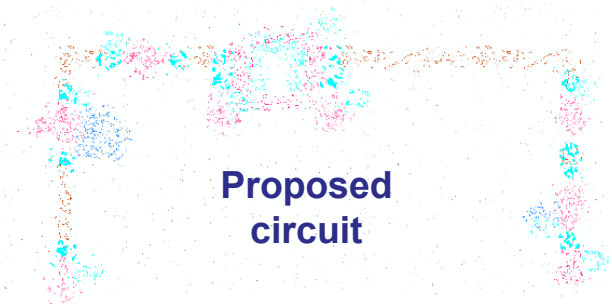
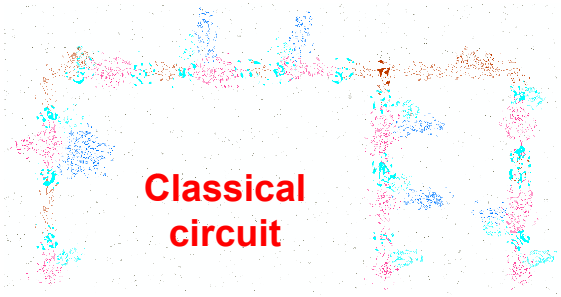
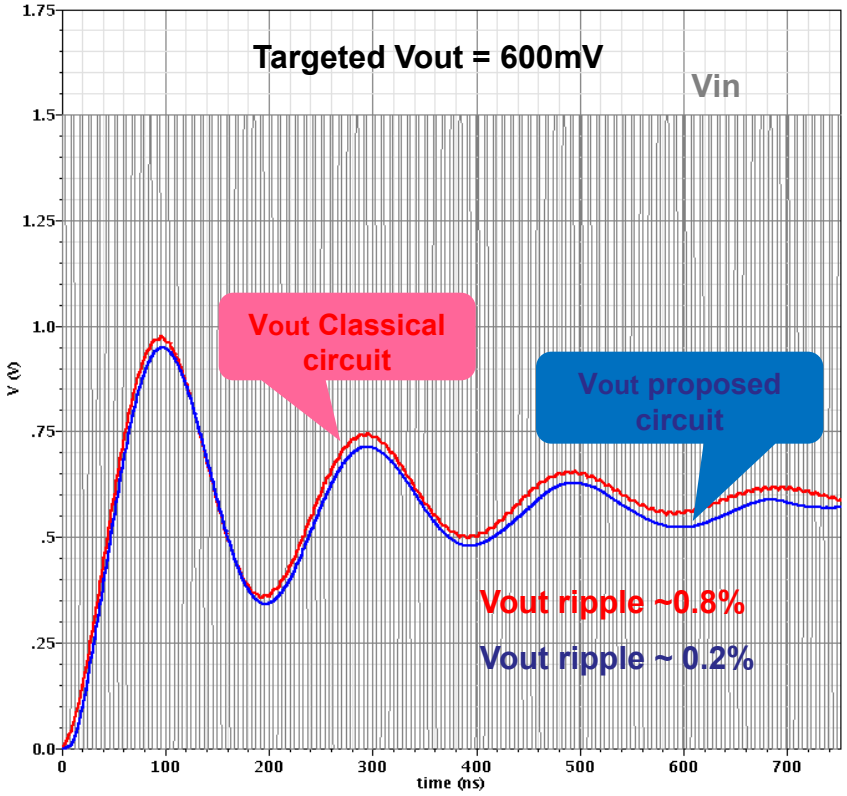
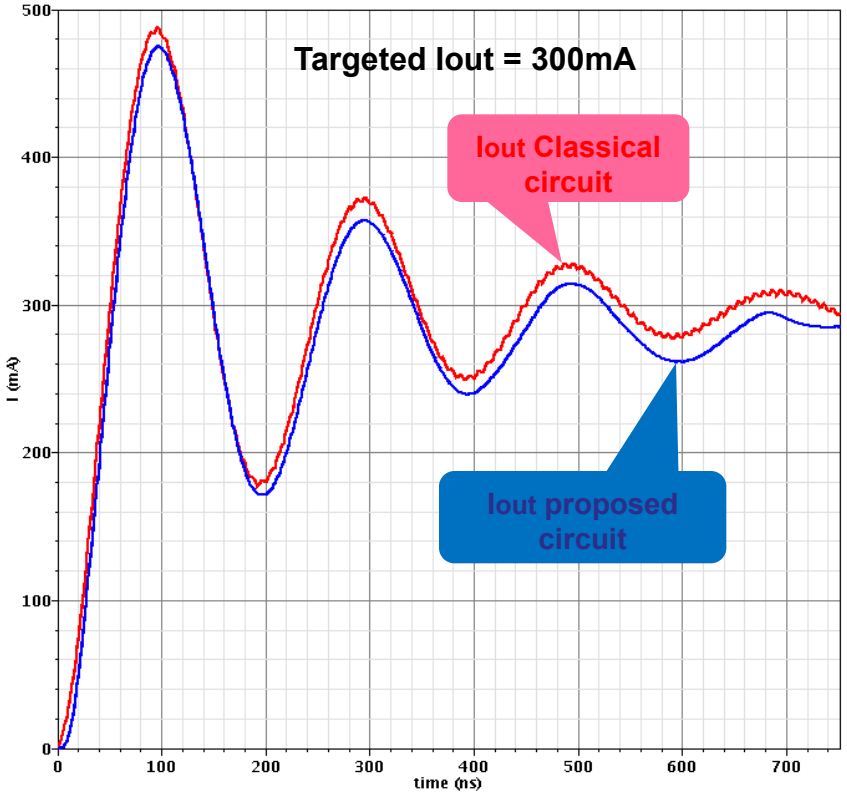
Transient Simulations





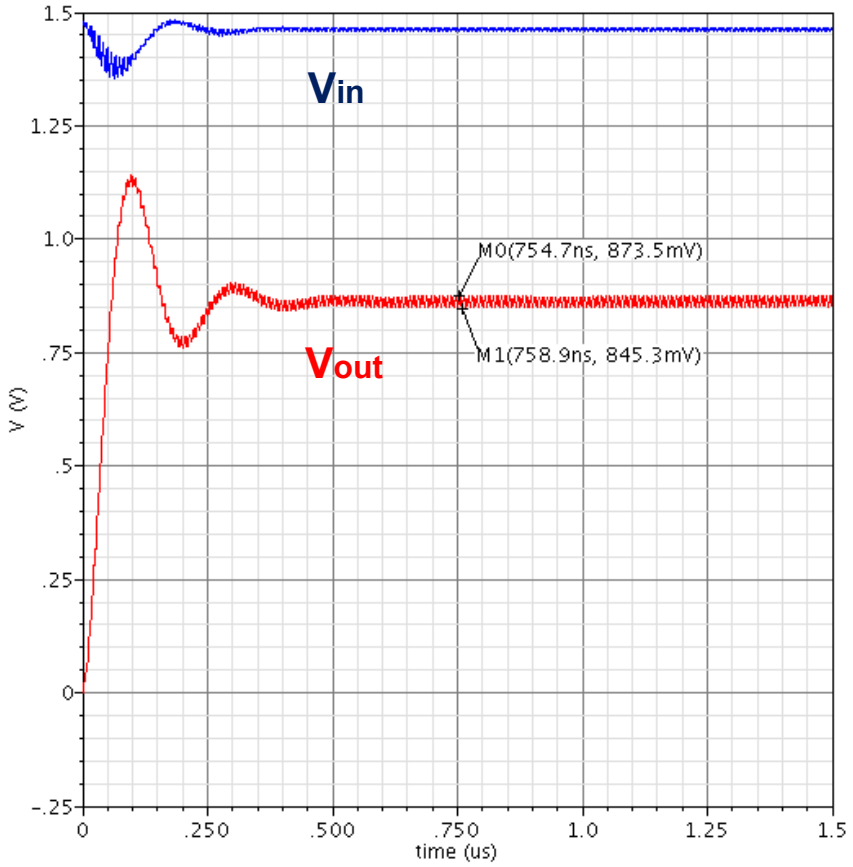


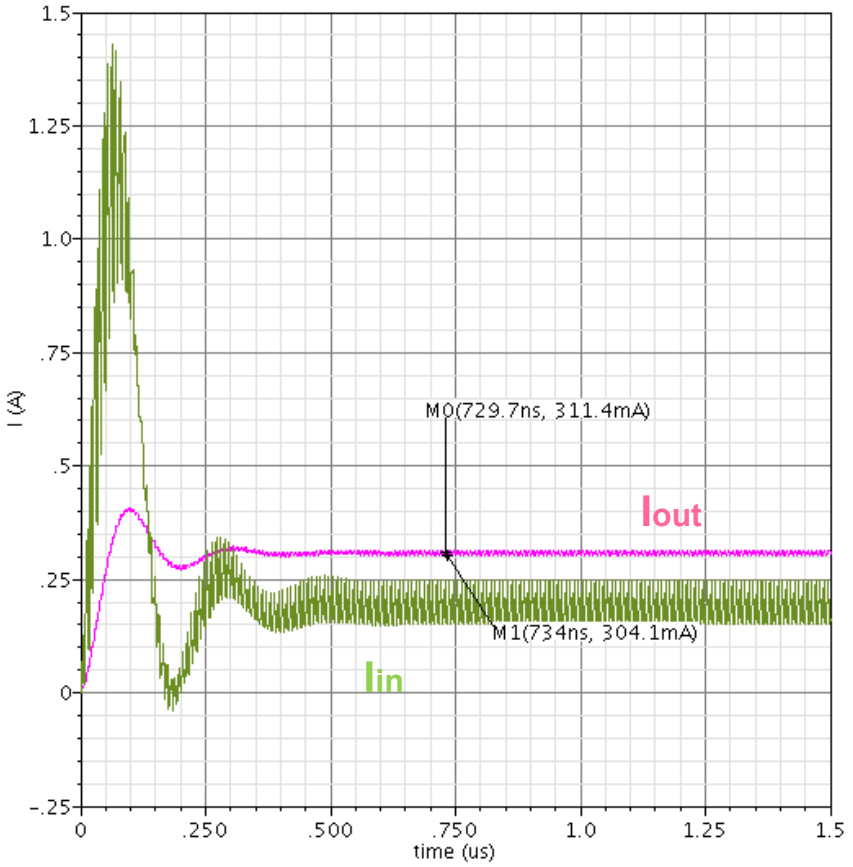


Application to Carricool project

- **Static**
  - Vin=3.3V / Vout=0.6 - 1.2V, 1V nominal
  - Iout=300mA
  - VOutRipple <1%
  - Efficiency >92% @ 1V/0.3A
  - PowerDensity
    - *Solution surface <5mm²*
    - *>0.3W/mm3 at max efficiency*
- **Dynamic**
  - VOutSwing =10mV (50% load step / 0.1ns)
- **Boundary conditions**
  - Frequency <200MHz
  - L ~ 13nH / esr>100mOhm
  - C unconstrained

Transient Response





Outlook

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Take aways

- Can implement LC circuit with **PICS core** for DC-DC converter 1 pole filtering
  - → this gives more **compact size** compared to equivalent discrete
  - → This gives higher attenuation at high frequency = **better rejection** of HF mode
- Carricool: PMIC was capable to achieve high conversion efficiency (typ. >95%) at frequency 115 MHz for output power of typ. 0.3W.
- IPDiA demonstrated that a new concept with passives could have loss limited to **~5%**, yielding a converter overall efficiency ~90%
- Compared to SOA, the proposed passive concept has the advantages of:
  - A **very low profile** (that can be reduced down to 60µm)
  - An ultimate density of integration (output filter L, C and PMIC could be overlaid in the vertical axis)
  - A simplified process stack that would largely lower processing complexity (wafer front-side processing only) and costs.
- New LC filter → Signals are on top (BTW) GND plane → no field leakage
- A physical implementation of this filter is currently processed on silicon and experimental results will be presented as a follow-up of this presentation

Acknowledgments

The authors would like to thank :

- Carricool project partners

http://www.carricool.eu/

CarrICool

(FP7/2007-2013)

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- *IPDiA team @ PwrSOC 2016 → We have solutions for you*

Thank you for your attention

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