THAYER SCHOOL OF ENGINEERING AT DARTMOUTH

Resonant & Multimode SC Converters:

Power Management in the mm^3 Regime

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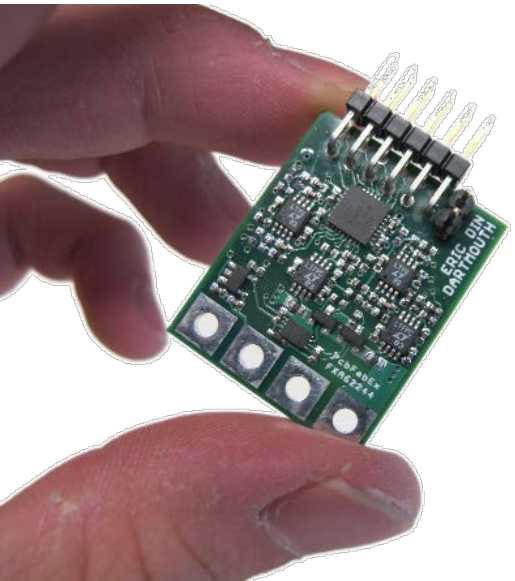
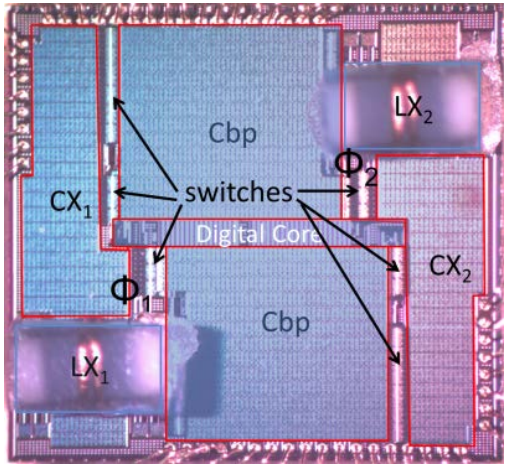
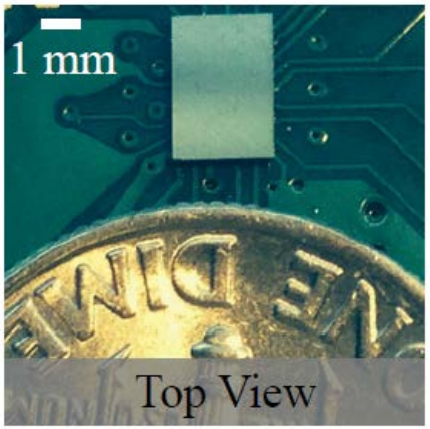






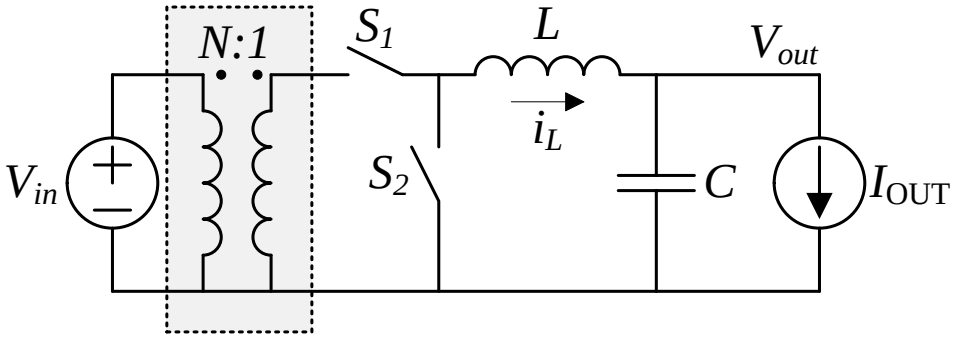
IEEE PowerSOC, October 5, 2016

Outline

- High-density DC-DC conversion
- Hybrid/Resonant Topology Overview
- Generalized output impedance modelling for N:1 resonant topologies
- Multimode operation
- SC/ReSC power loss minimization & comparison
- Example: 12V → 3.7V Quasiresonant Series-Parallel Converter
- Conclusion

High Density DC-DC Converter:

Key → Reduce passive component volume



$$\Delta i_{pp} \propto \frac{V_{in}}{f_{sw} L} \rightarrow \left[\frac{V \cdot s}{H}\right]$$

$$\Delta v_{out,pp} \propto \frac{\Delta i_{pp}}{f_{sw} C_{out}} \rightarrow \left[\frac{A \cdot s}{F}\right]$$

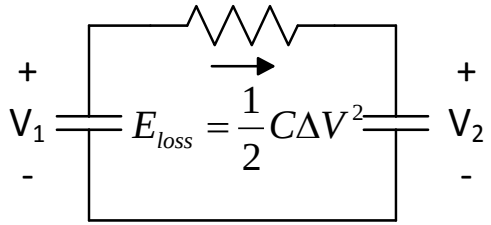
Strategy 1: Increase frequency

- Smaller inductor, capacitor
- Increase in frequency dependent losses (winding, core, gate drive etc.)

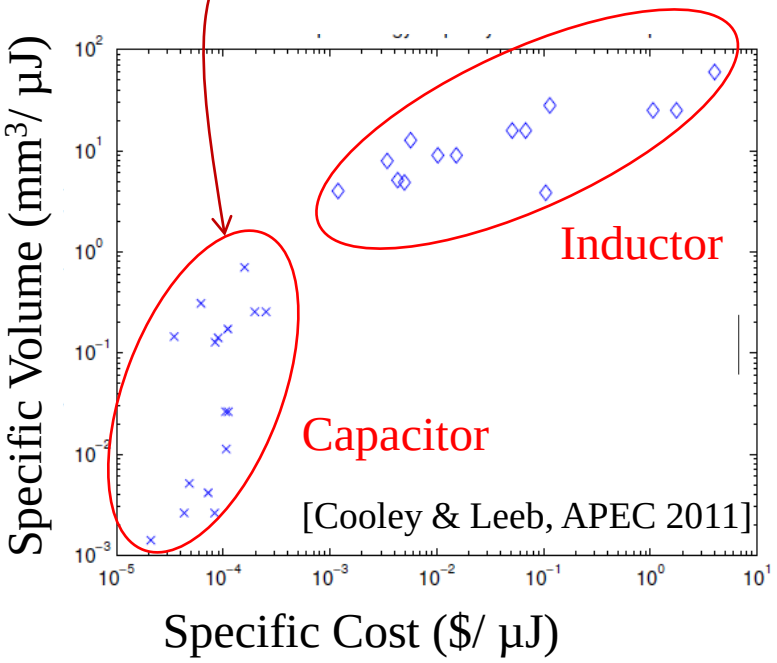
- Strategy 2: Change Architecture
  - Reduce inductor ΔV
  - Multi-level or multi-stage converter
  - Possible double efficiency penalty

- Do Both?

Switched Capacitor Perspective



Accessing this energy density costs power

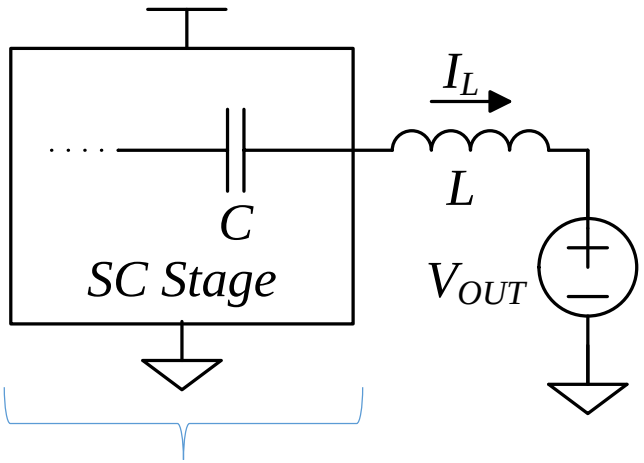


- Only switches and capacitors
  - Simple full integration in standard CMOS
- Capacitors have much higher energy density than inductors
- Stacked devices enable high voltage with low voltage process
- Achieve higher device utilization FOM[1]
- Inherent charge sharing loss
- Difficult Regulation
  - Reconfigurable Architectures
  - Lossy linear regulation

[1][Seeman & Sanders, TPEL 2008]

Hybrid/Resonant SC Converters

(Concept can be generalized to many topologies)



e.g. FCML [1, 3], Series Parallel [2], Fibonacci, Dickson [3]

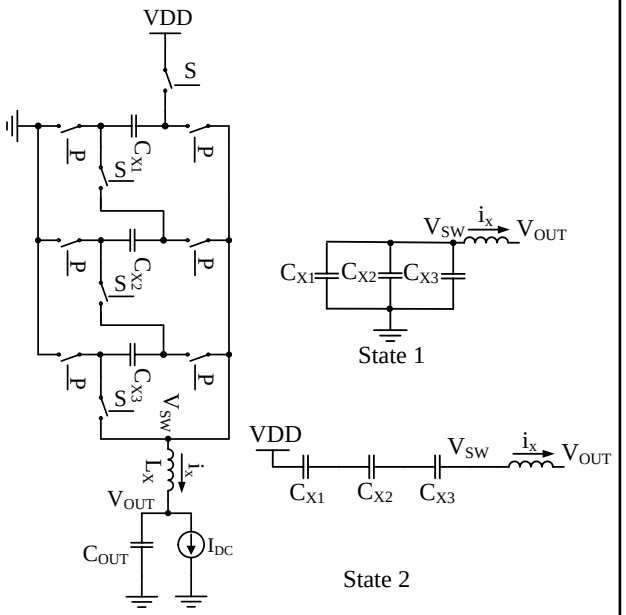
- Leverage high active device utilization (same as SC)
- Soft charging or resonant energy transfer (reduce charge sharing loss)
- Potential for higher utilization of capacitor energy density (larger voltage swing allowed)
- SC front end → lower V-s product → shrink inductor dramatically
- Capability for Variable Regulation
- Multi-mode operation: high efficiency across load range

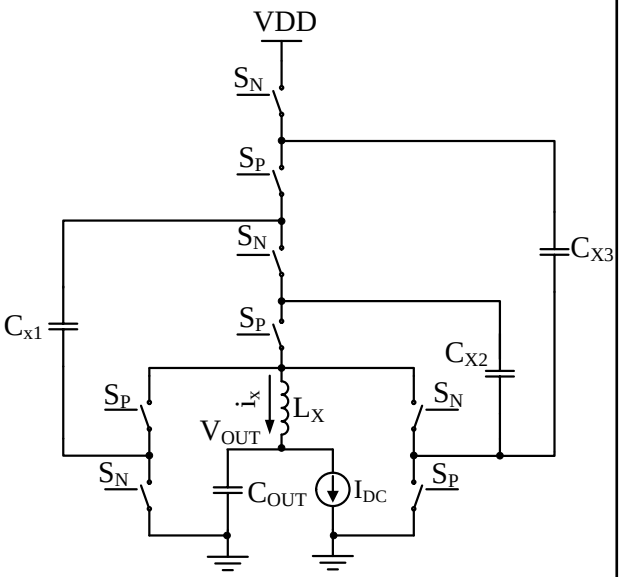
[Kesarwani Compel ’15]
[Rentmeister ECCE ‘16]

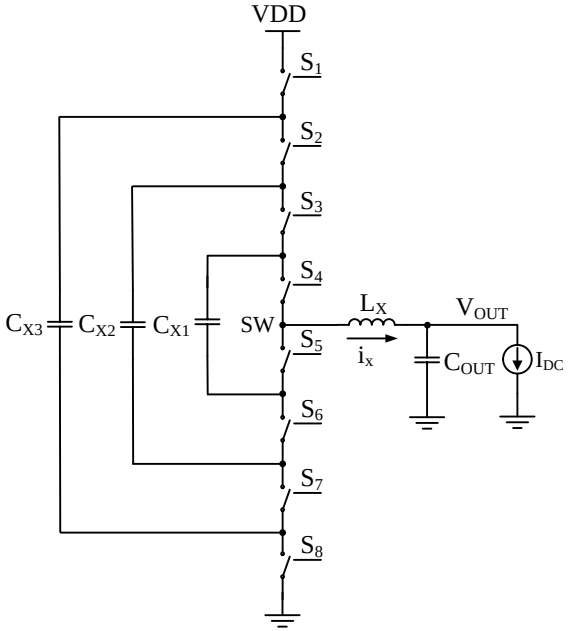
[1] Meynard PESC ‘92
[2] Schaef APEC ‘17
[3] Lei et al & Pilawa APEC ’16 & TPEL ‘15

Examples

Series-Parallel ReSC	Dickson ReSC	FCML/Meynard







Considerations:

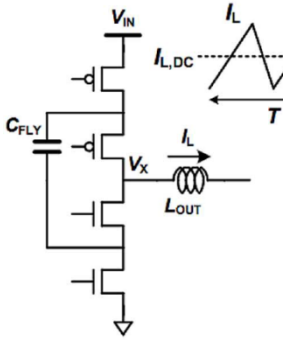
- Internal Charge Sharing [Lei et al, COMPEL 2013]
- Voltage Balance on Capacitors = universal challenge [Kesarwani, COMPEL '15]
- Startup, gate driving
- Variable control & timing
- Parasitics, ringing, etc.

Implementation is challenging, but performance is compelling

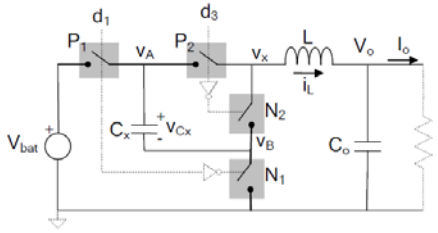
Examples: Past Work

Many other examples, esp FCML, 3-level:
Reusch & Lee; Salem & Mercier; Shenoy et al;

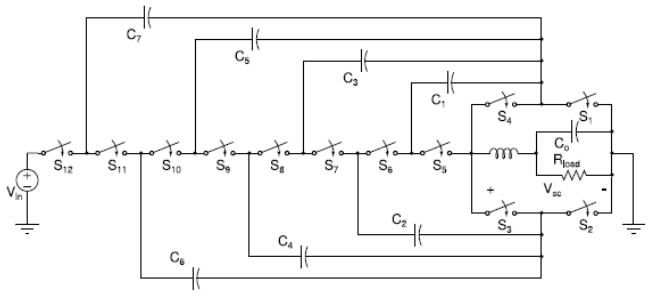
Kim, Brooks, Wei
(JSSC 2012)



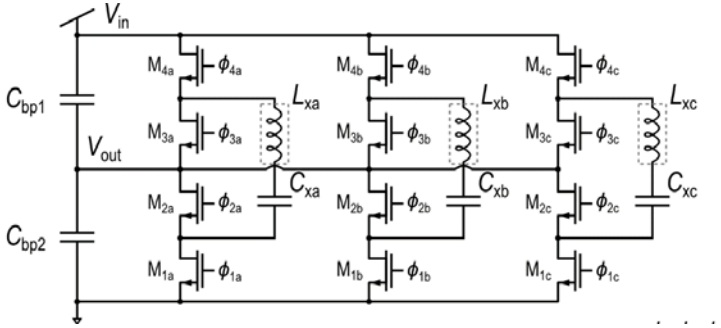
Pique, Alarcon
(PESC 2008)



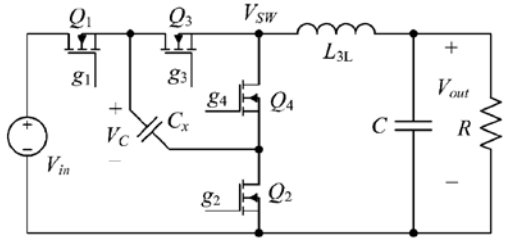
Lei, May, Pilawa
(TPEL 2016)



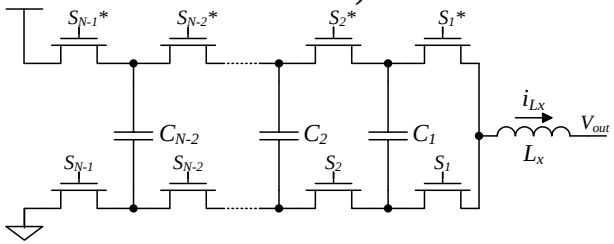
Schaef, Stauth,
(ISSCC 2015)



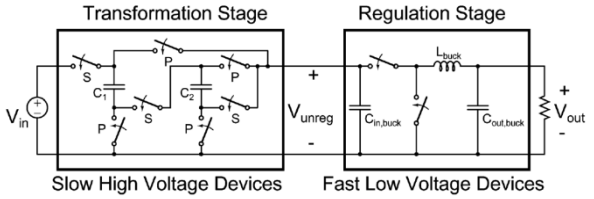
Yousefzadeh, Alarcon,
Maksimovic (TPEL 2006)



FCML: Meynard ’92
(& others, e.g. Pilawa Little Box
APEC ‘16)

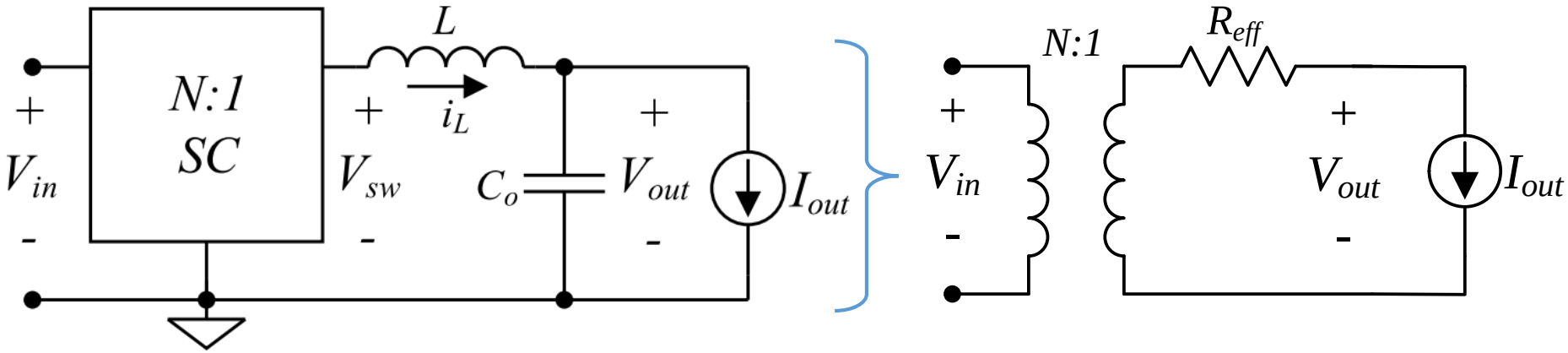


Pilawa, Perreault (JSSC 2012)



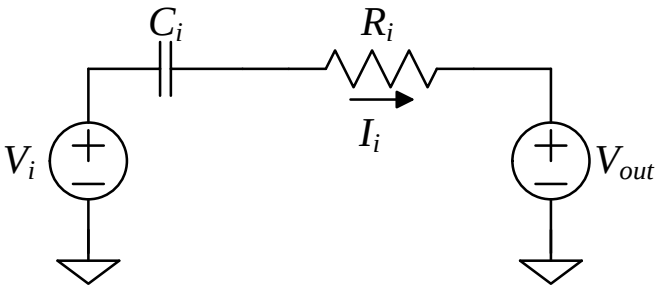
Generalized Output Impedance Modelling

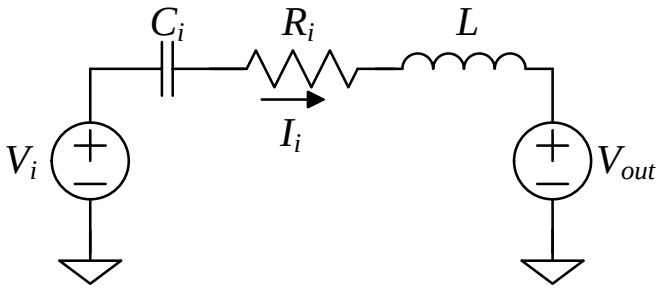
- Focus: Hybrid SC topologies that can be *resonated with a single inductor* (FCML, Series Parallel, Fibonacci)



- General formulation: Step-Down Topologies
- SC = unregulated, arbitrary N:1 step down stage
- Inductive impedance shapes the current waveform
- R_{eff} model: captures conduction loss & loadline

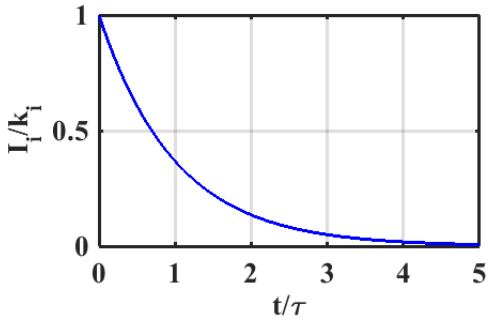
In Any Given Phase…



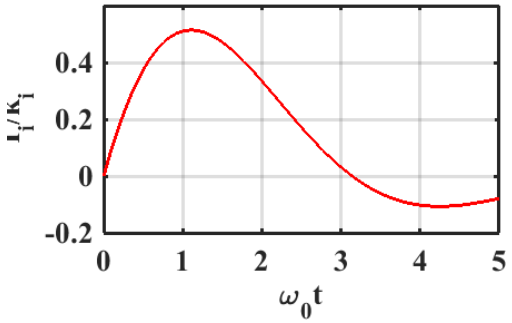


$$I_i(t) = k_i e^{\frac{-t}{R_i C_i}}$$

$$I_i(t) = k_i e^{\frac{-tR_i}{2L}} \sin(\omega_{0i} t)$$



$k_i = F(\text{initial conditions})$



Charge Transferred:

Energy Dissipated:

Key:

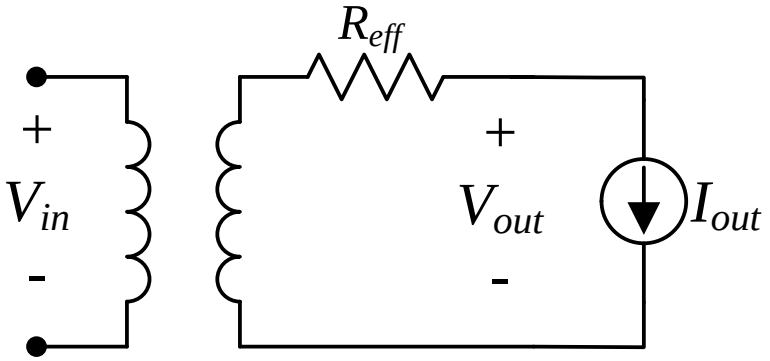
$$q_i = \int_0^{t_i} I_i \, dt$$

e.g. 2:1 →

$$t_i = \frac{T_{sw}}{2} = \frac{1}{2f_{sw}}$$

$$E_i = \int_0^{t_i} R_i I_i^2 \, dt$$

R_{eff} Model



$$P_{loss} = f_{sw} \sum E_i = I_{DC}^2 R_{eff} = \left(f_{sw} \sum q_i \right)^2 R_{eff}$$

$$R_{eff} = \frac{f_{sw} \sum E_i}{(f_{sw} \sum q_i)^2}$$

$$q_i = a_i \, q_{ref}$$

$e.g.: \; q_{ref} = \sum q_i$

Know proportionally how much charge flows out in each phase from topology

*optimized/normalized cap sizing/utilization

*normalized T_{sw}/τ per phase

Same as a_{out} element in:

[Seeman & Sanders, TPEL '08]

Cancels out in final calculation, sort of arbitrary

Results

Note: Result is general
- Works for arbitrary N-level SC/ReSC topologies where charge flow links the output: SP, FCML, Fibonacci
- Specific cases (Series parallel, FCML) worked out in: [Pasternak, Compel '16]

Arbitrary SC Circuit

$$R_{eff} = \frac{\sum \frac{a_i^2}{C_i} \coth\left(\frac{t_i}{2R_iC_i}\right)}{2f_{sw}(\sum a_i)^2}$$

$t_i \gg 2R_iC_i$

$$R_{SSL} = \frac{\sum \frac{a_i^2}{C_i}}{2f_{sw}(\sum a_i)^2}$$

$t_i \ll 2R_iC_i$

$$R_{FSL} = \frac{\sum \frac{a_i^2 R_i}{t_i}}{f_{sw}(\sum a_i)^2}$$

e.g. 2:1 → $a_i = 1$, $C_i = C$, $R_i = R$

$$R_{SSL} = \frac{1}{4f_{sw}C}$$

$$R_{FSL} = R$$

Arbitrary ReSC Circuit

$$R_{eff,ReSC} = \frac{\sum \frac{a_i^2}{C_i} \tanh\left(\frac{R_i}{8Lf_{0i}}\right)}{2f_{sw}(\sum a_i)^2}$$

@ high Q

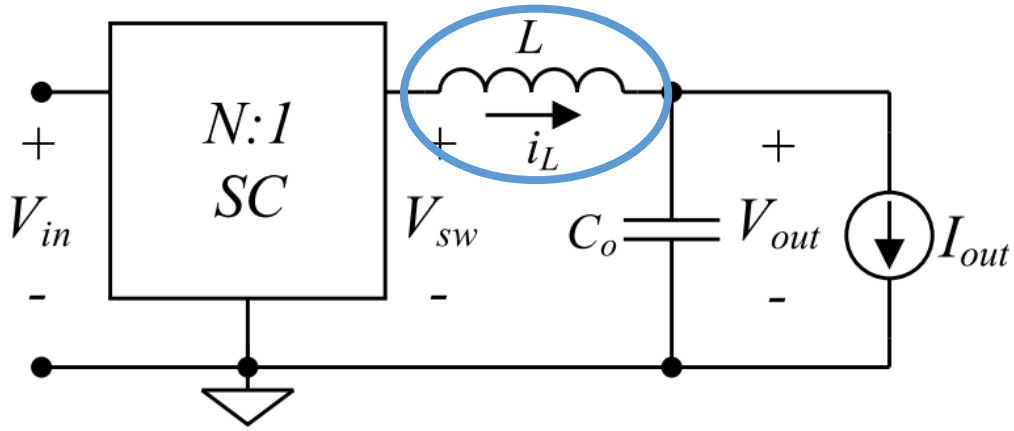
$$R_{eff,ReSC} \approx \frac{\sum \frac{\pi a_i^2}{4C_iQ_i}}{2f_{sw}(\sum a_i)^2}$$

e.g. 2:1 → $a_i = 1$, $C_i = C$, $R_i = R$, $Q_i = (\omega_o RC)^{-1}$

$$R_{eff,ReSC} \approx \frac{\pi^2}{8}R$$

Comparison

(any arbitrary converter or phase)



SC FSL/SSL boundary at $t_i = 2R_iC_i$ For ReSC $t_i \approx \pi\sqrt{LC_i}$

@ inflection, resonant period is increased (frequency is reduced) by $\sim \frac{\pi}{2} Q_i$

$$R_{SSL} = \frac{\sum \frac{a_i^2}{C_i}}{2f_{sw}(\sum a_i)^2} \qquad R_{ReSC} = \frac{\sum \frac{\pi a_i^2}{4C_iQ_i}}{2f_{sw}(\sum a_i)^2}$$

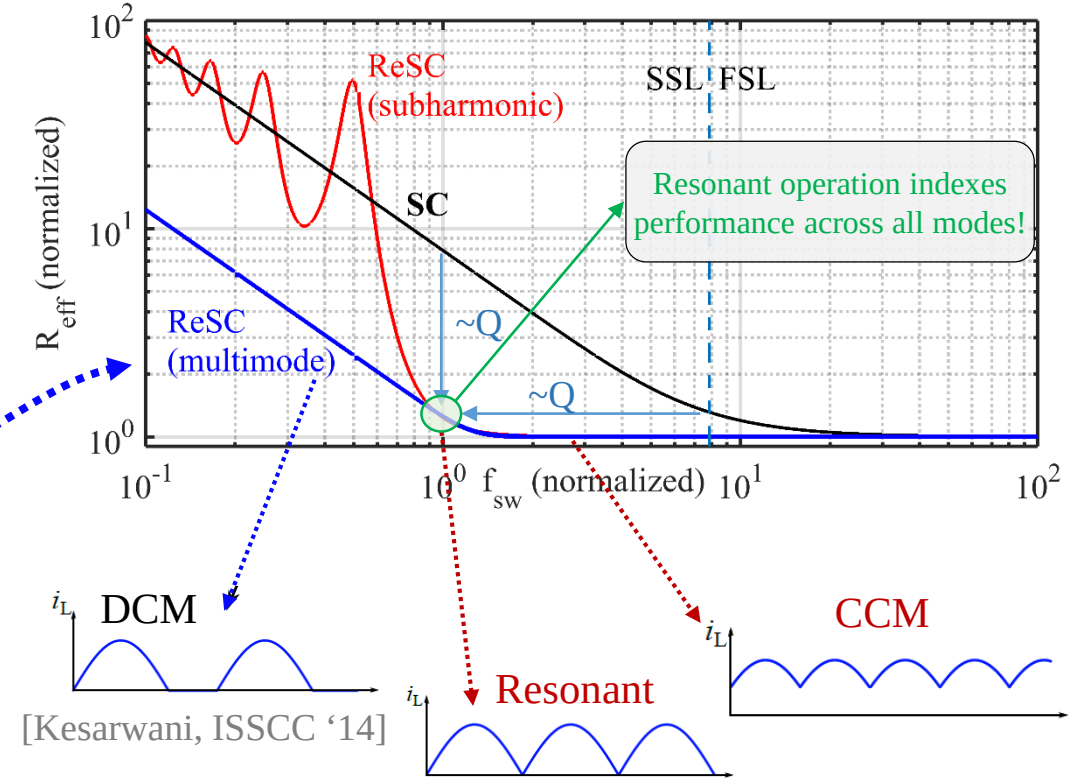
In SSL @ same frequency, R_{eff} of resonant case is improved by a factor of $\sim \frac{\pi}{4} Q_i$

R_{eff} vs Frequency: Any Arbitrary Phase

- Fundamental resonant operation = primary case treated thus far
- @ high frequency → CCM
- @ low frequency → off-time modulation (DCM)
- Behavioral model can be used to capture entire frequency range:

$$R_{EFF} \approx \sqrt[\alpha]{1+\left(\frac{\pi^2}{8}\frac{f_0}{f_{SW}}\right)^{\alpha}}\,R_{ESR}$$

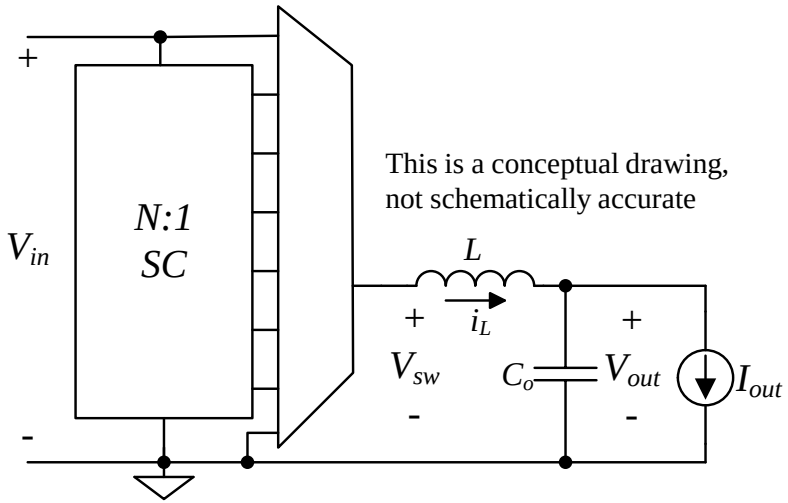
- α=9.2 (least squares analysis)
- Less than 2% error over entire range



Exact Expression –> 2:1 Converter: [Pasternak, Compel '16]

$$R_{eff} = \frac{1}{4Cf_{sw}}\left(\frac{\sinh\left(\frac{R}{4Lf_{sw}}\right)+\frac{R}{4\pi Lf_0}\sin\left(\frac{\pi f_0}{f_{sw}}\right)}{\cosh\left(\frac{R}{4Lf_{sw}}\right)-\cos\left(\frac{\pi f_0}{f_{sw}}\right)}\right)$$

Extended Multimode Operation

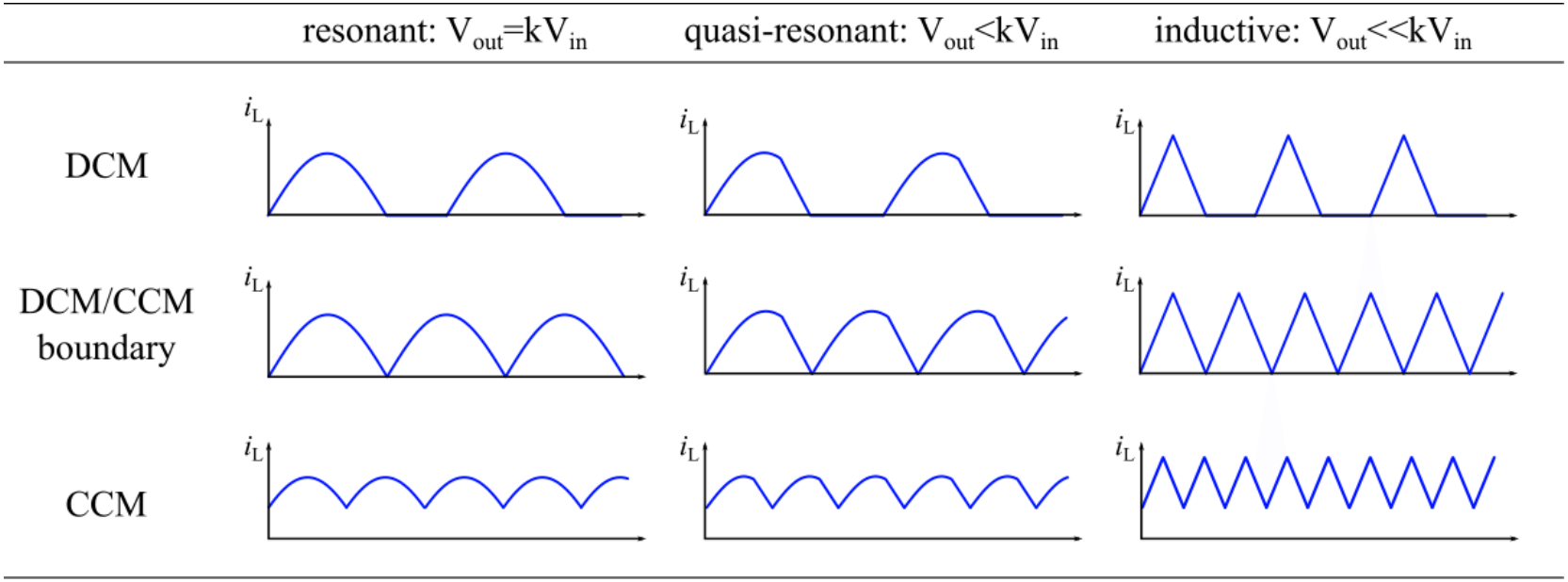


Variable regulation

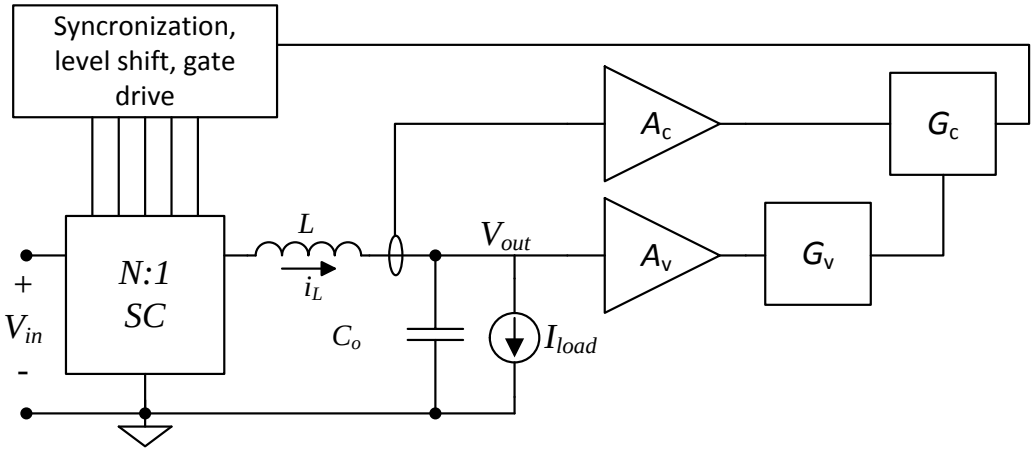
- Interpolate between levels:

$$\frac{k-1}{N-1} < \frac{V_{out}}{V_{in}} < \frac{k}{N-1} \qquad \text{for: } 1 < k < N-1$$

- Depending on volt-seconds applied (frequency and V_{sw}-V_{out})
  Inductor current waveform will appear:

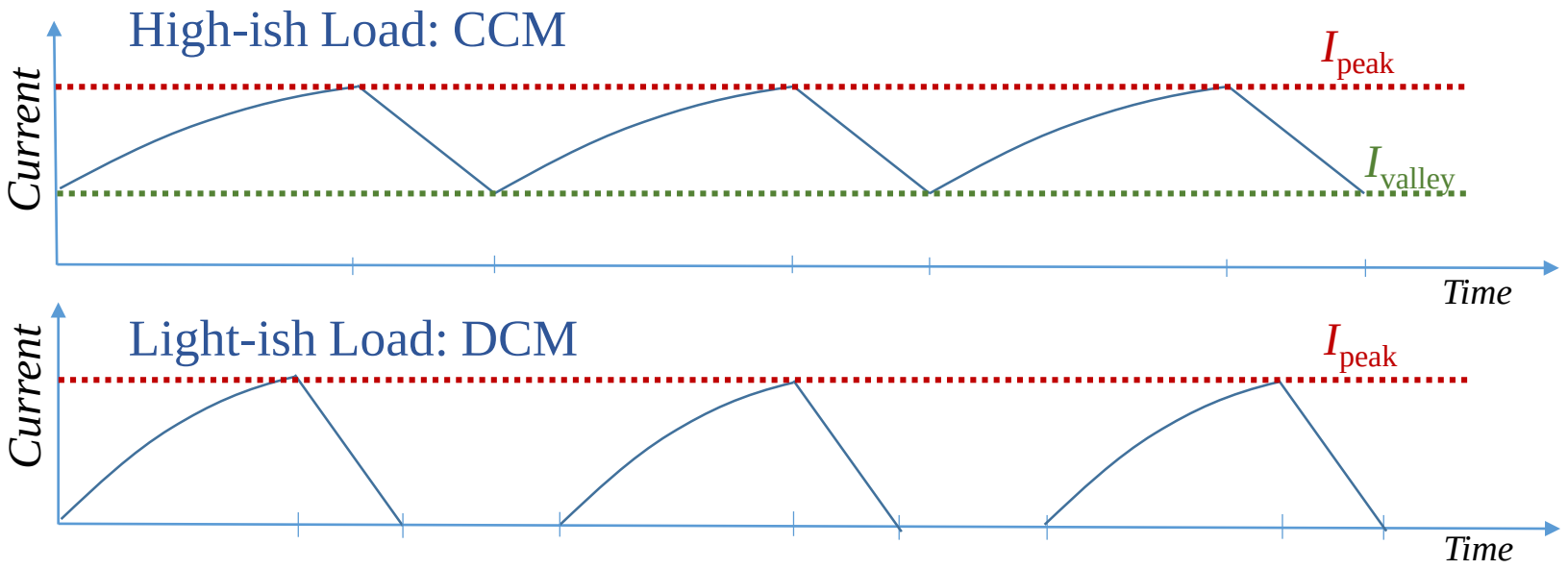


Nice way to accomplish multi-mode operation: Current Mode Control

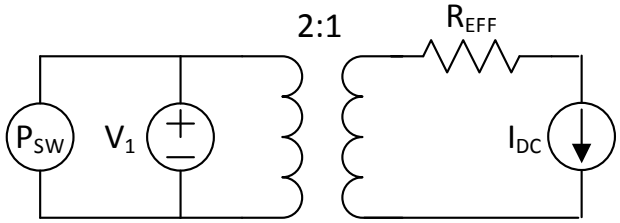


Nice bonus: This scheme can 'automatically' balance flying capacitor voltages!

[Rentmeister ECCE '16]



SC Optimization



Related to R_{switch}, ↓ with ↑ size

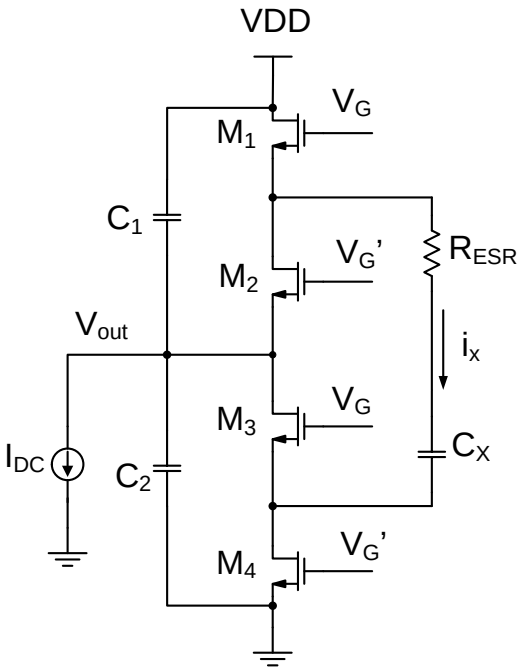
Related to C_{switch}, ↑ with ↑ size

$$P_{LOSS} = P_{COND} + P_{SW} = I_{DC}^2 R_{EFF} + E_{GG} f_{SW}$$

$$R_{EFF} = \frac{1}{4Cf_{SW}} \coth\left(\frac{1}{4 f_{SW} RC}\right)$$

$$E_{GG} = 4E_{GG,sp} W_{sw}$$

$$R = \frac{2R_{on,sp}}{W_{sw}}$$



$$\frac{\partial P_{LOSS}}{\partial W_{sw}} = 0$$

$$\Downarrow$$

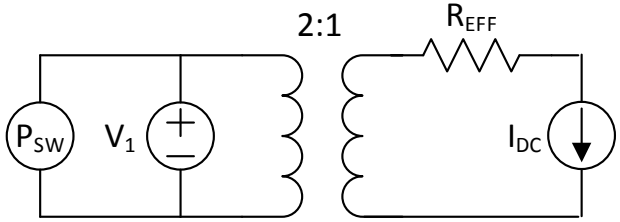
This is true regardless of static loss, fixed resistance, bottom plate capacitance

$$W_{opt} = 8C_X R_{ON,SP} f_{SW} \tanh^{-1}\left(\frac{I_{DC}}{\sqrt{I_{DC}^2 + 128E_{GG,SP} f_{SW}^3 C_X^2 R_{ON,SP}}}\right)$$

[Kesarwani, TPEL '14]

SC Optimization

$$W_{opt} = F(f_{sw})$$



$$P_{LOSS} = P_{COND} + P_{SW} = I_{DC}^2 R_{EFF} + E_{GG} f_{SW}$$

$$\frac{\partial P_{LOSS}}{\partial f_{sw}} = 0 \Rightarrow \text{trancendental equation?}$$

$$f_{SW,OPT} = \sqrt[3]{\frac{k I_{DC}^2}{128 C_X^2 E_{GG,SP} R_{ON,SP}}}$$

$$\frac{\sqrt{1+k}}{2k} = \sinh^{-1}\left(\frac{1}{\sqrt{k}}\right) \qquad k = 0.577$$

$$f_{SW,OPT} = 0.1652 \sqrt[3]{\frac{I_{DC}^2}{C_X^2 E_{GG,SP} R_{ON,SP}}}$$

$$W_{opt} = 1.4386 \cdot \sqrt[3]{\frac{C_X I_{DC}^2 R_{onsp}^2}{E_{GG,SP}}}$$

Device FOM

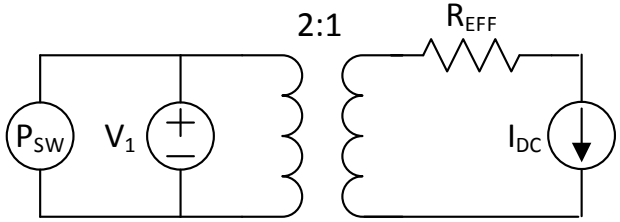
Note: does not include bottom plate loss… lets discuss later!

$$P_{LOSS} = 2.850966 \cdot I_{DC}^{4/3} \cdot \sqrt[3]{\frac{E_{GG,SP} R_{ON,SP}}{C_X}}$$

[Pasternak, Compel '16]

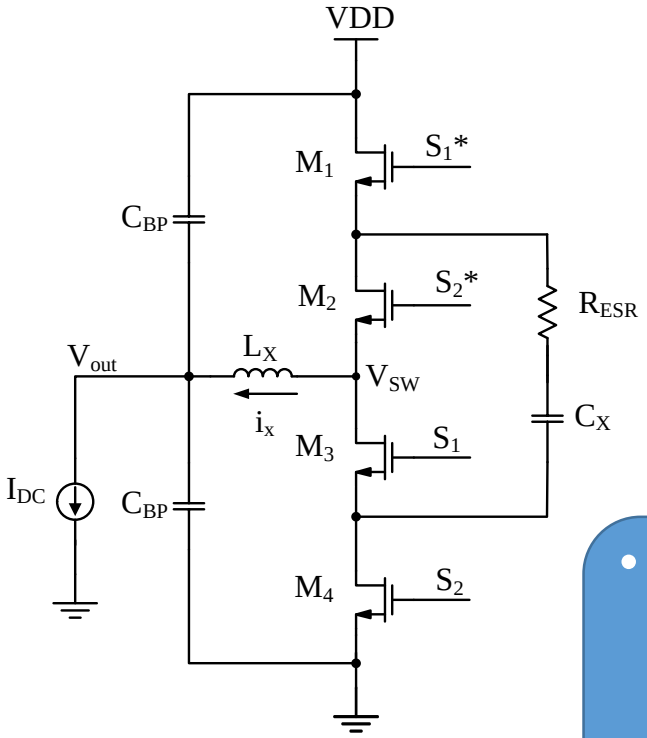
ReSC Optimization

Btw: similar optimizations for N:1 topologies in Pasternak '16



$$R_{EFF} = \frac{\pi^2}{8}\frac{2R_{on,sp}}{W_{sw}} \qquad E_{GG} = 4E_{GG,sp}W_{sw}$$

$$P_{LOSS} = P_{COND} + P_{SW} = I_{DC}^2 R_{EFF} + E_{GG} f_{SW}$$



$$\frac{\partial P_{LOSS}}{\partial W_{sw}} = 0 \Rightarrow W_{opt} = \frac{\pi}{4} I_{DC} \frac{1}{\sqrt{f_{SW}}} \sqrt{\frac{R_{on,sp}}{E_{GG,sp}}}$$

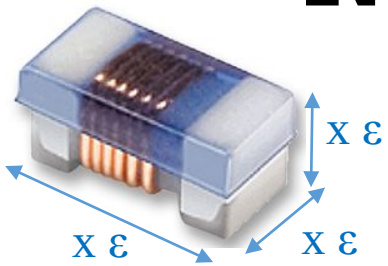
$$P_{MIN} = 2\pi I_{DC} \sqrt{f_{SW}} \sqrt{R_{on,sp} E_{GG,sp}}$$

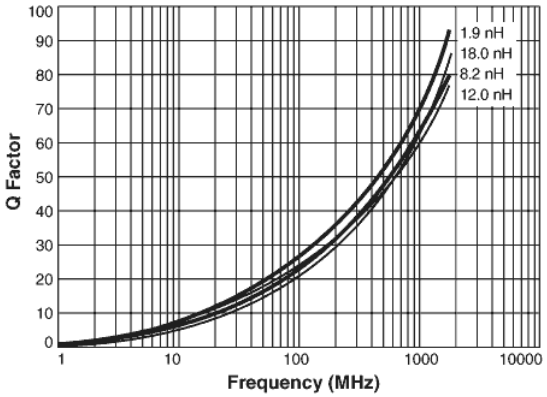
Device FOM

$$f_{SW,opt} = 0?$$

- Says that ReSC (and other hybrids) get better with arbitrarily low frequency, independent of other factors…
- What is happening → solution is choosing arbitrarily large, lossless inductor!

Realistic Inductor Model





$L_0 = \text{base L @ } V_0$

$R_{DC,0} = \text{base R @ low freq, } V_0$

$R_{AC,0} = \text{base R @ } f_0, V_0$

$Q_0 = \text{base Q @ } f_0, V_0$

Neglects R_{DC}
→ other models possible

$$R_{AC,0} = \frac{2\pi f_0 L_0}{Q_0} = k_0\sqrt{f_0}$$

Constant Volume Scaling of Inductance

$$L \propto N^2$$

$$R_{DC} \propto N^2 = R_{DC,0}\frac{L_{act}}{L_0}$$

$$R_{AC} \propto N^2 = R_{AC,0}\frac{L_{act}}{L_0}$$

Dimensional Scaling:

$$L_0^* = \varepsilon L_0 \longrightarrow \text{Same turns ratio} \quad L \propto N^2\varepsilon$$

$$R_{DC,0}^* = \frac{R_{DC,0}}{\varepsilon} \longrightarrow \frac{\rho l}{A} \propto \frac{1}{\varepsilon}$$

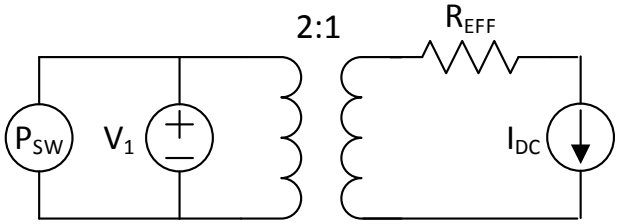
$$Q_0^* = \varepsilon Q_0 \longrightarrow \text{Invariant } R_{AC} \text{ (const } f_0\text{), larger L}$$

$$R_{AC}^* = k_0\sqrt{f_{act}}$$

[Perreault et al and Sullivan APEC '09]

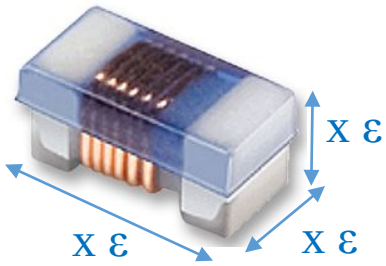
[Largely unpublished]

SC and ReSC Optimization

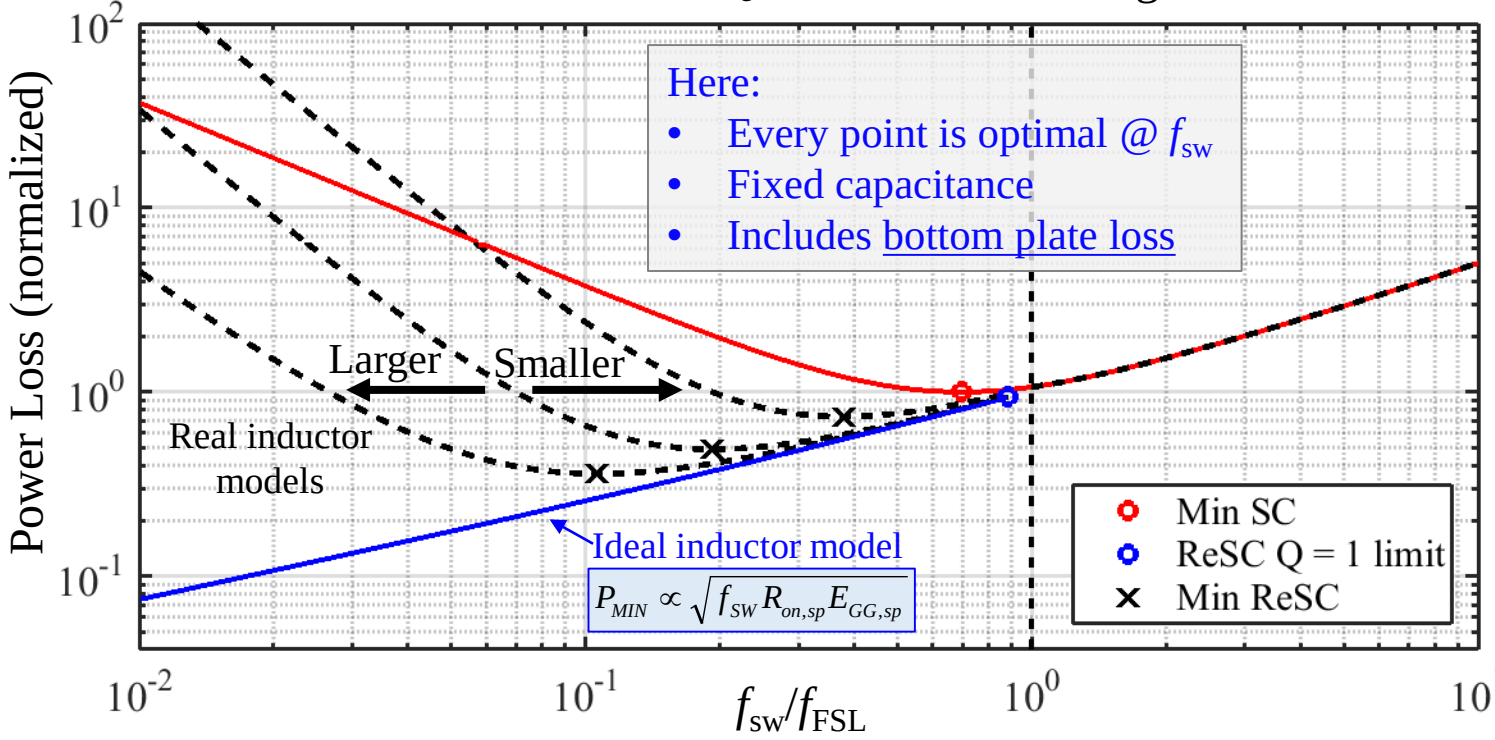


Total Power Loss

$$P_{LOSS} = P_{COND} + P_{SW}$$

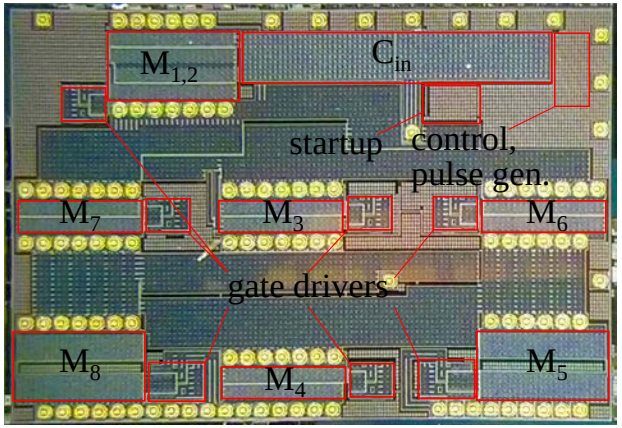


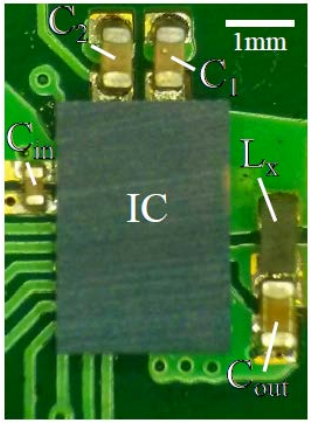
ReSC is practical with mm-scale air-core inductors!
Must achieve sufficient 'Q' to have an advantage

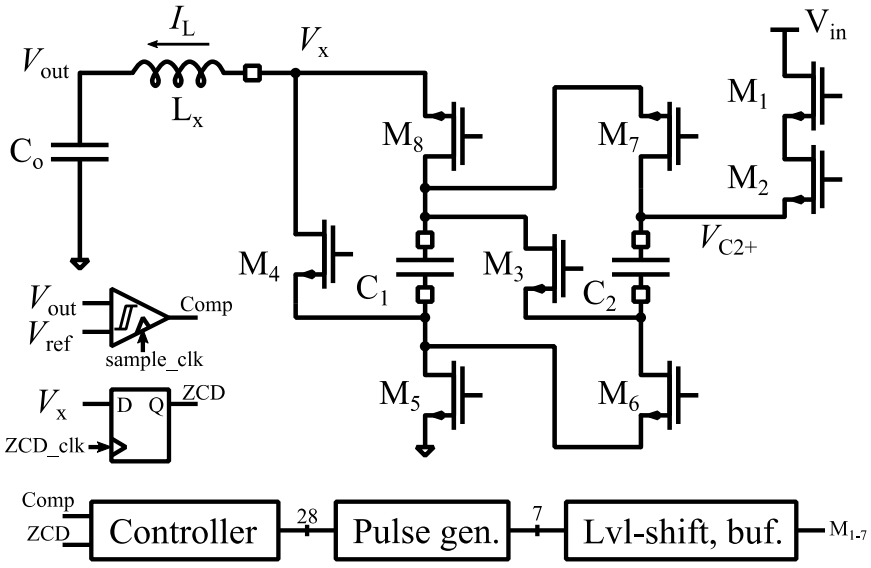


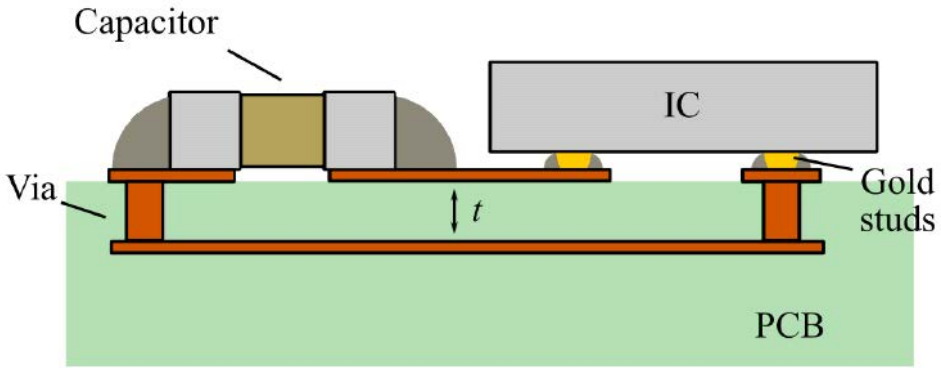
[Scaling Laws: Perreault et al and Sullivan, APEC '09]

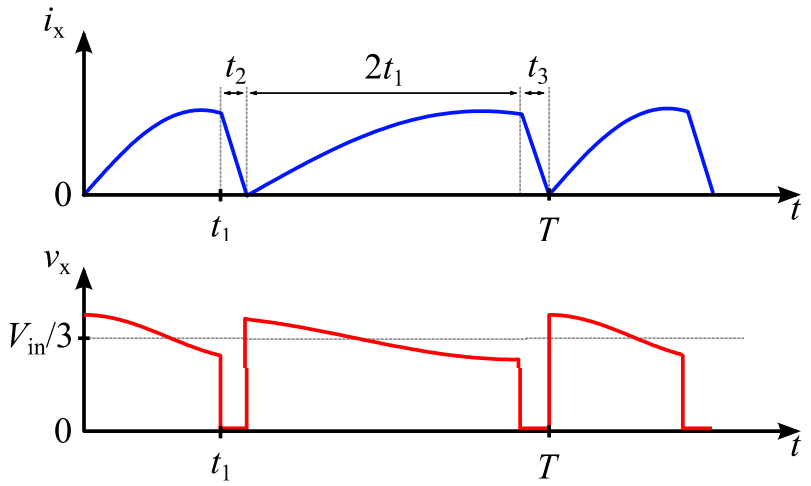
Example: 12V → 3.7V (LiIon) Quasiresonant Series Parallel





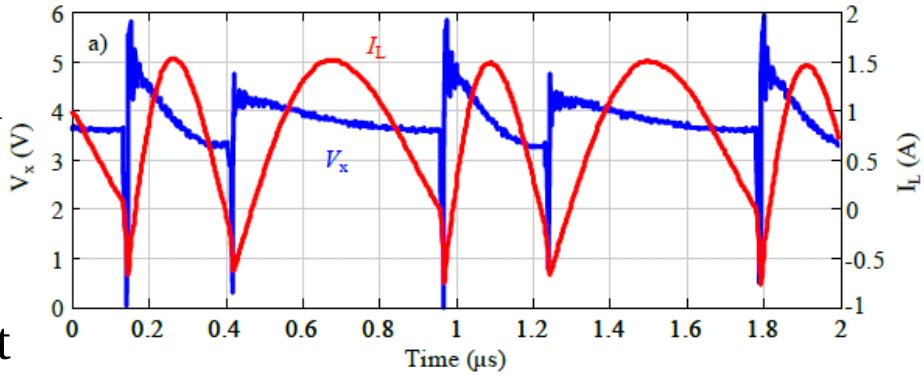






Details

- Regulation: 1-bit voltage-mode integral control with nested zero current detection
- Inductor = 33 nH (0402)
- Flying Cap = 2 x 330 nF (0402)
- Bypass Cap = (0201) input, (0402) output
- Peak efficiency = 87% @ 4.6 W
- Power density = 0.3 W/mm^3 ≈ 5.0 kW/in^3 (bounding box)



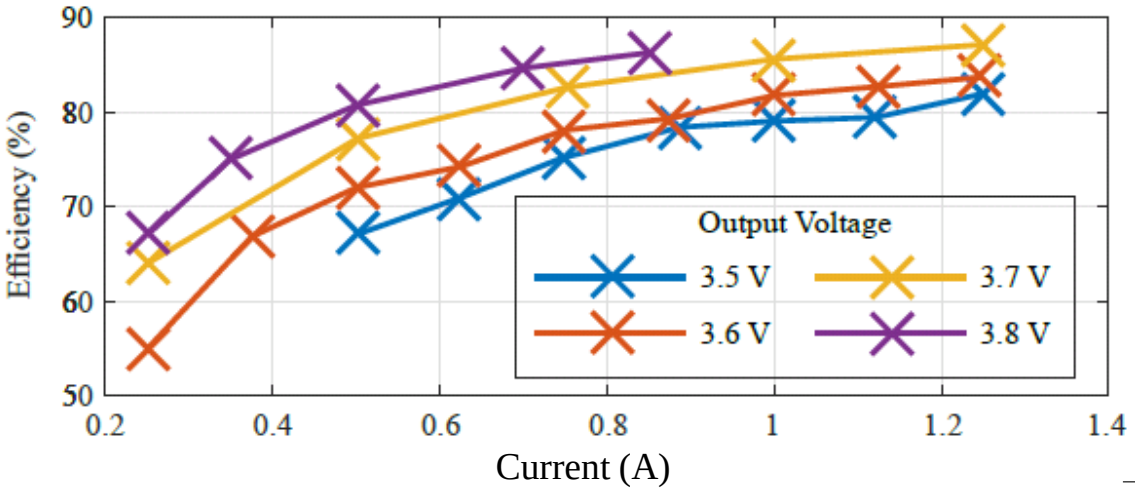


TABLE 5.1: PROTOTYPE SPECIFICATIONS

Parameter	Value
Process	180 nm CMOS
Active Area	10 mm^2
Max. Input Voltage	12 V
Conversion Ratio	3:1
Switch width	150 mm*
Switch channel length	500 nm
Flying capacitance	2x330 nF
Inductance	33 nH
Switching Frequency	1 MHz to 2 MHz

* width is doubled for M_5 and M_8

Conclusion

- Hybrid/Resonant SC topologies = great candidate high-density dc-dc converter
- Arbitrary N:1 converter → output impedance a useful tool for analysis and comparison
- Quality Factor → indexes performance in all modes, (without Q, you have nothing!)
- Multimode operation: great option for high efficiency across load range
- Any reasonable comparison must factor in the inductor: larger is better, but Q is the key driver

Thanks

THAYER SCHOOL OF ENGINEERING AT DARTMOUTH

This work was supported in part by NSF grants:
ECCS 1309905, ECCS-1407725, ECCS 1554265 (CAREER)