Fully-Integrated Digital Average Current-Mode Control Voltage Regulator Module IC

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IC division of Vishay Ltd. (Siliconix)
Controllers for VRMs and PoLs

Control Objectives

- Regulate the output voltage
- Obtain zero or small steady-state (DC) error
- Fast recovery from input and load changes
- Reasonable overshoot
Analog Controllers

+++ Still in the lead
✓ Accurate and efficient
✓ Fast response – wide bandwidth
✓ High (continuous) resolution
✓ Lower costs (<3A – All analog)

- - -

× Labor intensive
× Tailored compensation
× Pin count
× Limited flexibility/scalability
× Communication and interface
  \textit{Big D + Big A}
Digital Controllers

+++ - - -

✓ Comparable or better dynamics
✓ Reduced size of overall solution
✓ Scalable and flexible
✓ Auto-tuning - No compensation
✓ Plug-and-play
✓ Lower pin count
✓ Efficiency optimization

✗ Different design
✗ Power hungry
What do we really trade for a digital controller

- Mimicking analog controller operation by a digital one
- Conventional ADCs are too expansive
- High-res PWM is power hungry
- Do we ‘settle’ for voltage-mode

How “lean” can we go?

Protection, power management, etc. are still in…
Digital Architecture
Bottom up

Create an attractive alternative to analog control

• Hardware redesign
  – Focus on the benefits of digital electronics
    • Specifically targeted to power management
  – Avoid sensitive analog units
  – Standard-cell digital design (no custom design)

• Standardize the design flow
  – Reduce labor efforts
  – Easier testing
  – Faster development

One step ahead:
Entire controller created through code
## Digital Process

**Synchronous**

- ✔ Reliable
- ✔ Well-defined behavior
- ✔ Sequential or parallel

- × Power hungry (HS clk)
- × Synchronization hardware (e.g., clock tree)

**Asynchronous**

- ✔ Low power
- ✔ Ultrafast
- ✔ Area saving

- × Different design method
Objective

• Develop a compact All-digital controller architecture for VRM or PoL
• Entire hardware described through HDL
  – All standard digital design flow
  – No analog part
• Integrated switches (12V nominal input)
  – Minimize analog labor (drive)
Compensation type

Voltage-mode

\[ D[n] = D[n-1] + a v_{err}[n] - b v_{err}[n-1] - c v_{err}[n-2] \]

\[ D[n] = D[n-1] + a v_{err}[n] - b v_{err}[n-1] - c v_{err}[n-2] \]

3 multiplications + accumulator

Current-mode

\[ d[n] = d[n-1] + k \left[ i_{err}[n] - (1 - \frac{T}{t}) i_{err}[n-1] \right] \]

Single multiplication
Buck IC Conceptual diagram

Core controller
- Single-multiplier PI comp.
- Shared hardware
- 6-bit window ADC
- 12-bit HR-DPWM

Periphery
- SPI
- Programmable deadtime
Control flow

\[ v_c[n] = v_c[n-1] + av_{err}[n] - bv_{err}[n-1] \]

\[ a = k_p, \quad b = k_p \left( 1 - T_s / T_i \right) \]
Current (inner) loop

\[ d[n] = d[n-1] + k \left[ i_{err}[n] - (1 - \frac{T_s}{t}) i_{err}[n-1] \right] \]
Voltage (outer) loop

\[ v_e[n] = v_e[n-1] + k \left[ v_{err}[n] - (1 - \frac{T}{t})v_{err}[n-1] \right] \]
Timing sequence – key waveforms

- Ring-osc. generates mid-range frequency (10-20 MHz)
- Time-interleaved ADC
- Time scheduling PI operation

Each unit is designed as an asynchronous block
Delay-Line ADC

- Voltage-controlled delay
- Key factor – custom design of the delay cell
  - Not suitable for standard-cell synthesis
  - Difficult scalability
  - More complex layout
Constant-supply DL ADC

- 2-phase conversion: ATC + TDC
- ATC outside the buffer string
  - Realized by OS-timer
  - Digital gates
  - RC creates the analog link
  - No S&H
Window DL ADC
HR-DPWM
HS clock

- High power consumption
- High accuracy – very high clk freq
HR-DPWM
Delay-Line

- Area demanding

- Segmented DL
HR-DPWM
Segmented DL

- Low power consumption
- High accuracy
Gate driver

- Extended drain - similar to LDMOS structure
- Enabling the use of high drain-to-source voltages
- Compatible with ESD scenario
HS drive level shifter
Capacitive method

- Capacitive coupling level shifter
  - Short delay
- For higher shifting ratios (>2\(V_{DD}\)) – ladder configuration is essential
Level Shifter – current biased

Bias circuitry

\[ I_{Bias} = \frac{V_{ref}}{R_{ref}} \]
"Lean" Level shifter

Biasing circuitry (Analog) removed
Fully Integrated Digital ACM VRM IC

THE CENTER FOR POWER ELECTRONICS AND MIXED-SIGNAL IC, BEN-GURION UNIVERSITY

Fabricated IC

<table>
<thead>
<tr>
<th>IC Block / Digital Core</th>
<th>0.18μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>5V</td>
</tr>
<tr>
<td>DPWM resolution</td>
<td>12-bits</td>
</tr>
<tr>
<td>DPWM nominal frequency</td>
<td>1.25MHz</td>
</tr>
<tr>
<td>DPWM Si area</td>
<td>0.03 mm²</td>
</tr>
<tr>
<td>ADC resolution</td>
<td>6-bit</td>
</tr>
<tr>
<td>ADC conversion time</td>
<td>20nSec</td>
</tr>
<tr>
<td>ADC Si area</td>
<td>0.022 mm²</td>
</tr>
<tr>
<td>PI calculation time</td>
<td>&lt; 40nSec</td>
</tr>
<tr>
<td>PI Si area</td>
<td>0.034 mm²</td>
</tr>
<tr>
<td>Effective controller Si area</td>
<td>0.16 mm²</td>
</tr>
<tr>
<td>including Ring-Oscillator, Dead-Time and SPI</td>
<td></td>
</tr>
</tbody>
</table>
Experimental results

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>5x5 QFN - MLP</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>12V</td>
</tr>
<tr>
<td>Power-stage $R_{on}$</td>
<td>$\sim$ 160mΩ</td>
</tr>
<tr>
<td>Nominal $V_{out}$</td>
<td>1.5V</td>
</tr>
<tr>
<td>Nominal $I_{out}$</td>
<td>1.5A</td>
</tr>
<tr>
<td>Off-chip LC filter</td>
<td>2.2μH, 50μF</td>
</tr>
<tr>
<td>Switching frequency $f_{sw}$</td>
<td>1.25MHz (620KHz)</td>
</tr>
<tr>
<td>Peak efficiency</td>
<td>70% (76%)</td>
</tr>
<tr>
<td>***package limited</td>
<td></td>
</tr>
<tr>
<td>Total chip Si area</td>
<td>4.4mm²</td>
</tr>
</tbody>
</table>

- $f_{sw} = 620$KHz
- $f_{sw} = 1.25$MHz
- $V_{out} = 1.5$V
- $I_L = 12$V

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[Image of buck IC and circuit diagram]
Loading Transient

Loading transient 1.5A -> 2.5A
Vin=12V, Vout=1.3V
Unloading Transient

Unloading transient 2.5A -> 1A
Vin=12V, Vout=1.3V,

\[ V_{\text{out}} = 30 \text{mV} \]
\[ f_{\text{SW}} = 1.25 \text{MHz} \]
\[ 20 \mu s \]

\[ I_L = 2.2 \text{A} \]
\[ 1.5 \text{A} \]

\[ V_{\text{sw}} \]

\[ V_{\text{out}} = 70 \text{mV} \]
\[ f_{\text{SW}} = 620 \text{KHz} \]
\[ 20 \mu s \]

\[ I_L = 2.5 \text{A} \]
\[ 1 \text{A} \]

\[ V_{\text{sw}} \]
Acknowledgements

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Thank You!