Towards Fully Integrated Power Management

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Texas Instruments
The Power Management End-Game

Invisible → 100% Efficiency, 0 Volume
Easy-to-Use → Complete power management in 1 chip, no EMI

**Power Supply On a Chip**

**Devices**
- Conduction Losses
- Charge Losses

**Passives**
- Magnetics
- Capacitors

**Parasitics**
- Device Ringing – IV Overlap
- Reverse Recovery
Typical Loss Breakdown – Buck Converter

**Conduction**
- IV- Overlap Losses: 37%
- 26%
- 21%
- 16%

**Device Switching Losses**
- Overlap
- quil/diode
- switching
- conduction

*Topologies Can Improve Upon Some or All of the Above*
# Topology Classes

<table>
<thead>
<tr>
<th>Standard Converters</th>
<th>Hybrid Converters</th>
<th>Resonant Converters</th>
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<tr>
<td><img src="image1.png" alt="Standard Converter Diagram" /></td>
<td><img src="image2.png" alt="Hybrid Converter Diagram" /></td>
<td><img src="image3.png" alt="Resonant Converter Diagram" /></td>
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- **✓ Simple and proven**
- **✓ Low Cost**
- **✗ Hard Switched**
- **✗ Full VIN rated devices**

- **✓ Reduced Device Voltage Stresses**
- **✓ Reduced Energy Storage In Inductors**
- **✗ Hard Switched**
- **✗ Additional Component(s)**

- **✓ Reduced or eliminated switching losses**
- **✓ Majority of energy storage still in L**
- **✗ Additional Component(s)**

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TI Information

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Hybrid Converter Example

- **Advantages**
  - More energy storage in caps, less in inductors
  - Lower switch ratings and stress
  - Smaller current ripple

- **Disadvantages**
  - Added component
  - Duty cycle limitation

[Nishijima, 2005]
[Shenoy], 2015

17x smaller footprint
34X smaller volume
Hybrid Converter Example

- \( V_{IN} \) – VC Applied to \( L_1 \)
- \( V_C \) charged through phase 1 path
- \( L_2 \) current decreases

[Nishijima, 2005]
[Shenoy], 2015
Hybrid Converter Example

- Current in both inductors decreases
- No current flowing through $V_c$

[Nishijima, 2005]
[Shenoy], 2015
Hybrid Converter Example

- \( L_1 \) current decreases
- \( V_C \) Applied to \( L_2 \) → Becomes Phase 2 source
- \( L_2 \) current increases

[Nishijima, 2005]
[Shenoy], 2015
Hybrid Converter Example

- Current in both inductors decreases
- No current flowing through $V_c$

[Nishijima, 2005]
[Shenoy], 2015
Hybrid Converter Example

- Capacitor Voltage and Inductor currents naturally balanced
- More energy storage in the capacitor, less in inductors
- Device rated for $V_{IN}/2$
- X Hard Switched
- X Additional Component(s)
- X Duty Cycle Limitation
Advantages – Capacitors vs. Inductors

- Capacitor Voltage and Inductor currents naturally balanced
- More energy storage in the capacitor, less in inductors
- Device rated for $V_{IN}/2$
- Hard Switched
- Additional Component(s)
- Duty Cycle Limitation
Rsp Advantages

- Capacitor Voltage and Inductor currents naturally balanced
- More energy storage in the capacitor, less in inductors
- **Device rated for** $V_{IN}/2$
- X Hard Switched
- X Additional Component(s)
- X Duty Cycle Limitation

* B. El-Kareh, L. Hutter, "Silicon Analog Components"

~8V Rated
~0.1m$\Omega$-mm$^2$

~16V Rated
~0.6m$\Omega$-mm$^2$

- Enables Smaller Die Area -- $$ Savings
FOM Advantages

- Capacitor Voltage and Inductor currents naturally balanced
- More energy storage in the capacitor, less in inductors
- Device rated for $V_{\text{IN}}/2$
- X Hard Switched
- X Additional Component(s)
- X Duty Cycle Limitation

- ~8V Rated
- ~16V Rated

• ~3x-5x better FOM in this example
CV² and I-V Overlap Losses

- **Hard Switching Losses Reduced**
  - 1/2CV²
  - V/2 and C decreases w/FOM improvements
  - IV Overlap – \( \frac{1}{2} V_{\text{IN}} I_L t_r \)
  - Assume same DV/DT and DI/DT as a Buck
  - \( t_r \) halves, 2x more transitions,
  - 1/4 the transition losses

- Capacitor Voltage and Inductor currents naturally balanced
- More energy storage in the capacitor, less in inductors
- **Device rated for** \( V_{\text{IN}}/2 \)
- X Hard Switched
- X Additional Component(s)
- X Duty Cycle Limitation
Buck Converter vs. SC Buck

- IV- Overlap Losses: 37%
- Device Switching Losses:
  - Overlap: 26%
  - qrr/diode: 21%
  - Switching: 16%

Conduction

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Adding It All Up

- Dramatic Size Reduction
- Efficiency the same or better than comparison points
- Major downside of duty cycle limitations
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- **X Additional Component(s)**
- **✓ Reduced or eliminated switching losses**
- **✓ Majority of energy storage still in L**
- **X Additional Component(s)**
Resonant Converter Example

Resonant Converter Example

- Typical Buck Operation
- Inductor current slews down
Resonant Converter Example

- Q2 remains ON holding switched node at ground
- SAUX turns ON ramping up current in LAUX
- Once AUX current is greater than L current, Q1 Coss conducts
Resonant Converter Example

- Turn ON Q1 with ZVS
- LAUX current ramps down to zero after which SAUX is turned off
Resonant Converter Example

- Q1 conducts remainder of interval as in typical buck converter
Resonant Converter Example

- ZVS turn on of Q₁
- ZCS turn off of \( S_{\text{AUX}} \)
- No I-V turn on losses for Q₁

X Added conduction losses for \( S_{\text{AUX}} \)
X Added die area for \( S_{\text{AUX}} \)
X Extra component losses
## Analysis and Comparison

### Loss Breakdown

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<th>ZVT (1MHz)</th>
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<tr>
<td>Cond. Loss $L + L_{AUX}$</td>
<td>1.0x</td>
<td>~2.3x</td>
</tr>
<tr>
<td>$Q_{OSS}$</td>
<td>1.0x</td>
<td>0.5x</td>
</tr>
<tr>
<td>$Q_{rr}$</td>
<td>1.0x</td>
<td>0x</td>
</tr>
<tr>
<td>IV-Overlap (ON)</td>
<td>1.0x</td>
<td>0x</td>
</tr>
<tr>
<td>IV-Overlap (OFF)</td>
<td>1.0x</td>
<td>1.0x</td>
</tr>
<tr>
<td>$D_{RR}$ Cond.</td>
<td>1.0x</td>
<td>0.2x</td>
</tr>
<tr>
<td>$P_{GATE}$</td>
<td>1.0x</td>
<td>1.2x</td>
</tr>
<tr>
<td>$P_{TOT}$</td>
<td>1.0x</td>
<td>0.96x</td>
</tr>
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**Vs. 20% Smaller Die**
Buck Converter Vs. ZVT

- Conduction: 26%
- IV- Overlap Losses: 37%
- Device Switching Losses:
  - Overlap: 21%
  - qrr/diode: 16%
  - QRR: 21%
  - Conduction: 26%
Opportunities

- If cost is a non-factor (usually isn't), large efficiency gains possible
- Other main challenge → The Magnetic element
  - Conduction Losses
  - Core losses
  - Cost
  - Size

Vs. 20% Smaller Die
Summary

New Topologies offer opportunity to move towards full power supply on a chip
Options and alternatives with various pros and cons

Still need improvements on:
- Inductor integration
- Capacitor integration
- Better FETs
- Better packages
Questions