Challenges of integration of power supplies on chip

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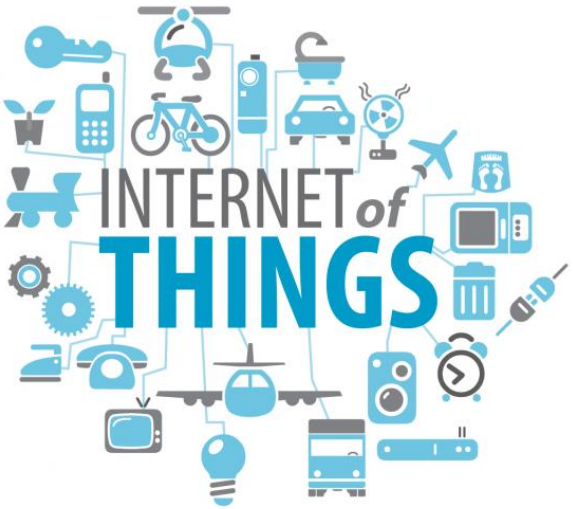
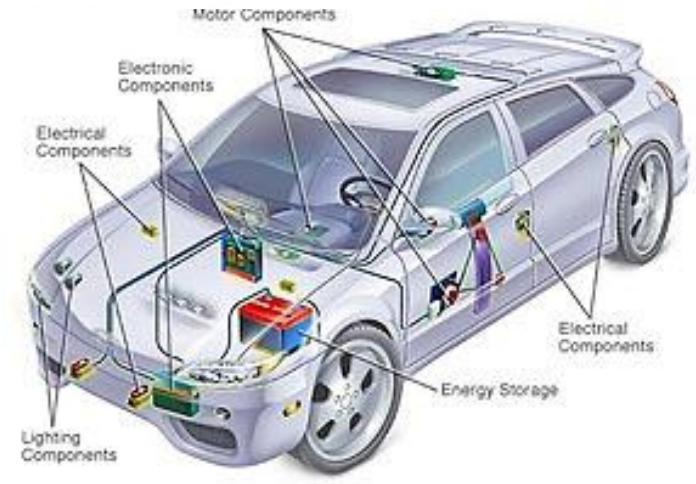
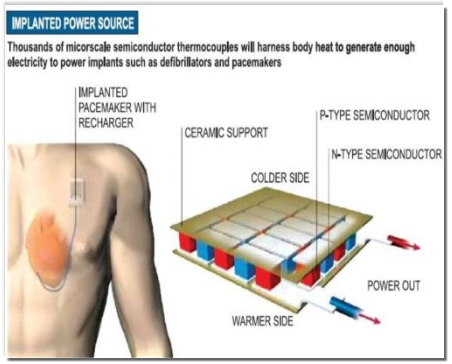
Why this is important:

- There is significant trend in the industry towards power density and integration in power supplies.
- This trend is due to internet of things and ever decreasing form factor.
- This integration has given rise to many complex issues such as power efficiency, building power supplies in nanometer CMOS, power supply noise coupling and increased thermal dissipation.
- This talk discusses these issues and future trends.

Applications where integration is critical







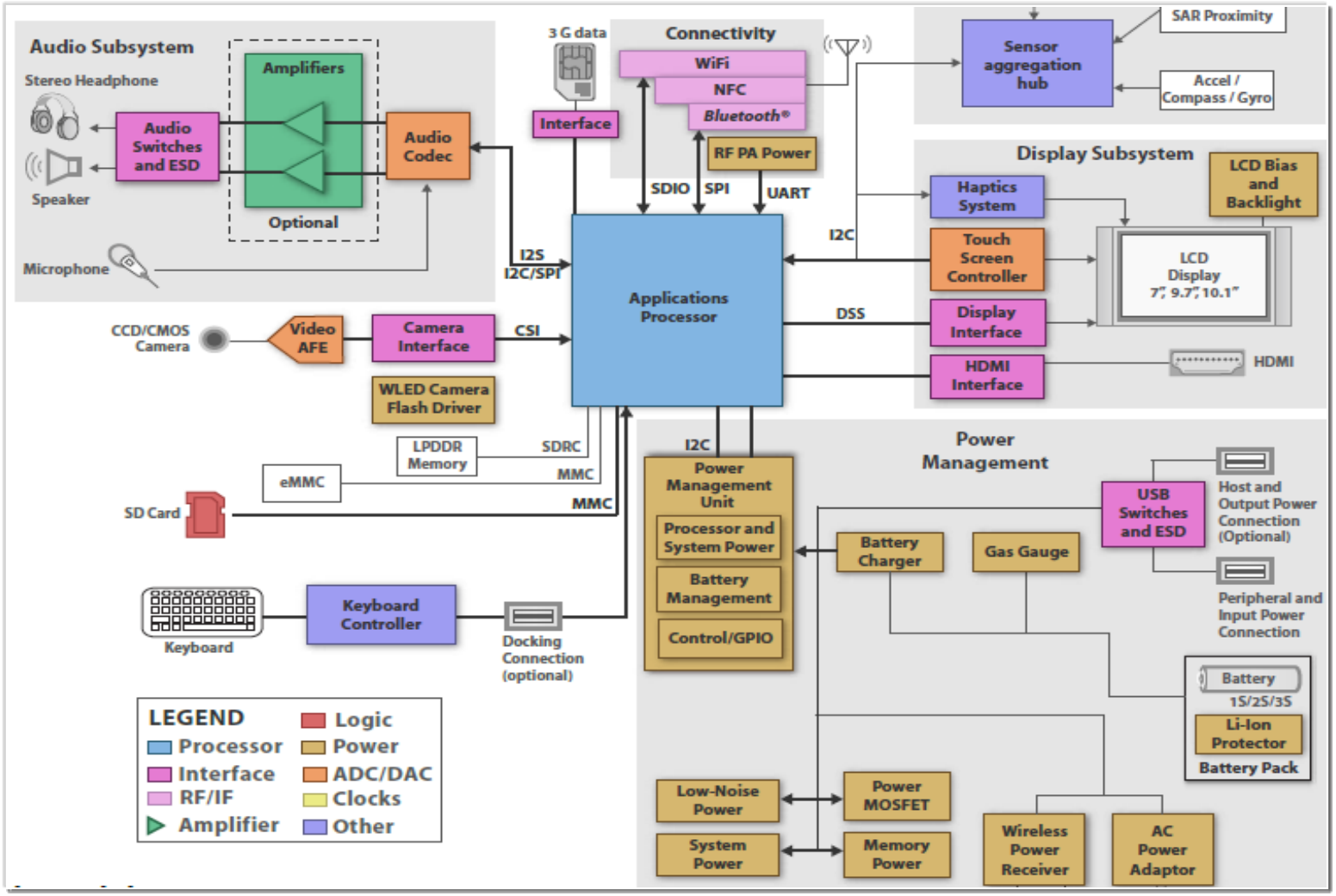
The Internet of Things (IoT)

- **The Internet of Things (IoT)**

- In the past: computers, tablets, phones
  - In the future: almost anything!
    - Home, car, office
    - Toaster, fridge, tooth brush
    - Light bulb, pill bottle, pop-tart package
  - Volumes will be huge
  - Market will be fragmented

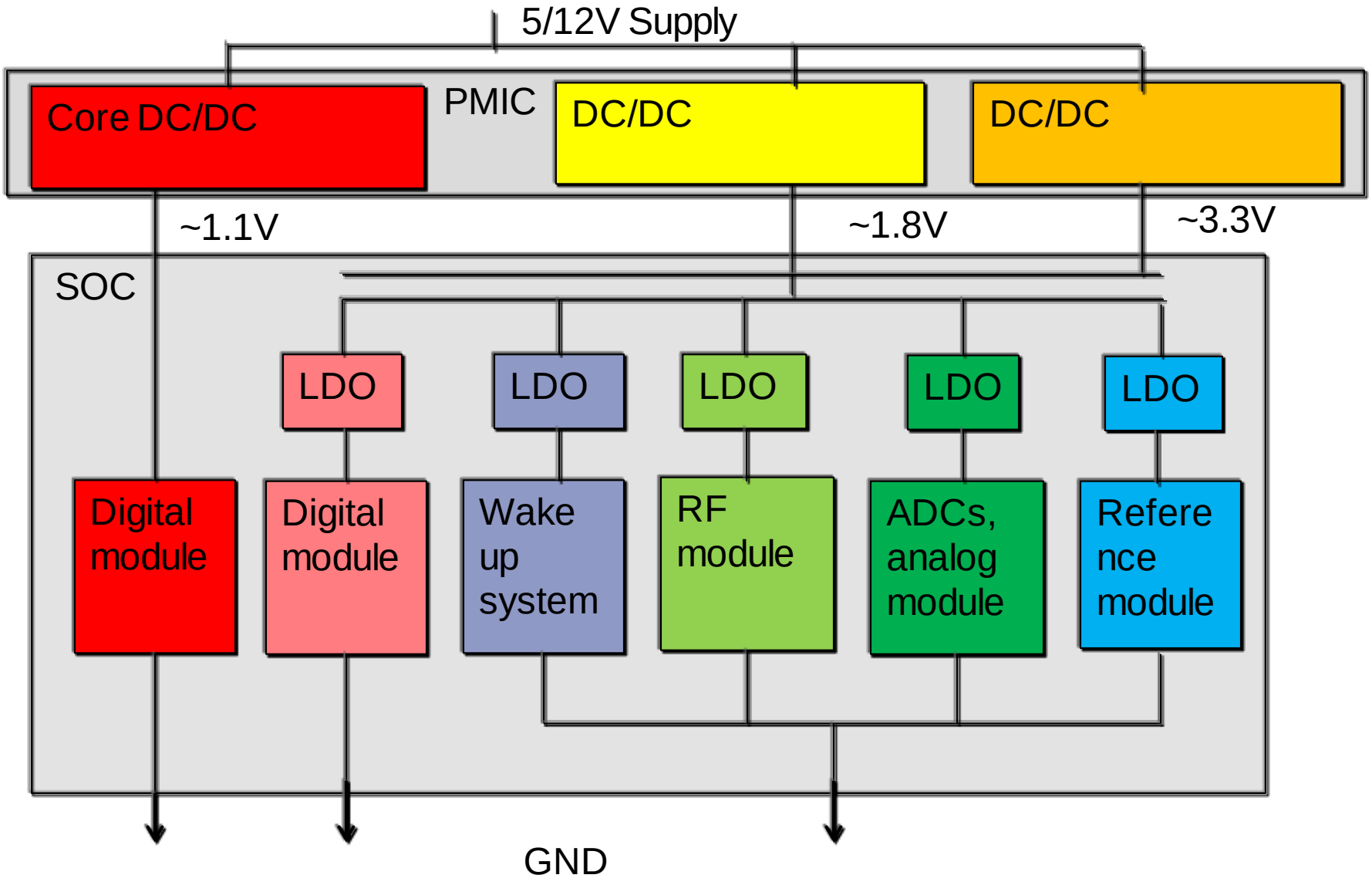
- **Where do we fit in?**
  - Tight spaces, low cost - power management in chip needs new solutions
  - Ultralow power (energy harvesting, coin cells) needs new solutions

Tablet power system



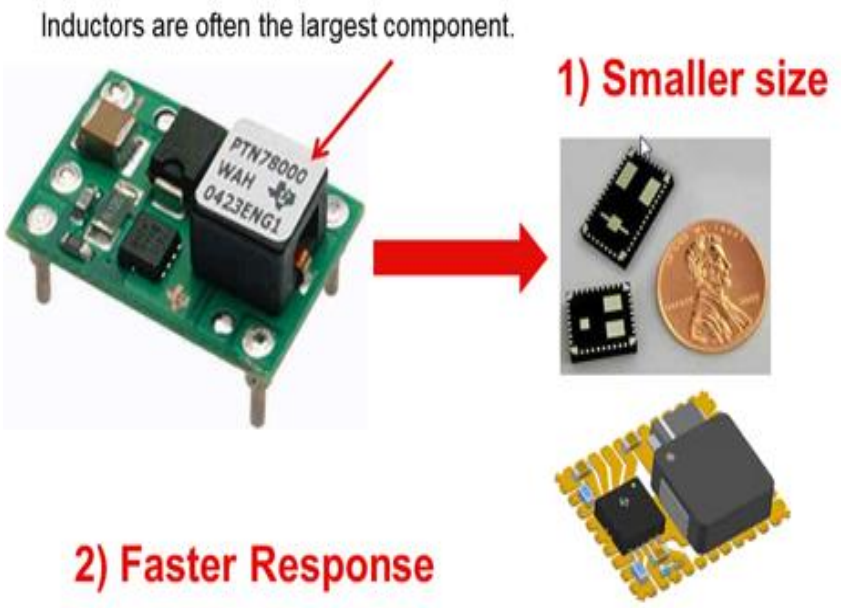
http://www.ti.com/general/docs/lit/getliterature.tsp?baseLiteratureNumber=slyy028&fileType=pdf

Todays SoC power supply architectures

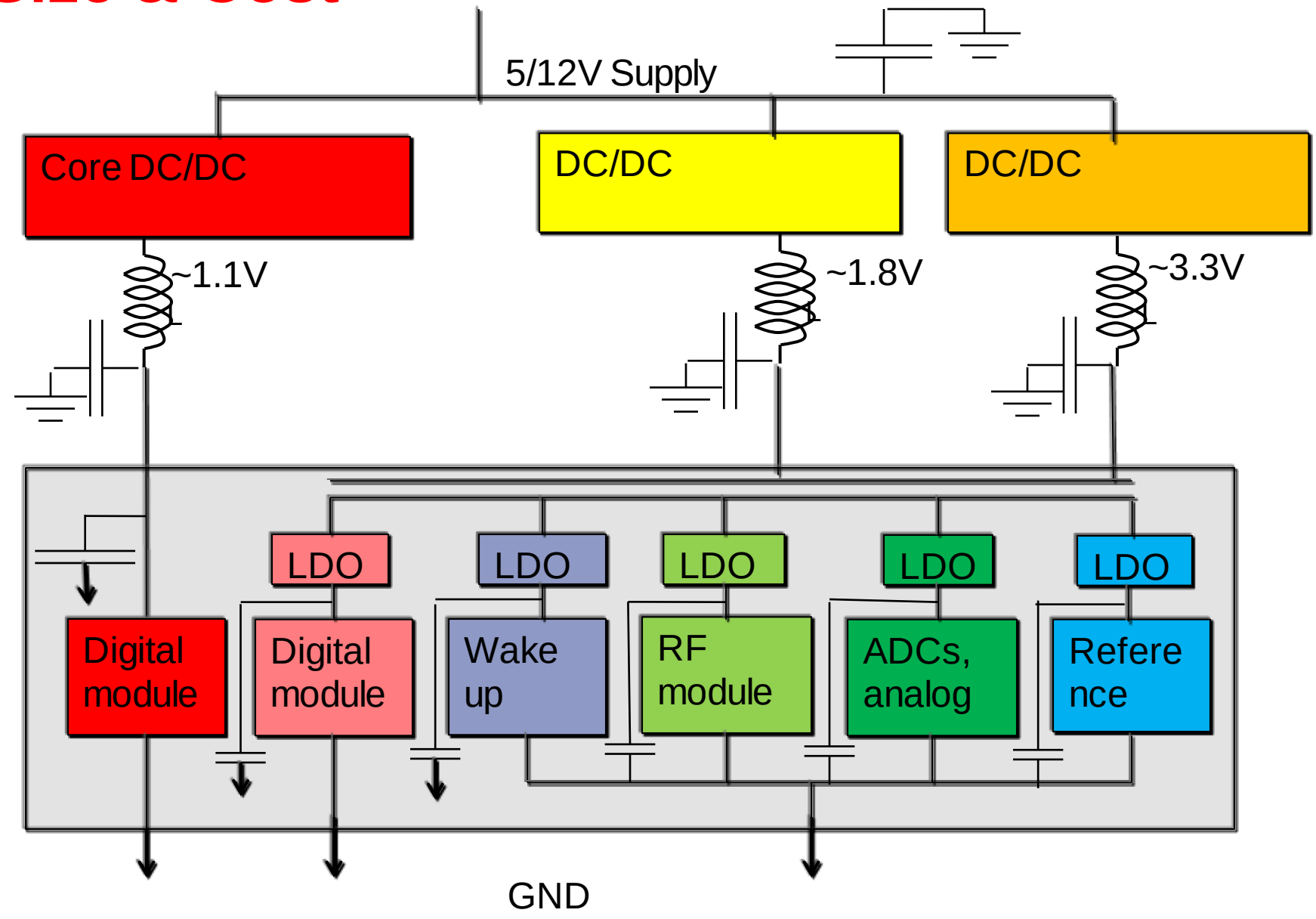


Challenges

Size & cost - There are multiple power supplies in SoCs with many external inductors and capacitors



Size & Cost


5/12V Supply
Core DC/DC
DC/DC
DC/DC
~1.1V
~1.8V
~3.3V
LDO
LDO
LDO
LDO
LDO
Digital module
Digital module
Wake up
RF module
ADCs, analog
Refere nce
GND

Size and Cost

- Higher switch frequency - > reduces inductor size
- SIMO converters -> reduces number of inductors
- Hybrid (SC & Buck) converters -> Reduces inductor size

Challenges

Efficiency

- DC/DC –> Low Qg, Low RdsON MOS, New topologies
- Processor/SoC core
  - Dynamic voltage scaling based on speed
  - Dynamic frequency scaling based on need
  - Adaptive voltage scaling based on process variations
  - Turn off modules, Clock gating

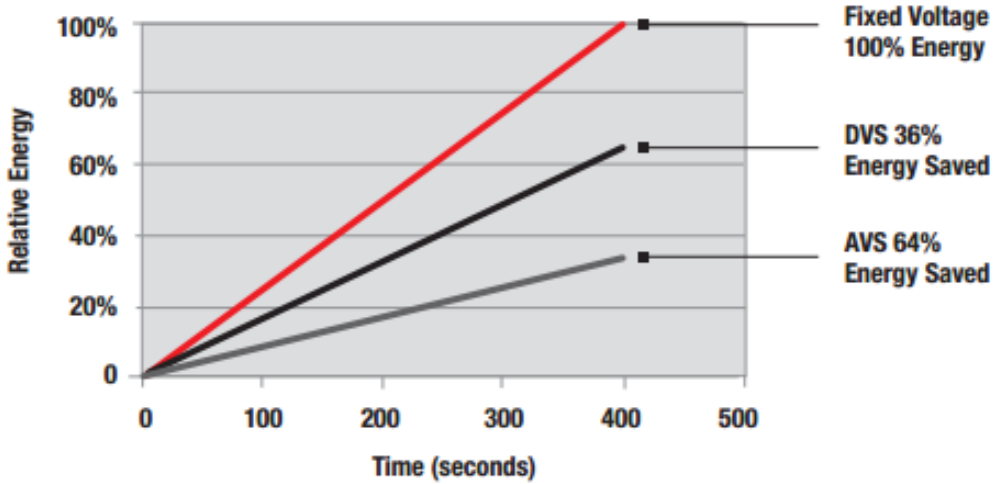


Figure 3. Energy savings with PowerWise AVS

http://www.ti.com/lit/ml/slyb186/slyb186.pdf

Challenges

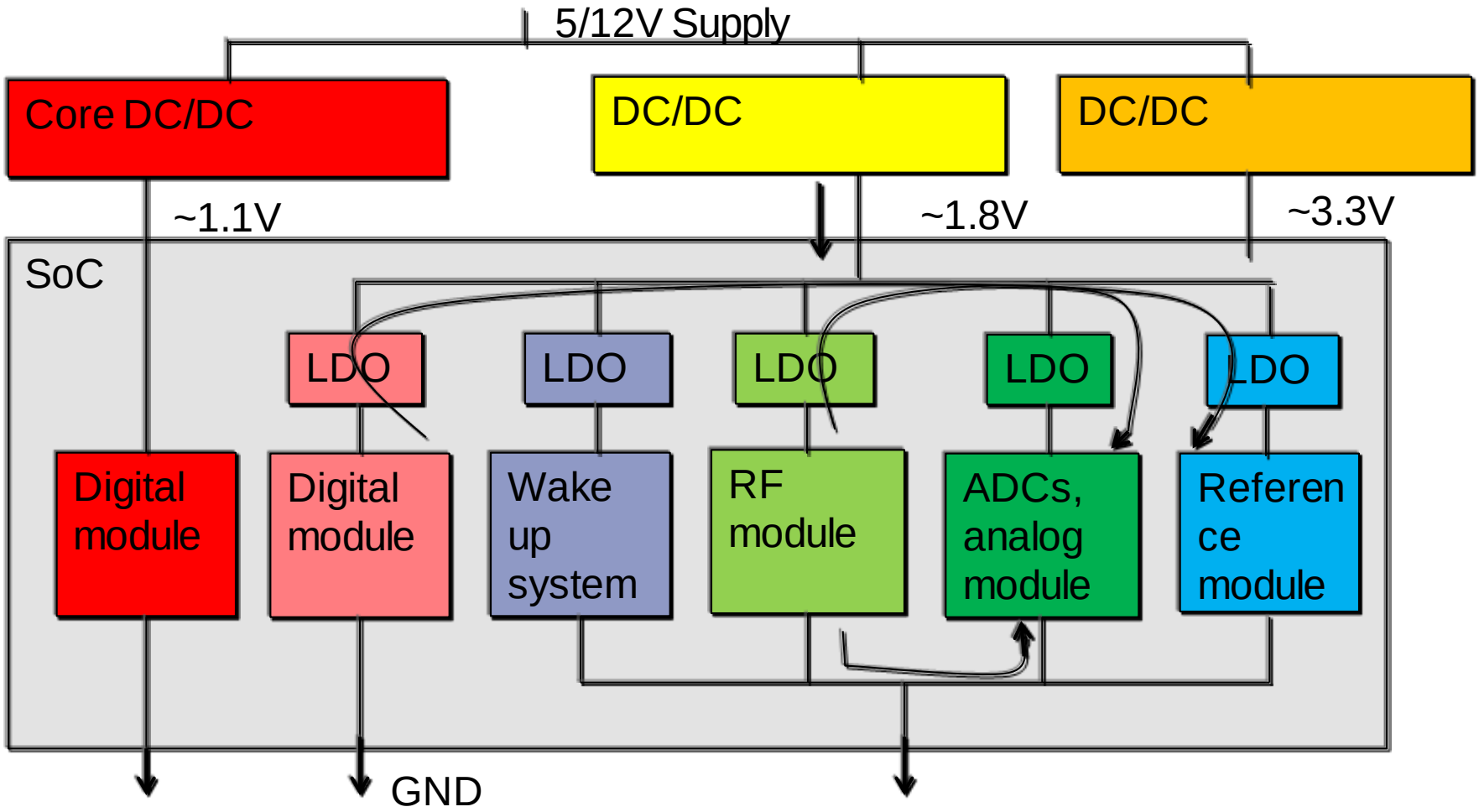
Transient response

- SoC Load surge causing Supply voltage droop – Getting worse with higher core current and lower core voltage
  - Look ahead voltage scaling
  - Current mode DC/DC
  - Multi phase DC/DC

Too many pins

- Power pins -> Reduce the number of major power domains (increases the number of LDOs, reduces efficiency)

Noise coupling through supply & substrate



Solutions:

If source is in PMIC – higher sw freq, multi phase, multi level converters

If source is on SoC - - On chip decoupling, Isolation in substrate, Power bus Isolation

Challenges

Thermal

- SoC core heat dissipation -> core temperature based Adaptive voltage and frequency scaling
- LDO heat dissipation - > reduce drop out, external LDO

Need for low quiescent current (sleep , stand by)

-> At light load PFM, Pulse skip

-> Turn off blocks not used, clock gating

-> DC/DC Dead time reduction

Automotive 12V Electrical system challenges

- Wide Vin (3.5 – 40/60V)
- Stringent EMI requirements
- High power density – LED systems, Converters
- High temperature operation
- Reliability of safety critical systems -> Failure prediction, Diagnostics, robust power switches

Future trends in Integration

Why it is difficult to integrate power supply into SoC?

Semiconductor Process

Low on resistance LDMOS is not typically available in state of the art digital process (e.g Fin FET)

- High voltage Devices not available
- High current metal system not available.
- High voltage capacitors not available.

SoC cannot handle thermal dissipation of converter

Large inductor & capacitor needed for DC/DC

Future trends - Process

Integration of active and passive components

- Trench capacitors in silicon
- Laminate inductors in MCM
- On silicon inductors

Finer geometry digital process with LDMOS

BCD processes with digital scaling to deep submicron

0.35->0.25->0.18->0.13um->TBD digital with high voltage LDMOS

Future trends - Process

Lower Qg, Coss, Ron LDMOS in digital process

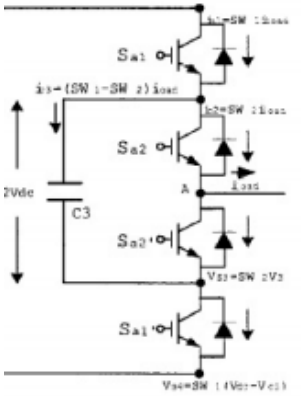
- Enables sophisticated digital control in PMIC
- Enables higher switching speed

Low ON resistance power process IC co-packaged with a nanometer CMOS digital IC

Future trends - Topology

High frequency converters

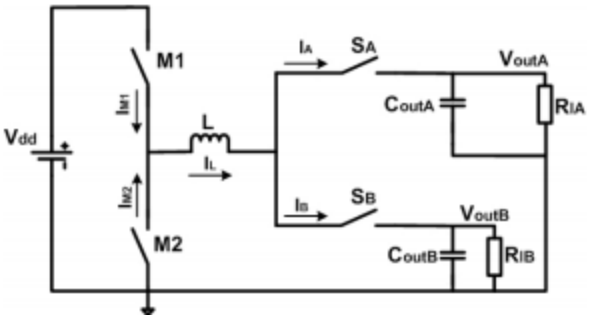
- Reduces inductor size
- Enables integration of inductor on PMIC



Multi level converters

- Use of low voltage FETs
- Reduces ripple, reduces inductor size

SIMO Converters



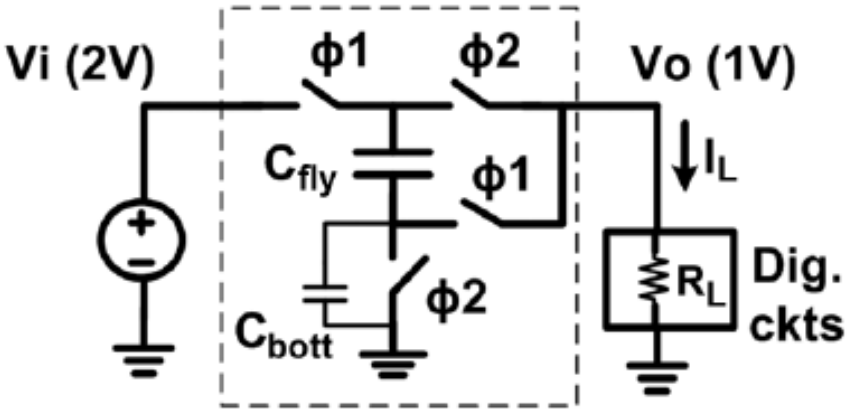
- Reduces number of inductors
- How to Mix large loads, light loads, load transients

http://ims.unipv.it/~franco/ChapterBooks/10.pdf

Future trends - Topology

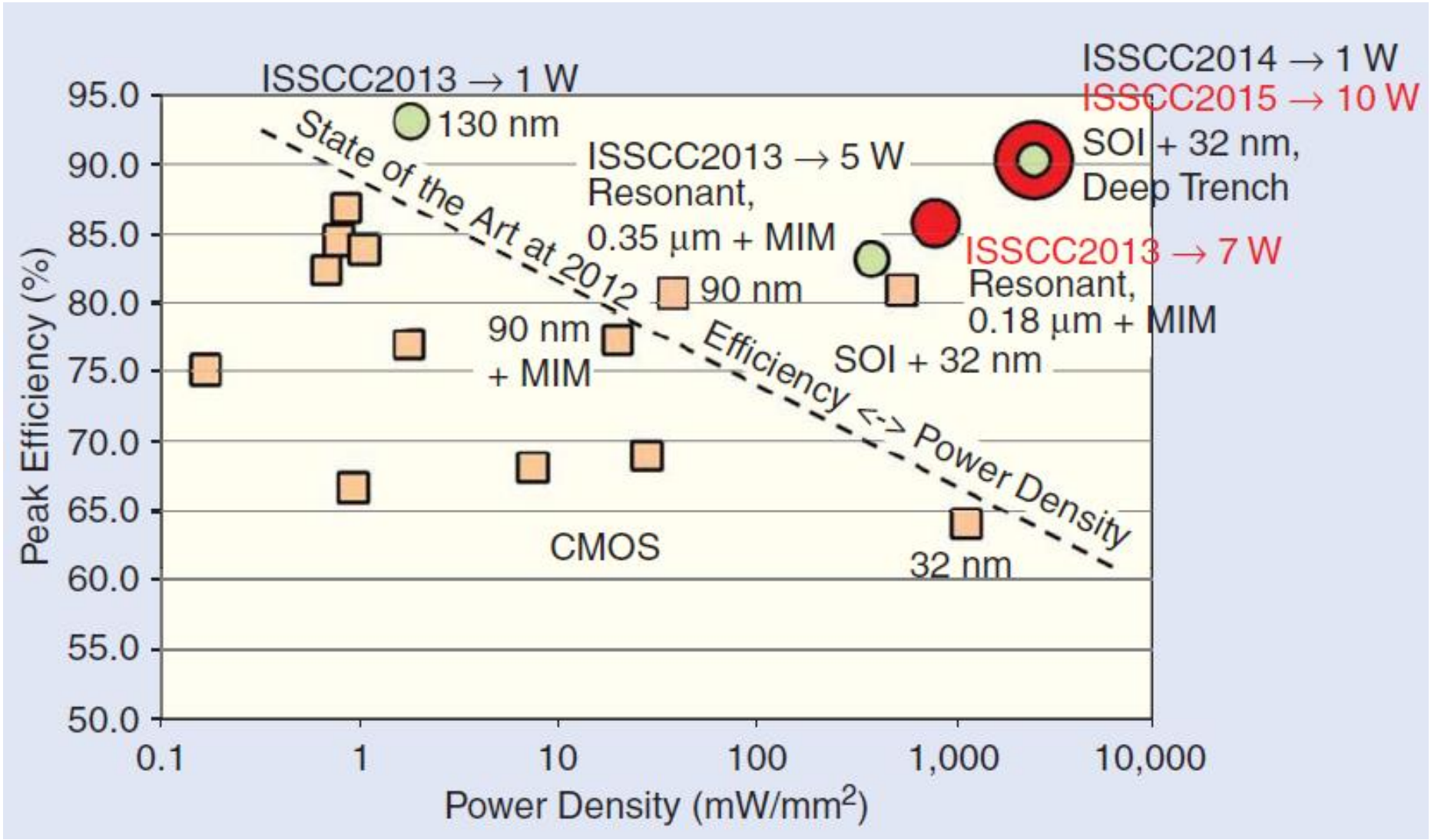
Switched capacitor & Hybrid converters – Capacitor has higher energy density than inductors

- Potential to integrate low load converter using trench cap or external cap
  - Issue in how to handle variable conversion ratios
- Hybrid SC & Buck topologies -> smaller inductor



Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters - Hanh-Phuc Le et al JSSC

Switched capacitor power converters



Technology trends – IEEE SSC Magazine winter 2015

Texas Instruments

PMIC - SoC potential future for the industry