Close supply chain collaboration enables easy implementation of chip embedded power SiP

Gerald Weidinger, R&D Project Leader, AT&S
History of embedded Die Technology

1970

Concepts

1980

Research

1990

Development Projects

2000

Industrialization

2004

Serial Production

2006

Embedded silicon

2008

Embedded Chip

2010

Printed capacitor

2012

Discrete capacitor

2014

Printed resistor

2016

Discrete resistor
<table>
<thead>
<tr>
<th>Unique Selling Propositions</th>
<th>... in detail</th>
</tr>
</thead>
</table>
| **Miniaturization**         | • Footprint reduction  
                             | • Higher component integration (additional assembly layer)  |
| **Electrical performance**  | • Improved signal performance (higher data rates)  
                             | • Reduction of parasitic effects  |
| **Mechanical performance**  | • Higher durability and reliability through copper-to-copper connections (copper filled microvias)  
                             | • Package enables protective enclosure  
                             | • High drop, shock and vibration tolerance  |
| **Thermal management**      | • Improved heat dissipation through direct copper connection  
                             | • Improved heat dissipation FR4 versus air (compared to SMD)  |
| **Additional functions**    | • EMV shielding (partial or full shielding of a package)  
                             | • Package is the housing → no additional molding required  |
| • Reduction of overall cost | • Lower set-up costs compared to other packaging technologies (packaging versus PCB processes)  
                             | • Customization of footprint and module versions can be done due to digital imaging - no separate tooling necessary (e.g. QFN)  |
| • EMI shielding              | • Hidden electronics preventing reverse engineering and counterfeiting  |

ECP is supporting the trend towards modularization
Embedding Technology Industrialization

Our collaboration enables customers success

- Global footprint
- Strong R&D focus
- High volume manufacturing experience, capacity, and capability
- Brought product portfolio
- Strong customer base
- Long history in embedded technology

Alignment on
- Business processes
- Aligned technical capabilities
- Common focus on segments and applications

- Global footprint
- High volume manufacturing experience, capacity, and capability
- Excellent testing capabilities
- Strong customer base
- Brought experience in backend processing of various applications
Strategic supply chain collaboration is a key success factor.

Supply Chain Offering

Co-Design
Wafer to Die
Substrate embedded chip
Package assembly
Test

Alignment on Design
Rules & Roadmaps
- Substrate design
- Assembly design
- Design integration

KGD test
RDL
Thin / Dice
Inspect / TnR

Substrate manufacturing
Embedded chip
Strip Test

SMT
Top FC / under fill
Cap or Mold
Solder Ball Attach
Package saw

Package level test
Reliability test

April 2015 - Joint marketing / supply chain agreement between AT&S and UTAC for 3D SiP with embedded chip technology. Collaboration press release April 2016. AT&S over 5 years production embedding experience.
UTAC at a glance

• Outsourced Semiconductor Assembly and Test services (OSAT) provider in support of Analog, Mixed-Signal, Logic, Power and Memory products.

• UTAC 2015 Revenue $878M; Ranked 6th in the Top Ten OSATs

• Focus – Assy, Test and Full Turnkey; Test comprises 35% of sales in 2015.

• 1997 Established in Singapore

• Mfg Footprint - Singapore, Taiwan, Malaysia, Indonesia, Thailand, China.

• >260K M² Manufacturing Space and ~ 12K Employees Globally.

• Sales offices located worldwide.

• Markets: Mobile Phone, Automotive, Security, Wearable’s, Industrial & Medical.
UTAC at a glance

**UTAC Dongguan, China (UDG)**
- [Since 1988, >500k sq ft, China Logistics, WW distribution]
- BGA, LGA, QFN, Memory Cards, USB, SiP
- 3D SiP w/ Embedded chip

**UTAC Thailand (UTL)**
- [Since 1973, 640k sq ft, Auto & Security certifications.]
- QFN, GQFN, LGA, MIS, MEMS, Power QFN with Cu Clip

**UTAC Shanghai, China (USC)**
- [90k sq ft, WGQ Free trade zone, Focus - Asia customers]
- QFN, FBGA, LGA, MIS
AT&S – a world leading high-tech PCB company

High-End Interconnection Solutions for Mobile Devices, Automotive, Industrial, Medical Applications

Continuously Outperforming market growth

One of the most profitable Players in the Industry: EBITDA margin of 22% in FY 2015/16

# 3 in High-End Technology worldwide

€ 762.9m Revenue in FY 2015/16, 5.2% organic growth

# 1 manufacturer in Europe

9,165 employees

Cost-competitive production footprint with 6 plants in Europe and Asia
AT&S at a glance & global footprint

BU AIM Headquarters
Plant Leoben, Austria
Headquarters
Staff: ~950
Customer Orientation:
9% Automotive
91% Industrial

BU AIM
Plant Fehring, Austria
Staff: ~350
Customer Orientation:
44% Automotive
56% Industrial

BU AIM
Plant Nanjangud, India
Staff: ~1.100
Customer Orientation:
60% Automotive
40% Industrial

BU MS
Plant Shanghai, China
Staff: ~4600
Customer Orientation:
84% Mobile Devices
14% Automotive
2% Industrial

BU AIM
Plant Ansan, Korea
Staff: ~280
Customer Orientation:
13% Automotive
47% Industrial
40% Mobile Devices

BU MS
Plant Chongqing, China
Staff: ~1800

AT&S AG Headquarters
Leoben, Austria

AT&S AG
Headquarters

Sales Offices /Representations
Business Unit Mobile Devices & Substrates (BU MS)
Business Unit Industrial & Automotive (BU IA)
ECP® Basics – What’s ECP®

AT&S ECP® - Embedded Component Packaging

ECP® (Embedded Component Packaging) uses the space in an organic, laminate substrate (Printed Circuit Board) for active and passive components integration.

Components embedding into the PCB core with copper plated microvia connections.
ECP® Basics – Keyfacts

AT&S ECP® - Embedded Component Packaging

- Active and/or passive components
- Copper surface on IO’s
  - Thickness 100µm - 350µm
    - In development: 80 – 500µm
- Laser drilled microvias
- Galvanic copper plating
- HDI PCB processes
- PCB material and processes
- Various combination of stack-ups possible
- Miniaturization
- Reliable interconnection
- Performance
- Protection of components
Product Illustrations

**X-section of embedded devices**

---

**For interconnection, same technology and processes as for HDI/microvia PCBs!**

---

CT image of embedded caps in a 4 layer PTH board
Package Type: 4.5 x 7.2mm LGA-SIP
Highlights: 2 embedded die + 24 passive components on substrate top side

<table>
<thead>
<tr>
<th>Package size / Type</th>
<th>4.5 x 7.2 mm LGA-SIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Thickness</td>
<td>560 um ± 10%</td>
</tr>
<tr>
<td></td>
<td>320um core</td>
</tr>
<tr>
<td>Die thickness</td>
<td>200 um Max.</td>
</tr>
<tr>
<td>Surface finish (Die DAP)</td>
<td>Electrolytic NI/AU</td>
</tr>
<tr>
<td>Surface finish (Land Pad)</td>
<td>Electrolytic NI/AU</td>
</tr>
<tr>
<td># of Passive Component</td>
<td>24ea Passive</td>
</tr>
<tr>
<td>(Top of substrate surface)</td>
<td></td>
</tr>
<tr>
<td>Component Sizes</td>
<td>Passive</td>
</tr>
<tr>
<td></td>
<td>10ea 01005, 10ea 0402, 4ea 0201.</td>
</tr>
<tr>
<td># of embedded chip</td>
<td>2</td>
</tr>
<tr>
<td>Strip Size</td>
<td>188x64mm</td>
</tr>
<tr>
<td>Substrate Metal layer</td>
<td>4 Layer</td>
</tr>
</tbody>
</table>
Summary

- System in a package (SiP) is a strategic focus area for UTAC and AT&S
- 3D SiP with Embedded Chip provides integration, size and performance benefits over 2D planar SiP solutions
- 3D Embedded Chip technology adoption is accelerating in Power and High Density Interconnect Applications
- Supply chain collaboration for emerging 3D SiP solutions with embedded chip technology will advance the technology and provide full turnkey (FTK) supply solutions for customers.
- Flexible business models available to fit to customer requirements
AT&S first choice for advanced applications