



**CEIUPM**

Centro de  
Electrónica  
Industrial

# CAD Tool for the optimization of Power Converters on Chip

Jesús A. Oliver, Pedro Alou and José A. Cobos

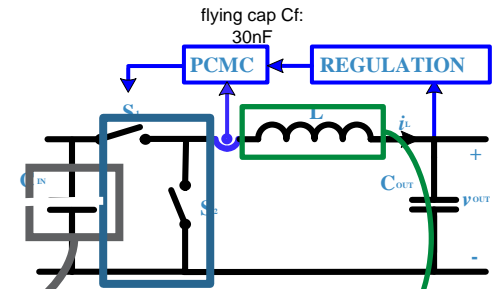
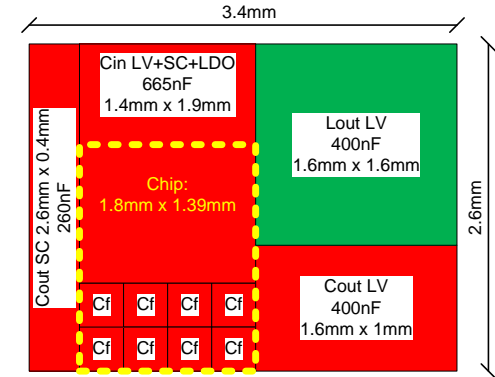
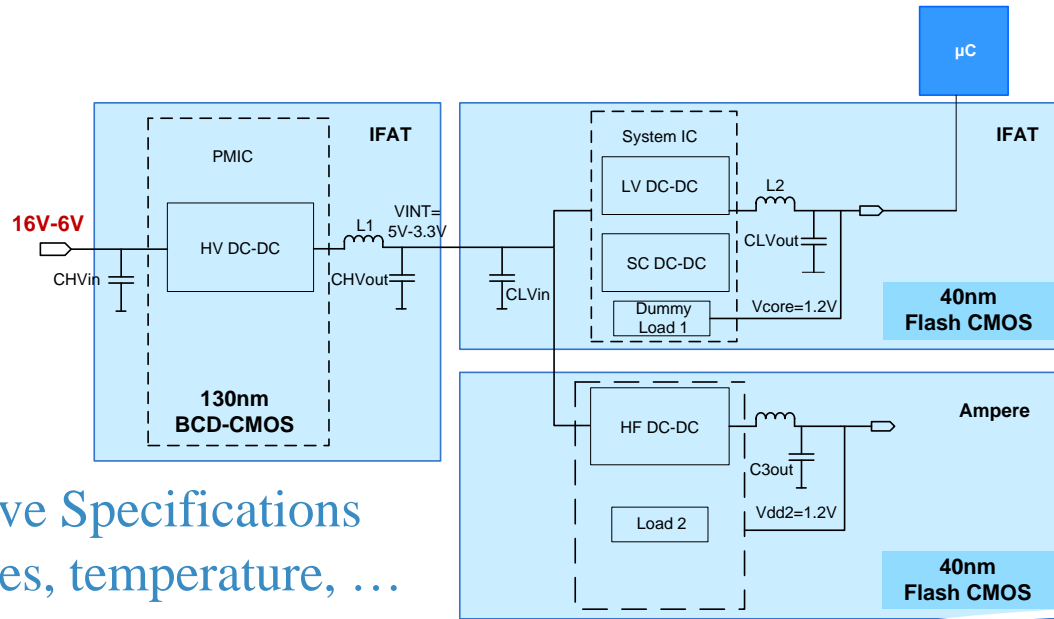
PWRSoc 2016 Madrid

UNIVERSIDAD POLITÉCNICA DE MADRID

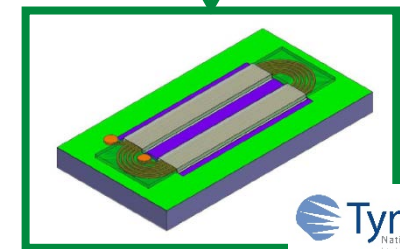
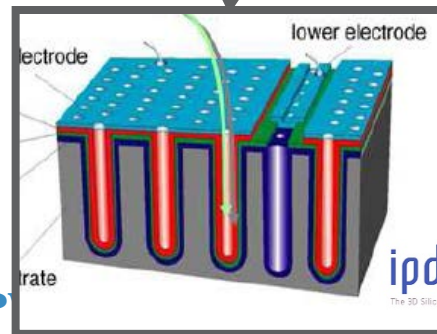
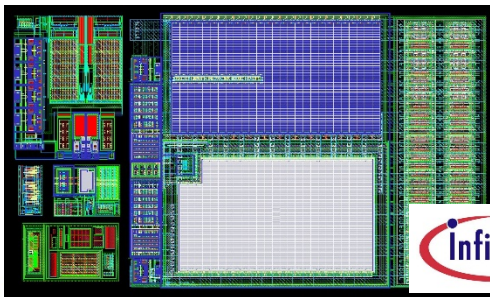
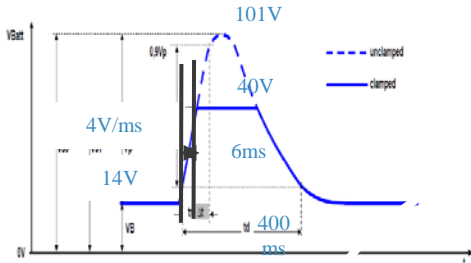


POLITÉCNICA

# The need of an integrated multi-domain tool

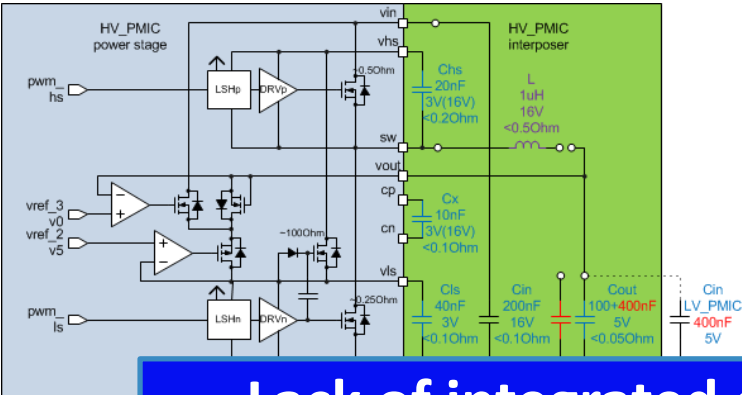


Automotive Specifications  
(ISO pulses, temperature, ...)

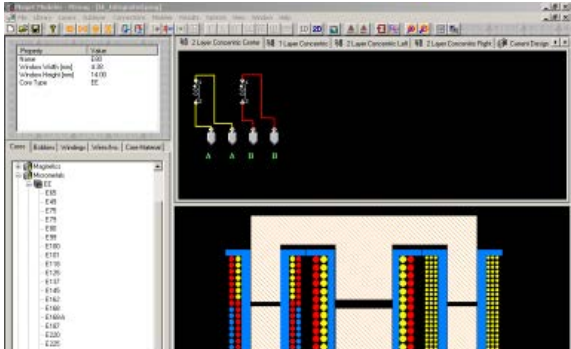


# State of the art CAD Tools

## Circuit Level Simulators



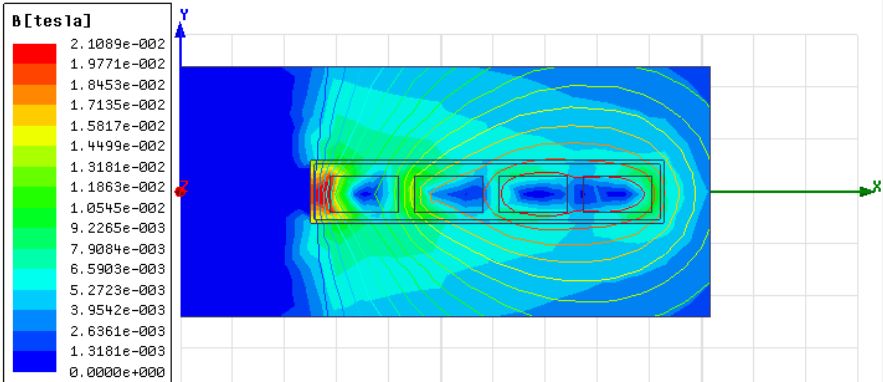
## Magnetic Component Optimization Tools



PEXprt-Pemag developed by UPM

**Lack of integrated design environment for Power Systems on Chip**

## Finite Element Analysis Tools



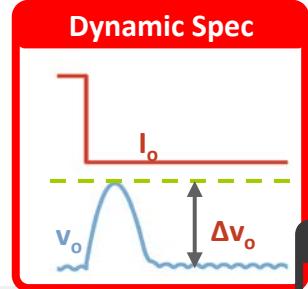
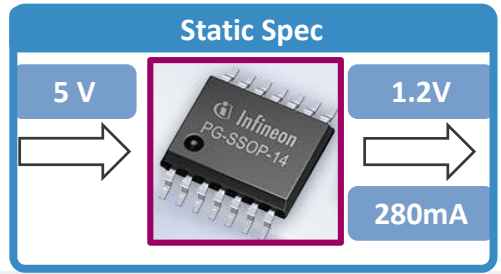
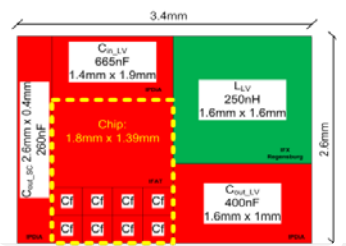
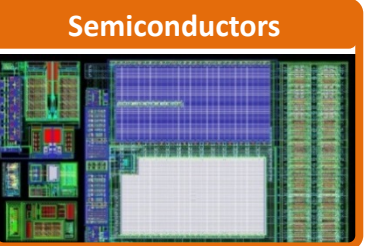
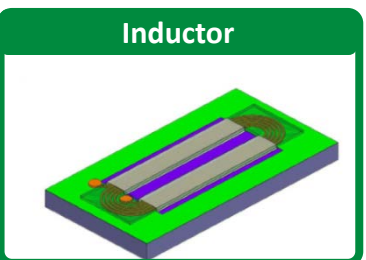
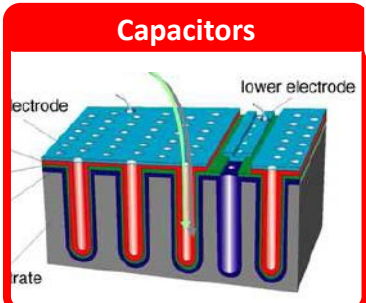
## General Purpose Math Tools



FWKSOC 2016 Madrid



# System Level Analysis and Optimization Tool



#### Capacitors

Cout	250	nF
Cin	250	nF
Precision	5	nF
Density	220	nF/mm2
Area	9	mm2
Vout pp	60	mV
Vin pp	60	mV
Rcin par	10	mOhm
Lcin par	100	pH
Rcout par	10	mOhm
Lcout par	100	pH

#### Total Passives Area

Area: 13 mm2

L	150	nH
Lmax	2000	nH
Precision	1	nH
LLpp max	500	mA
#Lamin	1	
Area	4	mm2
ILpp	12	mA
R parz	10	mOhm
L parz	100	pH

#### System Specification

tsw	20	MHz
tsw min	1	MHz
fsww max	30	MHz
Output		
Vout	1.2	V
Static ripple pp	5	%
Dynamic ripple pp	12	%
Input		
Vin	5	V
Static ripple pp	5	%
Dynamic ripple pp	5	%
Load		
Iout typical	280	mA
Iout maximal	500	mA
Iout minimal	50	mA
Target Efficiency		
eta @ Iout typical	90	%
eta @ Iout maximal	85	%
eta @ Iout minimal	75	%

#### Resistor Constraints

PM	60	deg
BWmin	0	MHz
BW	5	MHz
BWmax	5	MHz

#### Load Design Control

Single Buck VMC: CCM solution

Select Optimized Values:

Cin/Cout  Lout  fsw

wp  wn  Area

Load Design

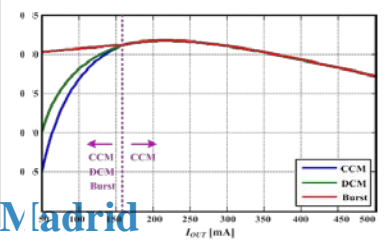
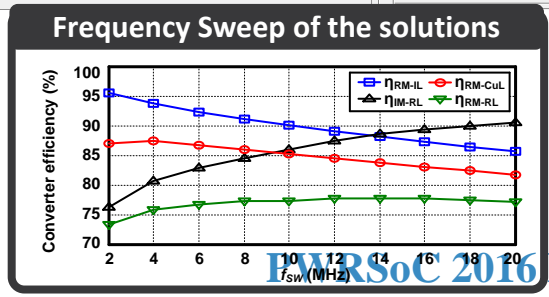
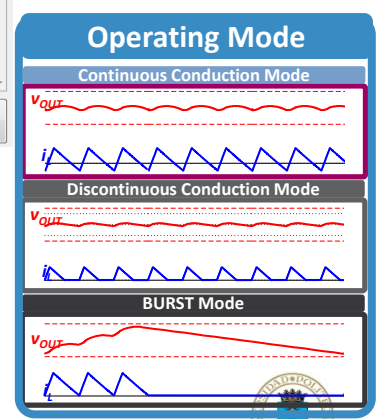
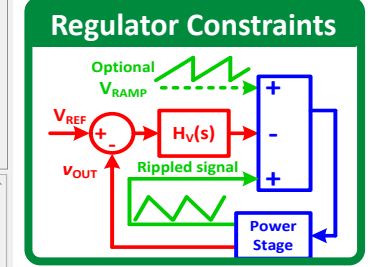
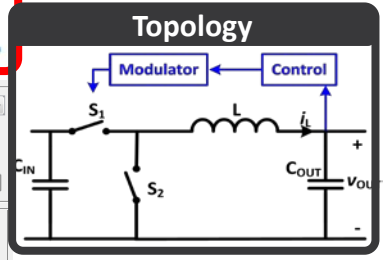
#### Wires

Wp	8000	um
Wp min	2000	um
Wp max	30000	um
Vgs	5.0	V
Ig max	80	mA
Ron	548.507	mOh

Wh	8000	um
Wh min	2000	um
Wh max	30000	um
Vgs	5.0	V
Ig max	80	mA
Ron	171.658	mOh

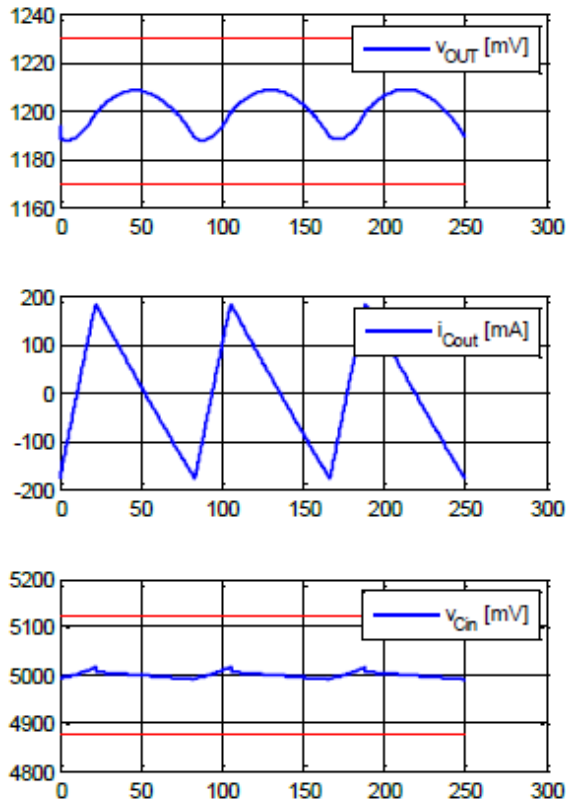
#### Load Steps

Dlout	50, 300	mA
Set. Time	2, 20000	ns
Input Voltage Steps		
DVin	250	mV
Set. Time	0	ns

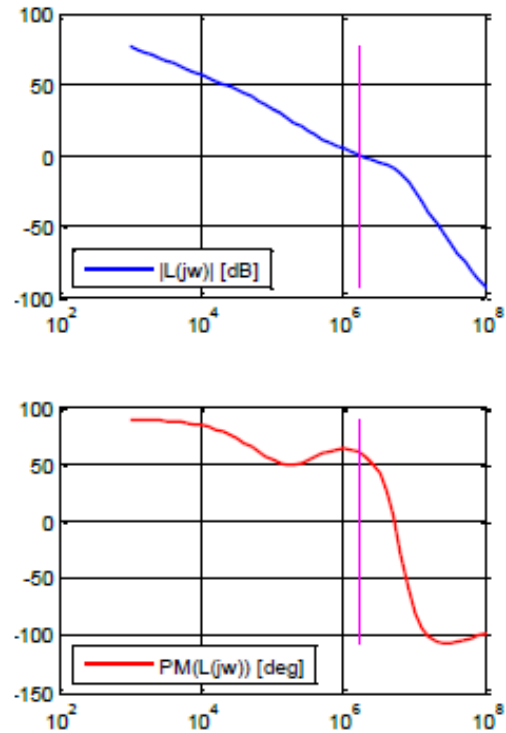


# Built-in Simulator

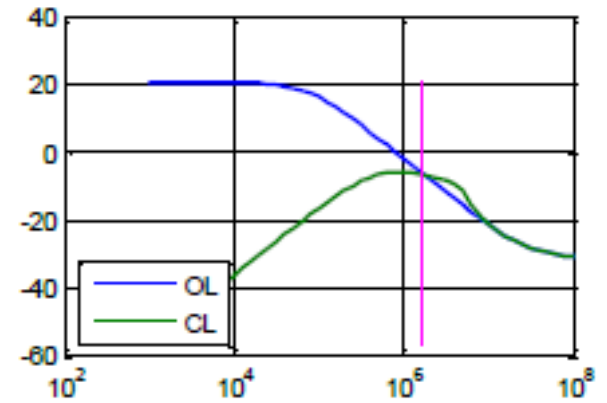
## Steady-state and transient



## Optimal Control Design



## System level performance



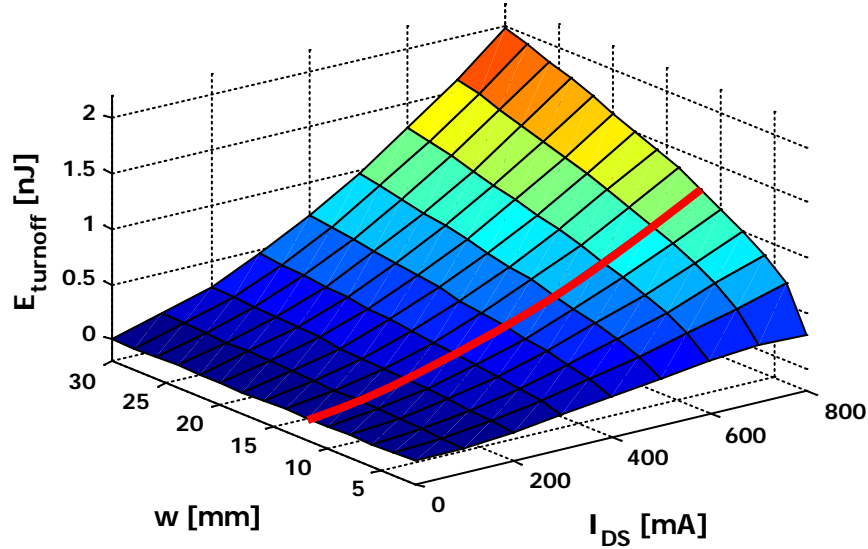
Open loop vs closed loop  $Z_{out}$

Loop Gain  
PWRSoC 2016 Madrid

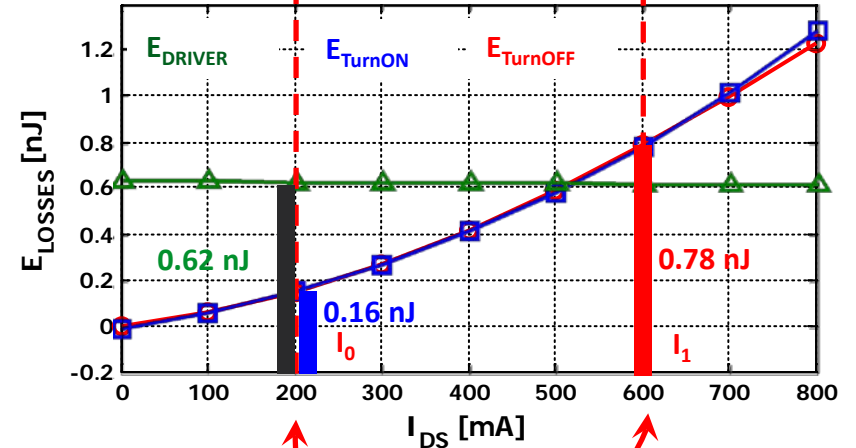


# Example: HI-Side (LV-DC-DC)

Turn-Off Transient Energy of PMOS



PMOS Switching Losses



$f_{\text{SW}} = 10 \text{ MHz}$

$P_{\text{TurnOFF}} = 7.86 \text{ mW}$

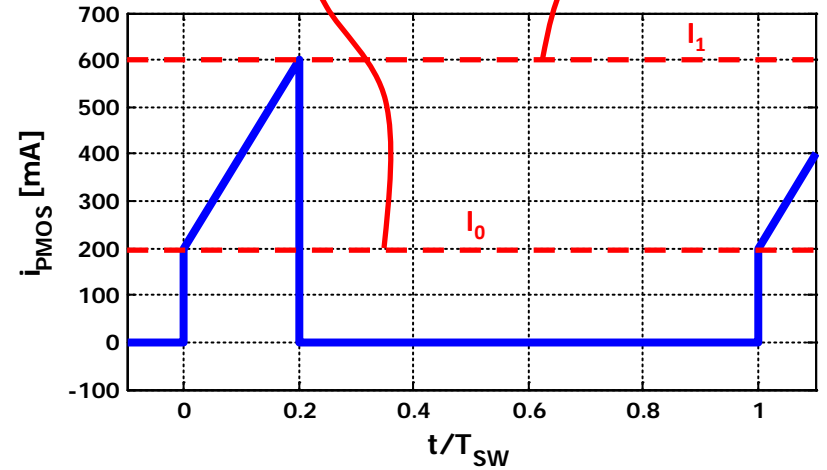
$P_{\text{TurnON}} = 1.6 \text{ mW}$

$P_{\text{Driver}} = 6.25 \text{ mW}$

$I_{\text{PMOSrms}} = 186.2 \text{ mA}$

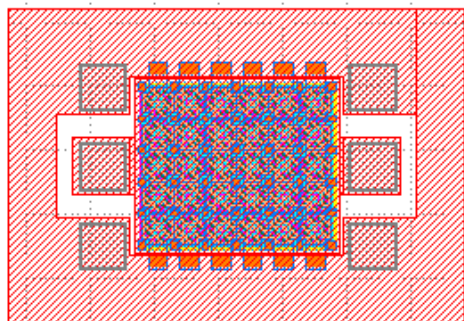
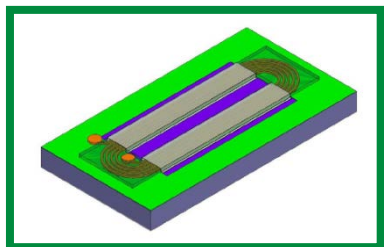
$R_{\text{PMOSon}} = 410 \text{ m}\Omega$

$P_{\text{COND}} = 14.2 \text{ mW}$

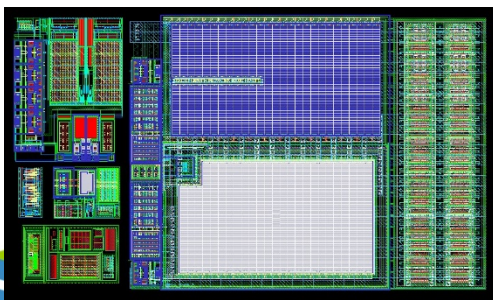




# LV DC-DC Optimization Results



hdcmos\_ref1\_12n8\_36cell



Geometry Parameters	Name	Value
Total area	$A_T$	3.2 mm <sup>2</sup>
Number of turns	N	4
Core thickness	$T_{core}$	5.15 μm
Core width	$W_{core}$	292.79 μm
Core height	$H_{core}$	75.3 μm
Core length	$L_{core}$	2993.84 μm
Copper width	$W_{cu}$	45.62 μm
Copper thickness	$T_{cu}$	35 μm
Vertical spacing	$H_{air}$	15 μm
Horizontal spacing	$W_{air}$	20 μm
Distance between cores	$D_{core}$	0.35 mm
Electrical Parameters		Value
L (analytical)		270 nH
L (FEA tool)		268 nH

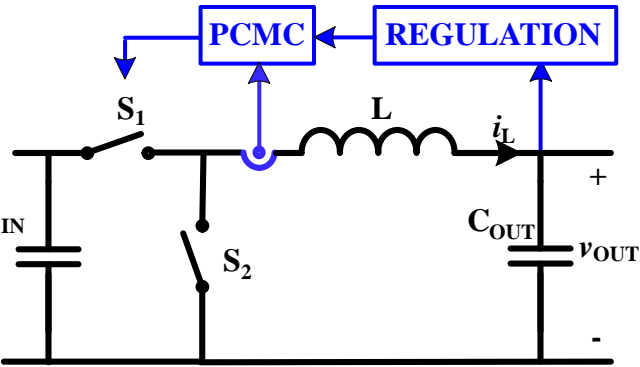
	Cap	ESR	area
$C_{IN}$	300 nF	17.5 mΩ	1.5 mm <sup>2</sup>
$C_{OUT}$	200 nF	11.7 mΩ	1 mm <sup>2</sup>

	Width	Length	$R_{ON}$ ( $V_{GS}=5V$ )	$R_{ON}$ ( $V_{GS}=3.3V$ )	$I_{Drive}$
PMOS	12 mm	650 nm	406.7 mΩ	530.9 mΩ	80 mA
NMOS	12.08 mm	560 nm	114.5 mΩ	142.4 mΩ	80 mA

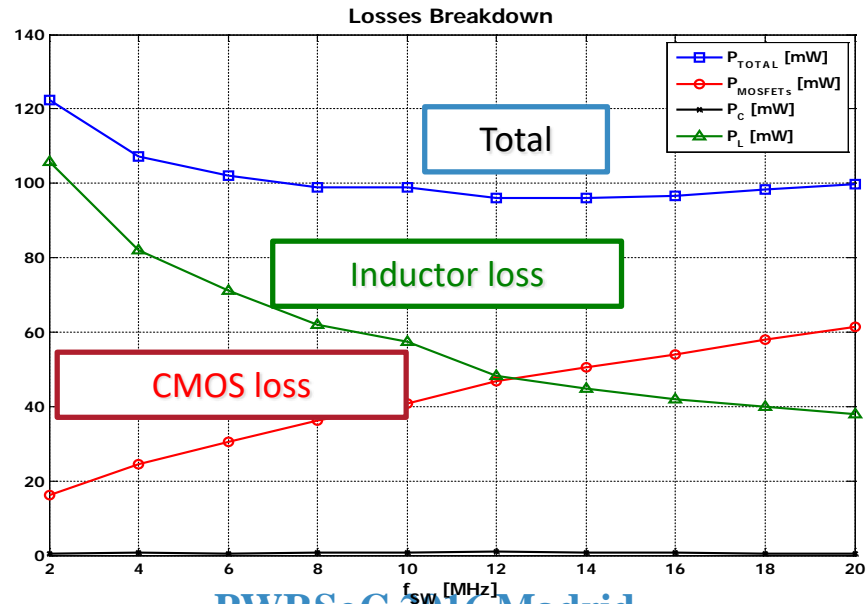
PWRSC 2016 Madrid



# LV DC-DC Optimization Results



$V_{IN}$		3.3 V	5 V
$f_{SW}$		11.86 MHz	11.75 MHz
$I_{OUT} = 280 \text{ mA}$	Efficiency	78.71%	75.53 %
	$P_{Total}$	90.88 mW	108.88 mW
$I_{OUT} = 500 \text{ mA}$	Efficiency	73.75%	73.59%
	$P_{Total}$	213.56 mW	215.29 mW

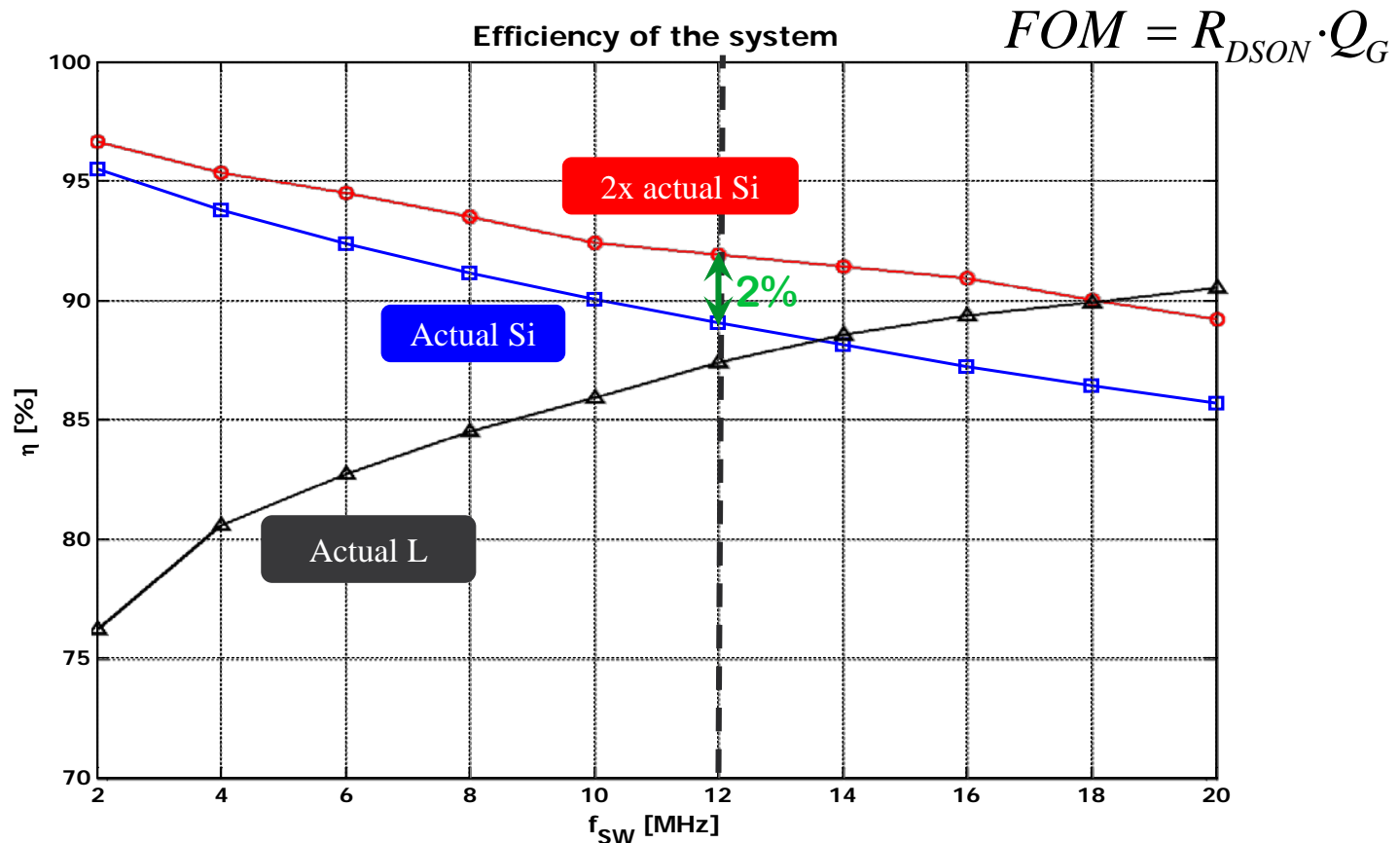


PWRSoC 2016 Madrid





# Evaluation of the Impact of technology



Improvement of Si technology has stronger influence **at high  $f_{sw}$**

A technology two times better, provides 2 % improvement in the efficiency (@  $f_{sw} > 12\text{MHz}$ )

$$\eta_{(\text{tech}, 12\text{MHz})} = 89\%$$

$$\eta_{(2\text{xtech}, 12\text{MHz})} = 91\%$$

40% switching losses and 60% conduction losses

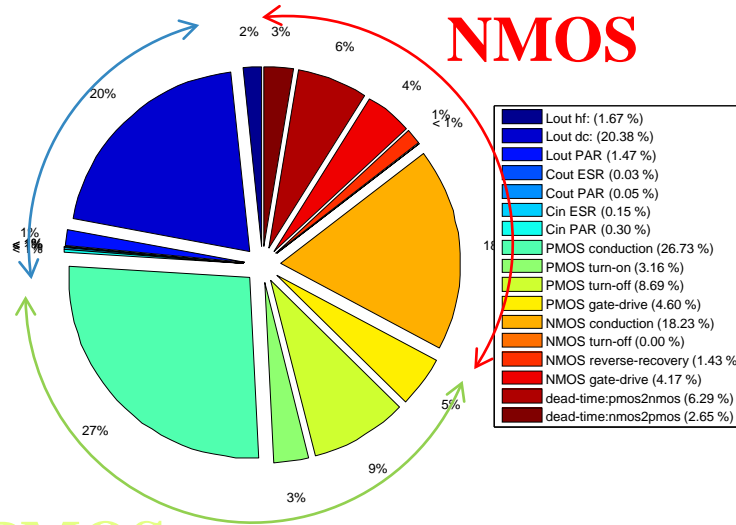


# System Level Optimization electrical performance

Efficiency: 77.21%

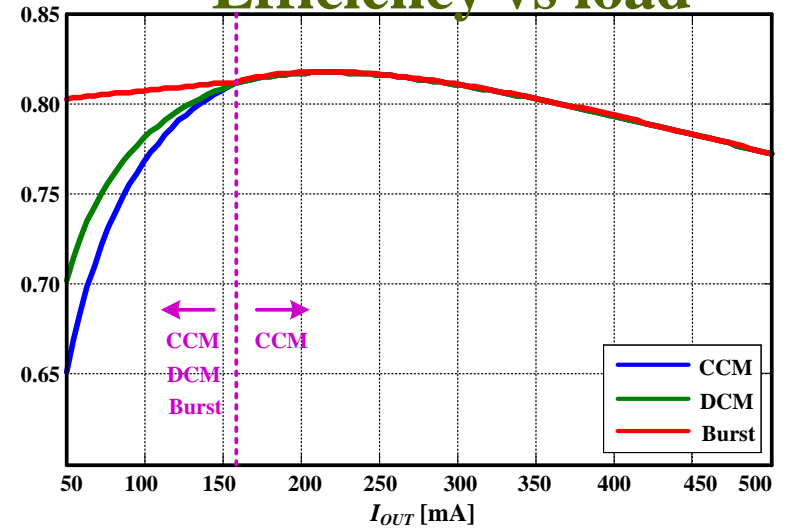
## Losses breakdown

**NMOS**

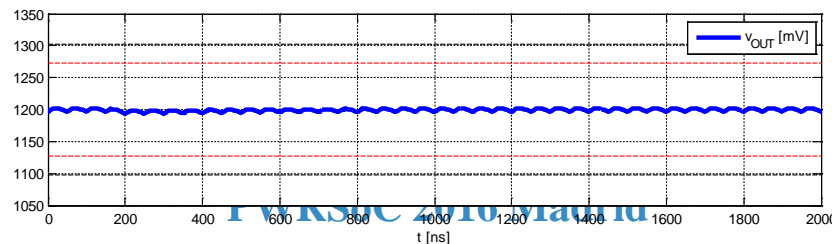
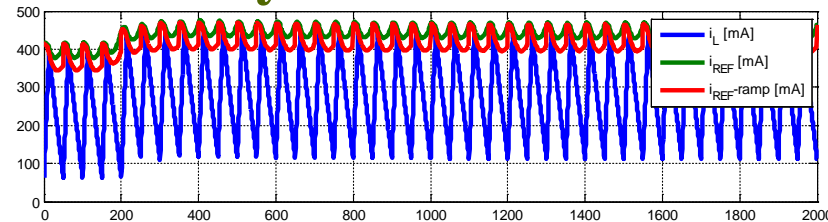


**PMOS**

## Efficiency vs load

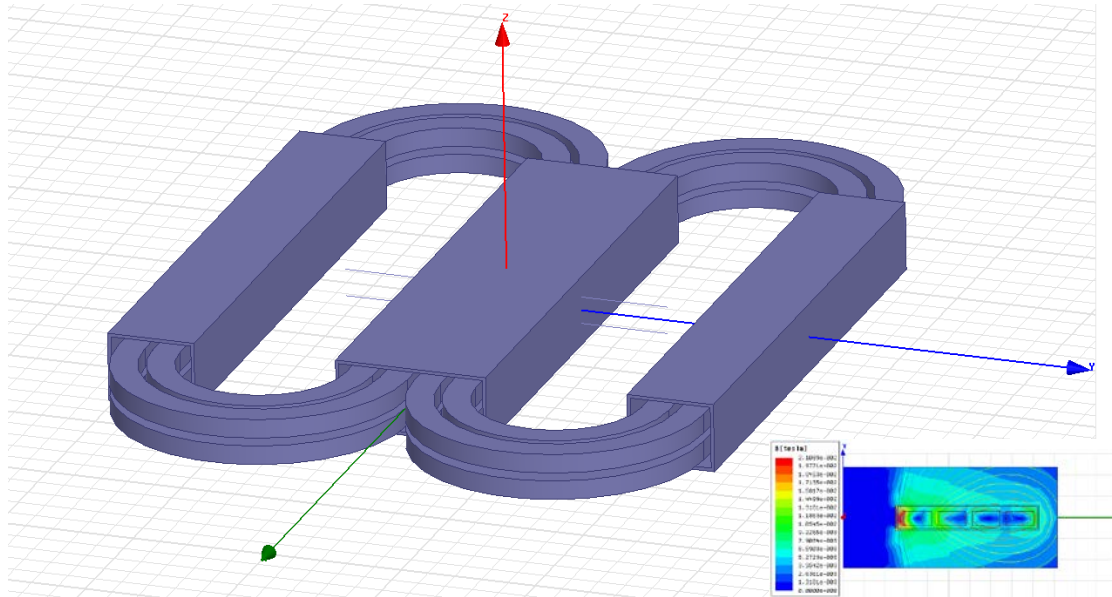


## Dynamic behavior



# FEA Modeling/Validation of Coupled Inductors

## Option A: Maxwell 3D simulations



### PARAMETERS

Geometry Parameters	Name	Value
Total area	$A_T$	xx mm <sup>2</sup>
Number of turns	N	4
Core thickness	$T_{core}$	6 $\mu\text{m}$
Core width (Inductor)	$W_{coreI}$	157 $\mu\text{m}$
Core width (Transformer)	$W_{coreT}$	187 $\mu\text{m}$
Core height	$H_{core}$	127 $\mu\text{m}$
Core length	$L_{core}$	1.00 mm
Copper width	$W_{cu}$	50 $\mu\text{m}$
Copper thickness	$T_{cu}$	35 $\mu\text{m}$
Vertical spacing	$H_{air}$	15 $\mu\text{m}$
Horizontal spacing	$W_{air}$	15 $\mu\text{m}$
Distance between cores	$D_{core}$	264 $\mu\text{m}$

Material parameters	Value
Resistivity core	45 $\mu\Omega \cdot \text{cm}$
Relative Permeability core	280
Resistivity copper	1.71 $\mu\Omega \cdot \text{cm}$

$L_{\text{Analytical (simple)}}$   $L_{\text{Analytical (complex)}}$

$$L_M = 21.14 \text{ nH}$$

$$L_K = 31.34 \text{ nH}$$

nH

$$L_M = 21.82 \text{ nH}$$

$$L_K = 41.03 \text{ nH}$$

$L_{\text{FEA}}$

$$L_M = 22.18 \text{ nH}$$

$$L_K = 43.47 \text{ nH}$$

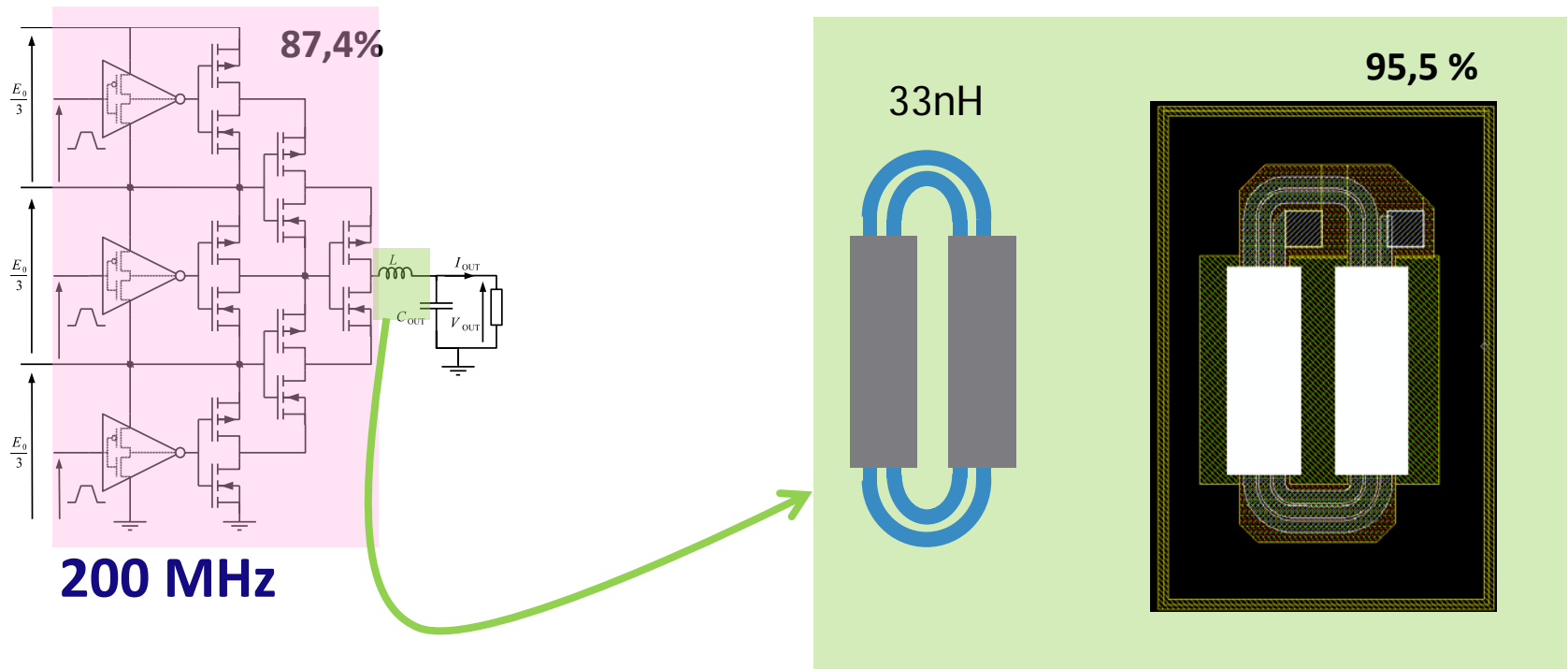
PWRSoC 2016 Madrid



# 200 MHz Single Inductor (33nH)

## Simulation Results

PowerSWIPE ITVs	L (nH)	Core Thickness	Core Length	Copper width	Copper Thickness	DCR (Ohm)	Device Footprint
ITV 2A	33	1.2 $\mu\text{m}$	1.22 mm	72.2 $\mu\text{m}$	35 $\mu\text{m}$	0.084	2 mm <sup>2</sup>



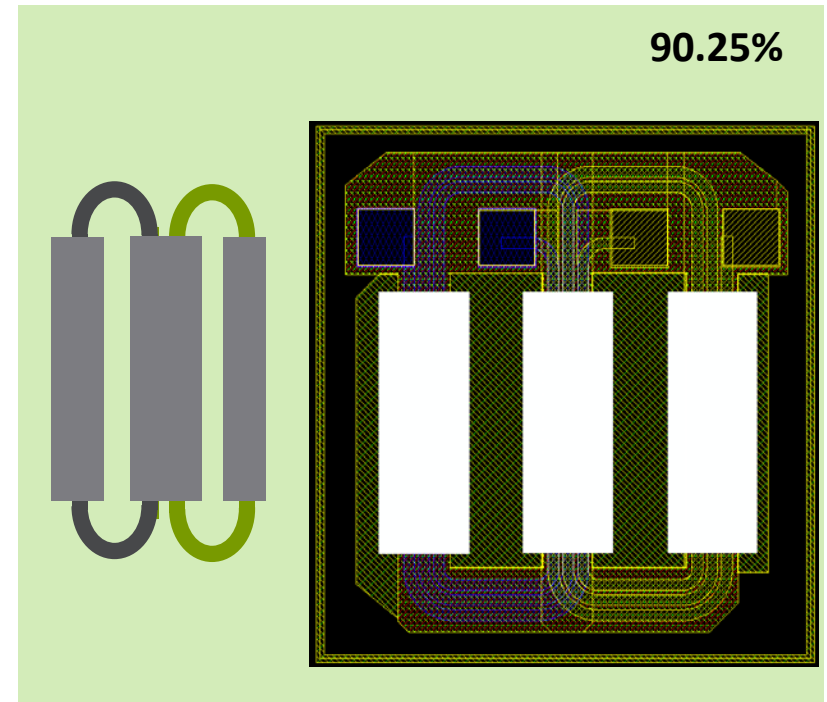
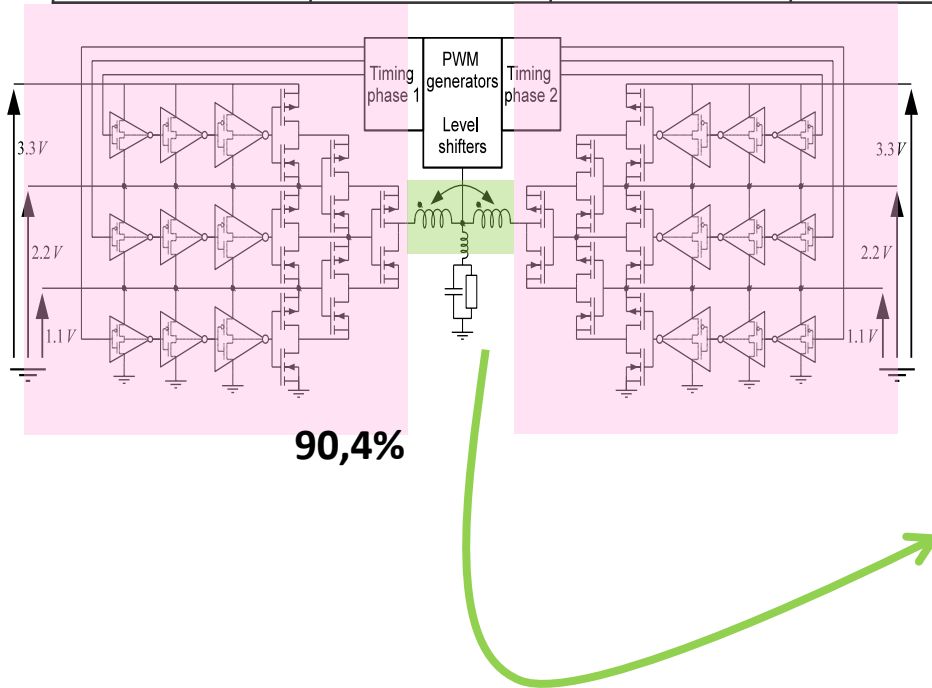
**Total converter efficiency 83%**  
PWRSoC 2016 Madrid



# 100 MHz Coupled Inductors (47nH)

## Simulation Results

PowerSWIPE ITVs	L (nH)	Core Thickness	Core Length	Copper width	Copper Thickness	DCR (Ohm)	Device Footprint
ITV 2B	47 Coupled (k=0.4)	1.6 $\mu\text{m}$	1.78 mm	50.62	15 $\mu\text{m}$	0.3425	2 mm <sup>2</sup>

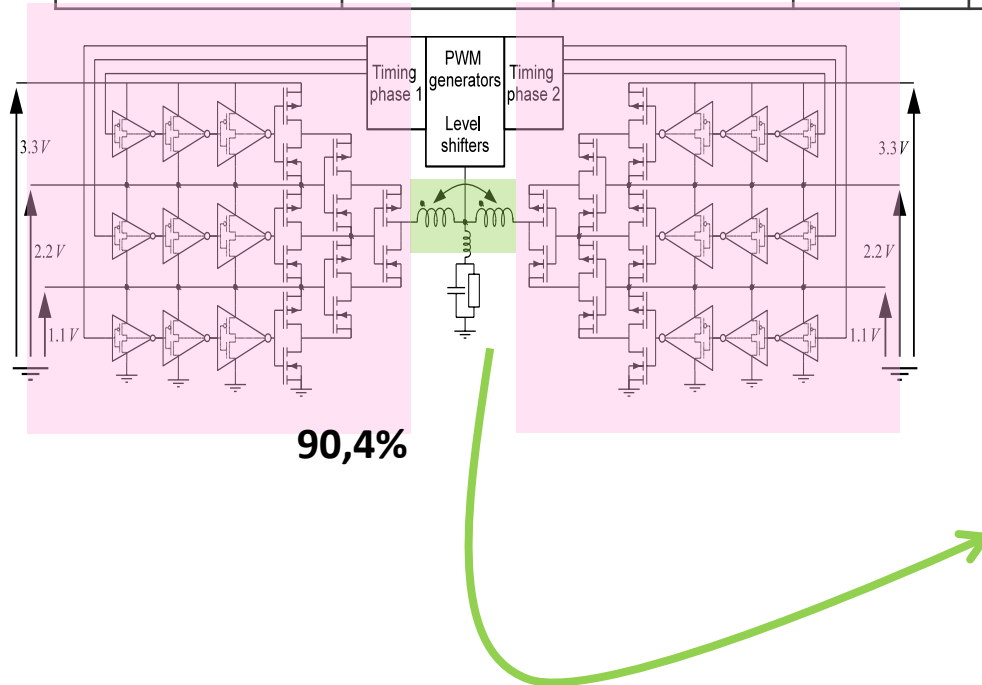


**Total converter efficiency 81%**  
PWRSoC 2016 Madrid

# 100 MHz Coupled Inductors (35nH) + Single Inductor (20nH)

## Simulation Results

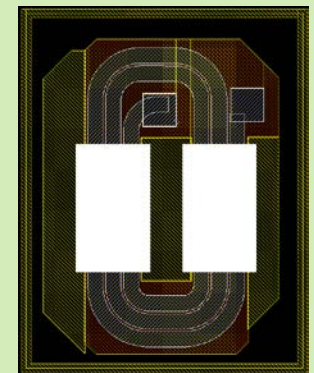
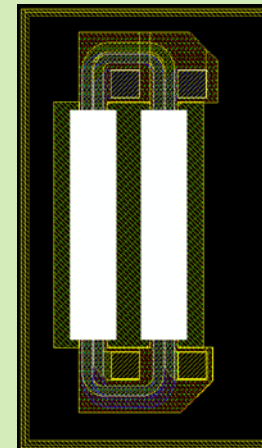
PowerSWIPE ITVs	L (nH)	Core Thickness	Core Length	Copper width	Copper Thickness	DCR (Ohm)	Device Footprint
ITV 2C	35 nH Coupled k=0.8	1.6 $\mu\text{m}$	1.83 mm	75.71 $\mu\text{m}$	15 $\mu\text{m}$	0.155	2 mm <sup>2</sup>
	20 nH	1.6 $\mu\text{m}$	0.78 mm	97 $\mu\text{m}$	35 $\mu\text{m}$	0.053	2 mm <sup>2</sup>



85.6%

90.25%

94.8%



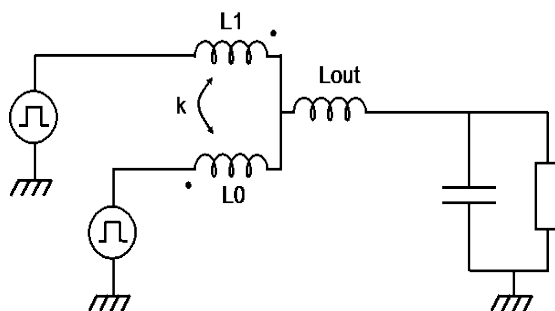
**Total converter efficiency 77%**

PWRSoC 2016 Madrid





# Coupled Inductor Comparison

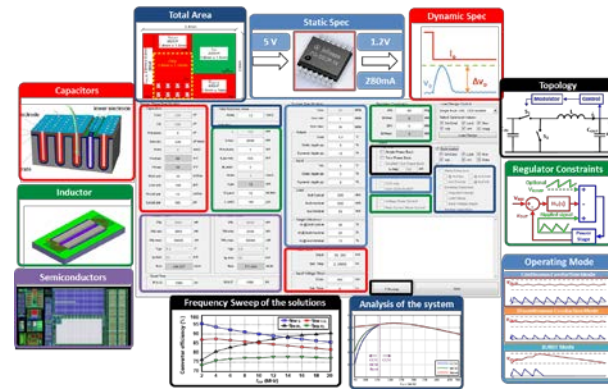
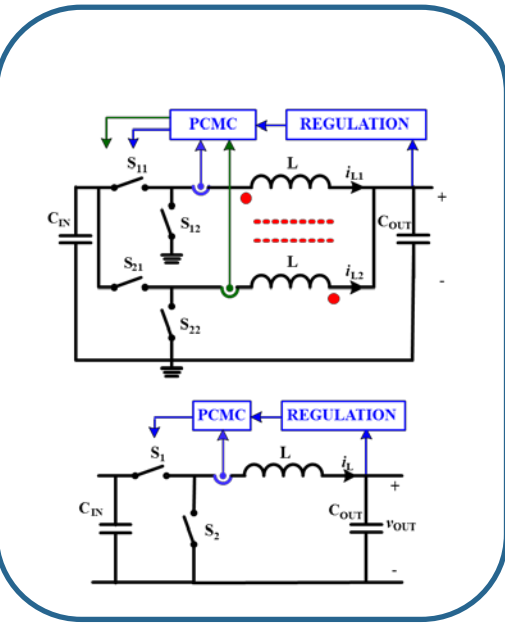


## Comparison single-phase and two-phase dc/dc converter

	Inductor design	Freq. (MHz)	L (nH)	Coupling factor	Efficiency (magnetics)	Efficiency (IC)	Total efficiency
ITV2a	Single phase	200	33	--	95,5 %	87,4%	83%
ITV2b	Coupled	100	45	~0.4	90%	90,4%	81%
ITV2c	Coupled +Lout	100	35+21	>0.8	85.6% (90.25%·94.8%)	90,4%	77%

# Conclusions

## 1<sup>st</sup> Integrated multi-domain optimization tool for PwrSoC

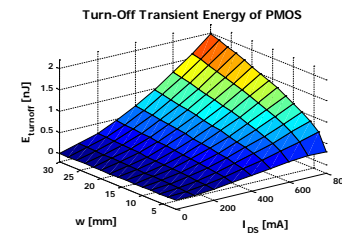
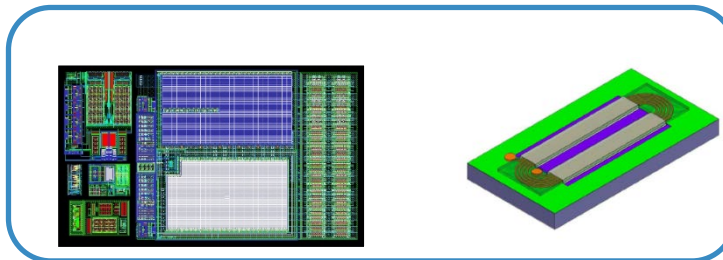


## Physical Design

Parameter	Name	Value
Total area	$A_T$	3.2 mm <sup>2</sup>
Number of turns	N	4
Core thickness	$T_{core}$	5.15 $\mu$ m
Core width	$W_{core}$	292.79 $\mu$ m
Core height	$H_{core}$	75.3 $\mu$ m
Core length	$L_{core}$	2993.84 $\mu$ m
Copper width	$W_{Cu}$	45.62 $\mu$ m
Copper thickness	$T_{Cu}$	35 $\mu$ m
Vertical spacing	$H_{air}$	15 $\mu$ m
Horizontal spacing	$W_{air}$	20 $\mu$ m
Distance between cores	$D_{core}$	0.35 mm
Electrical Parameters		Value
L (analytical)		270 nH
L (FEA tool)		268 nH

Minimum LC requirements

## Technologies



PWRSoC 2016 Madrid

Accurate Models



Thank you!

