CEI UPM | Centro de Electrónica Industrial

CAD Tool for the optimization of Power Converters on Chip

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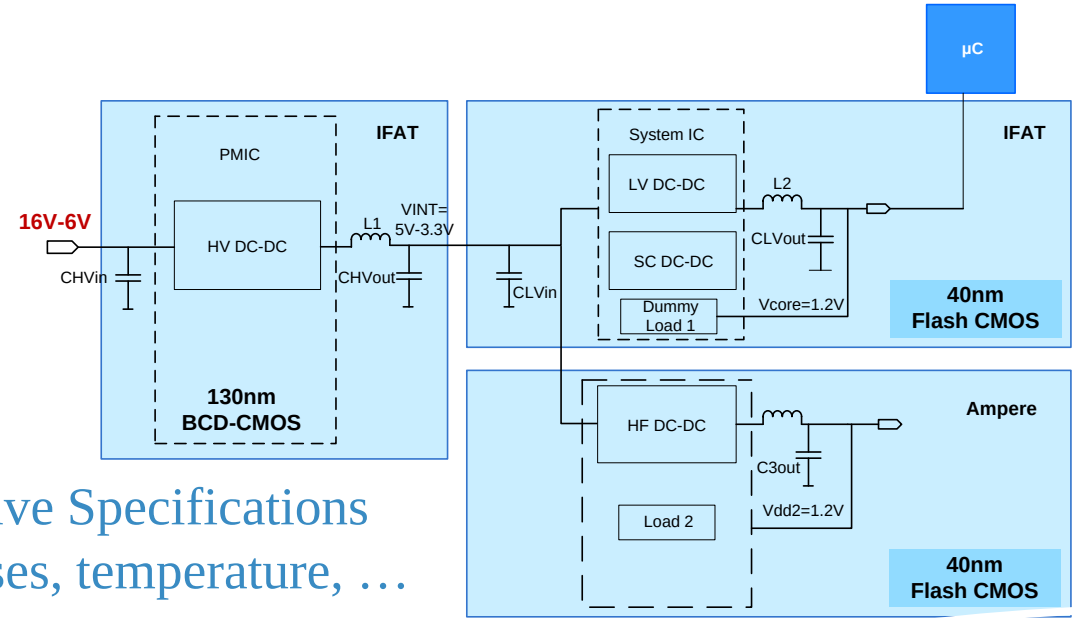
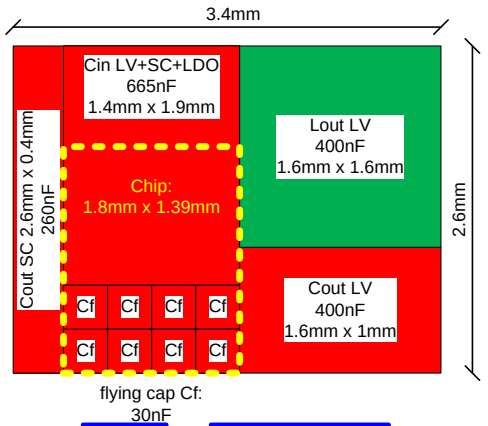
PWRSoC 2016 Madrid

UNIVERSIDAD POLITÉCNICA DE MADRID

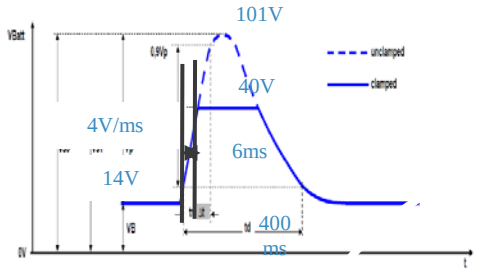
POLITÉCNICA

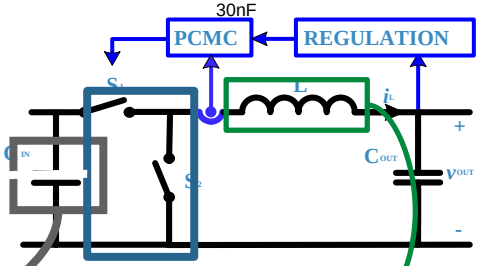
The need of an integrated multi-domain tool

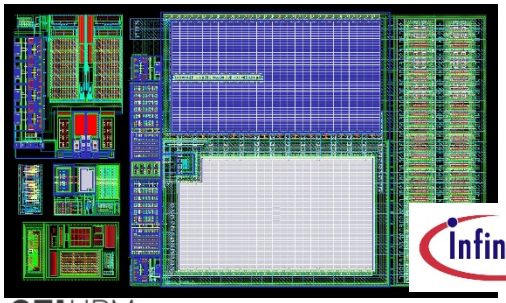


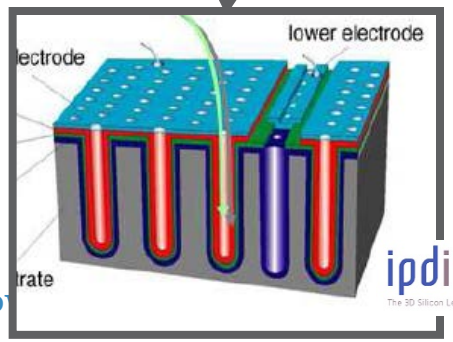


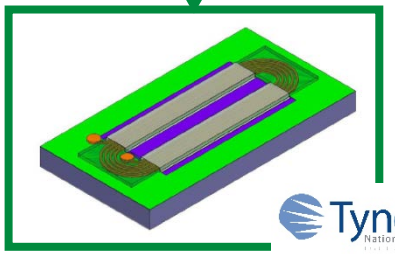
Automotive Specifications
(ISO pulses, temperature, …





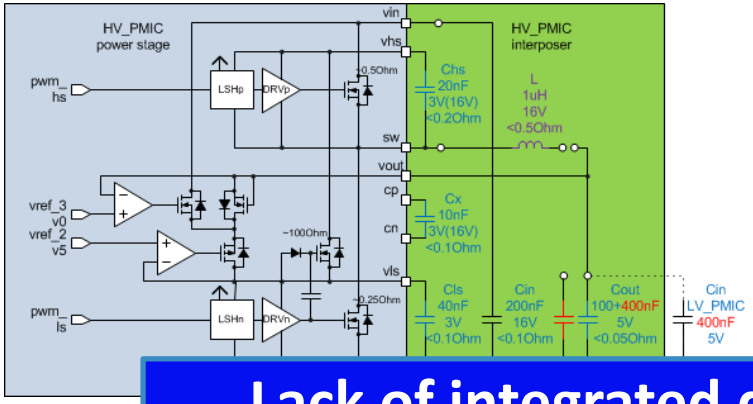




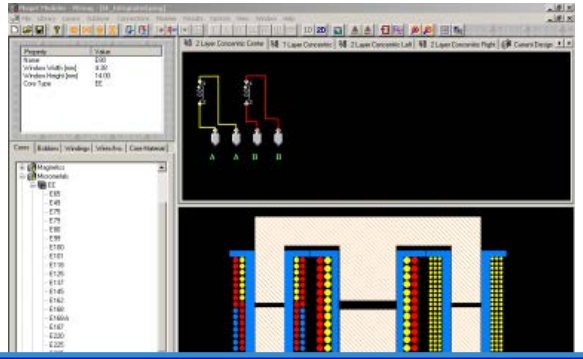


State of the art CAD Tools

Circuit Level Simulators



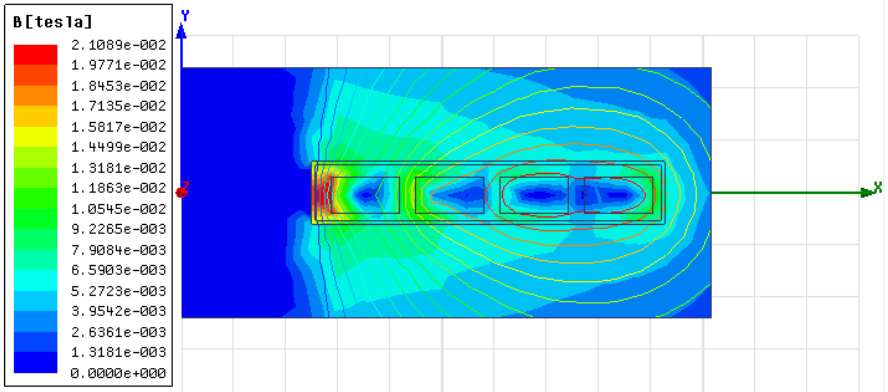
Magnetic Component Optimization Tools



PEXprt-Pemag developed by UPM

Lack of integrated design environment for Power Systems on Chip

Finite Element Analysis Tools

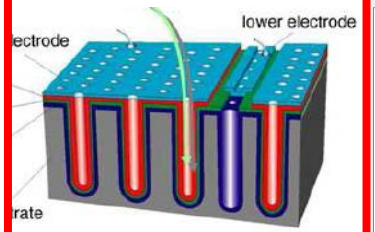


General Purpose Math Tools

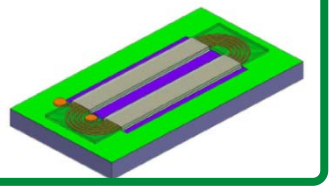
MathWorks

System Level Analysis and Optimization Tool

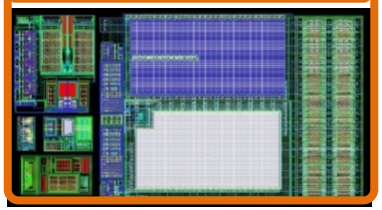
Capacitors

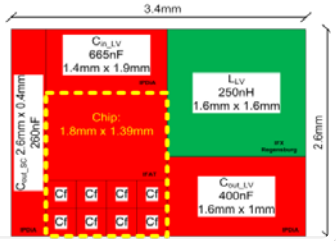


Inductor

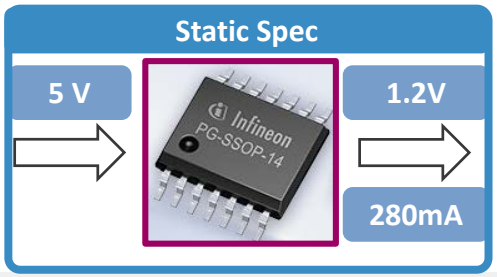


Semiconductors

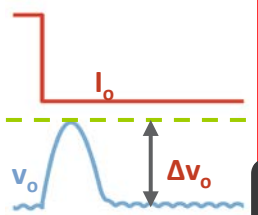




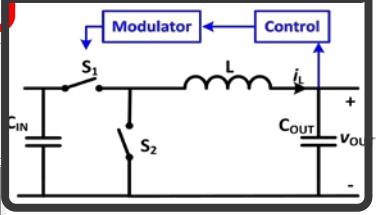
Static Spec



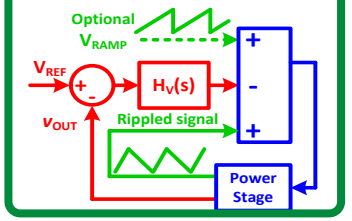
Dynamic Spec



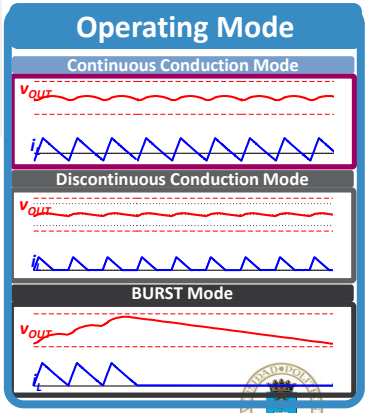
Topology



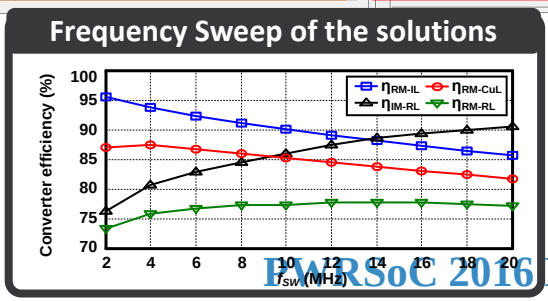
Regulator Constraints

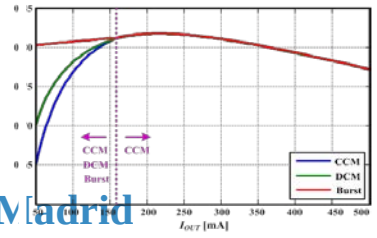


Operating Mode



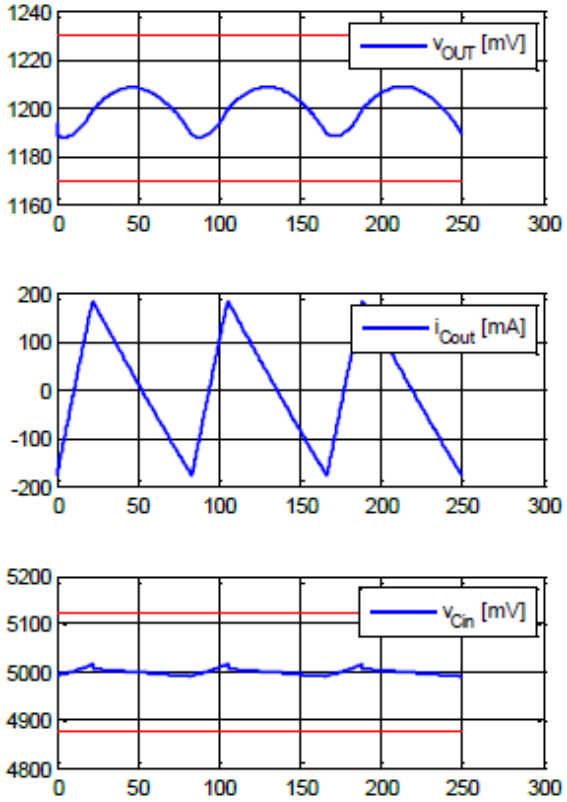
Frequency Sweep of the solutions





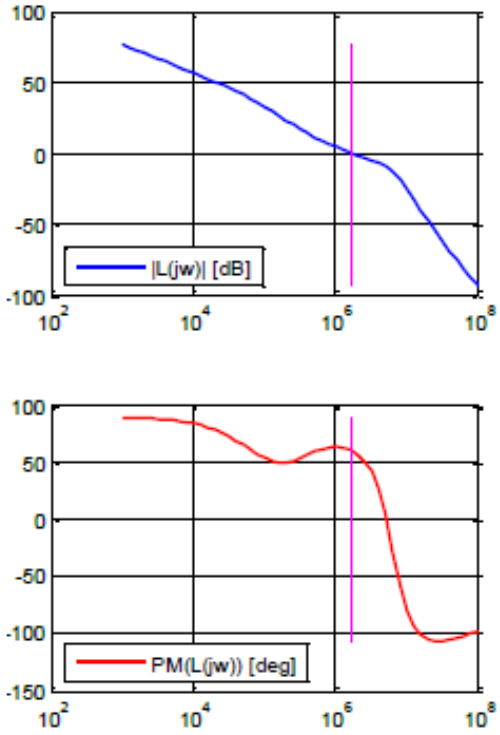
Built-in Simulator

Steady-state and transient



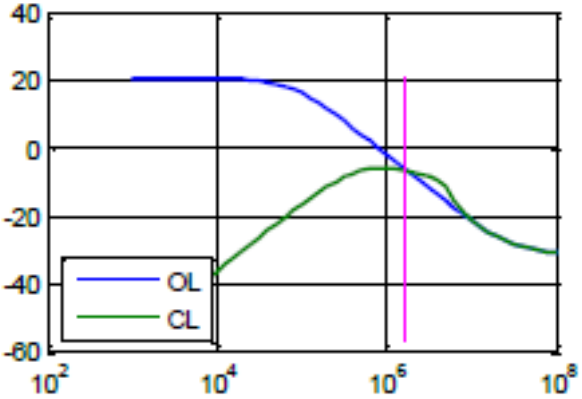
Time domain waveforms

Optimal Control Design



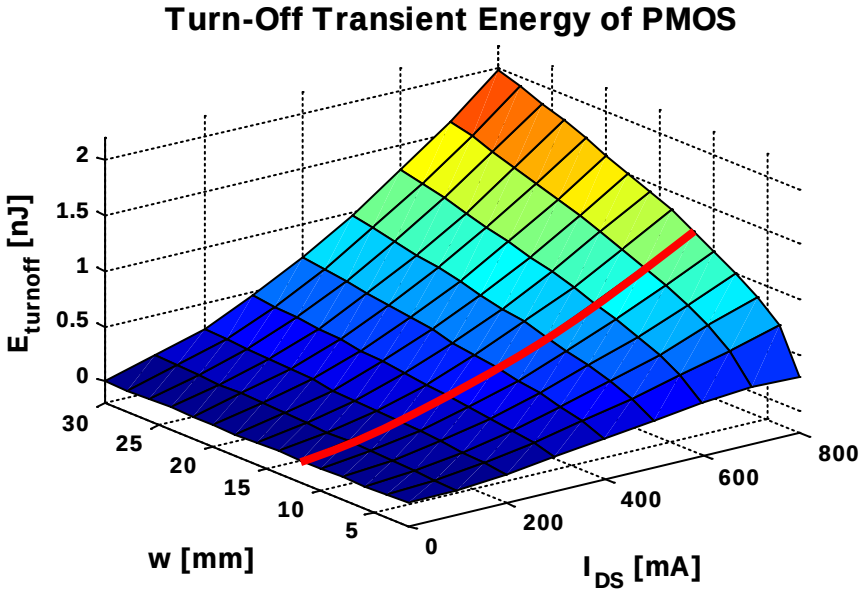
Loop Gain

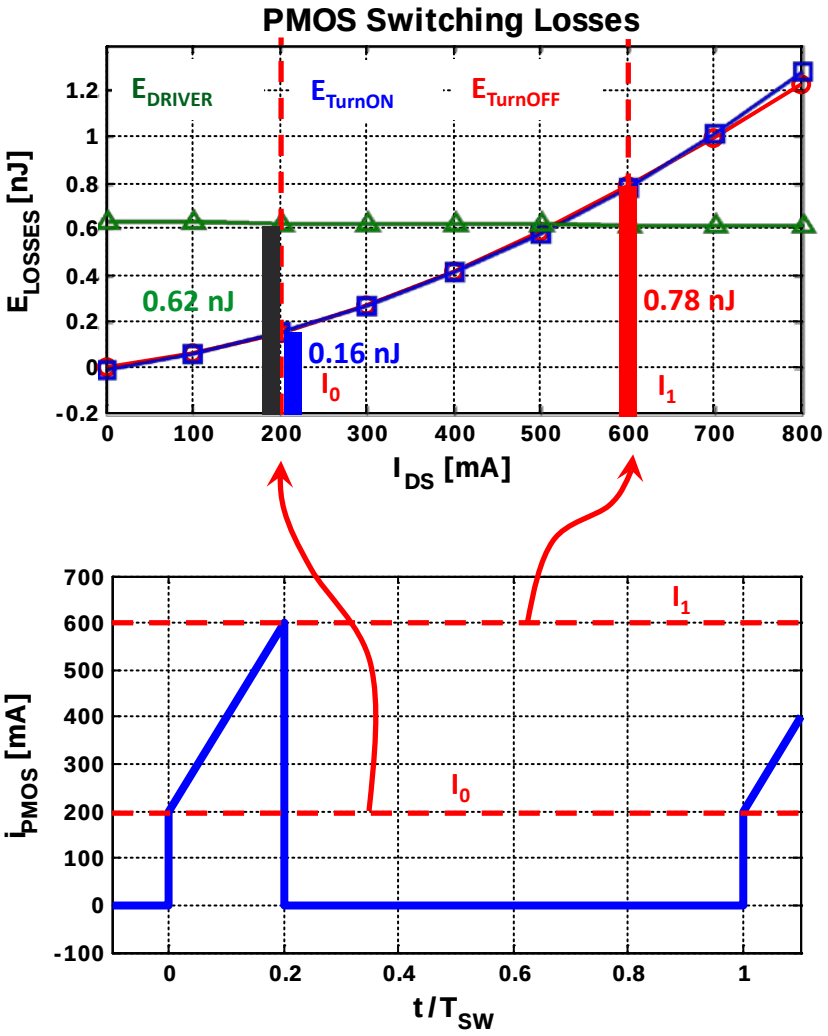
System level performance



Open loop vs closed loop Zout

Example: HI-Side (LV-DC-DC)





f_{SW} = 10 MHz

$P_{TurnOFF}$ = 7.86 mW

P_{TurnON} = 1.6 mW

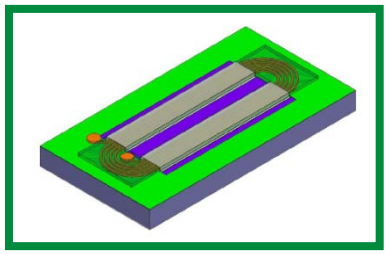
P_{Driver} = 6.25 mW

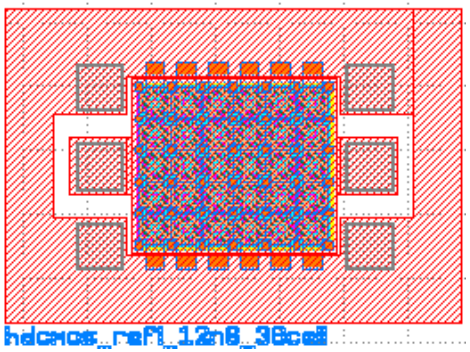
$I_{PMOSrms}$ = 186.2 mA

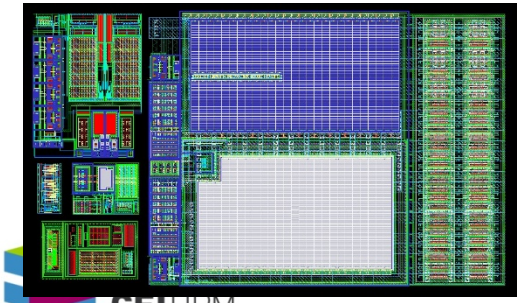
R_{PMOSon} = 410 mΩ

P_{COND} = 14.2 mW

LV DC-DC Optimization Results





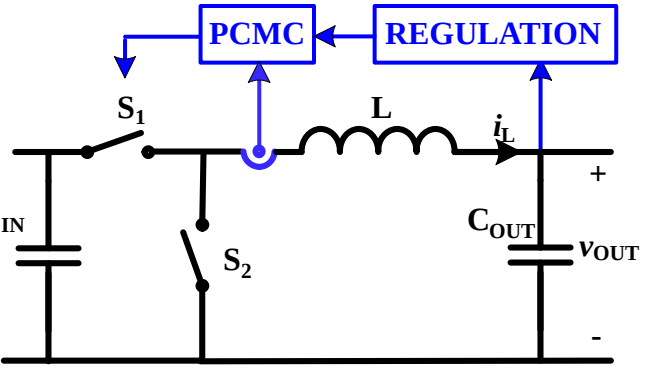


Geometry Parameters	Name	Value
Total area	A_T	3.2 mm^2
Number of turns	N	4
Core thickness	T_{core}	5.15 µm
Core width	W_{core}	292.79 µm
Core height	H_{core}	75.3 µm
Core length	L_{core}	2993.84 µm
Copper width	W_{cu}	45.62 µm
Copper thickness	T_{cu}	35 µm
Vertical spacing	H_{air}	15 µm
Horizontal spacing	W_{air}	20 µm
Distance between cores	D_{core}	0.35 mm
Electrical Parameters		**Value**
L (analytical)		270 nH
L (FEA tool)		268 nH

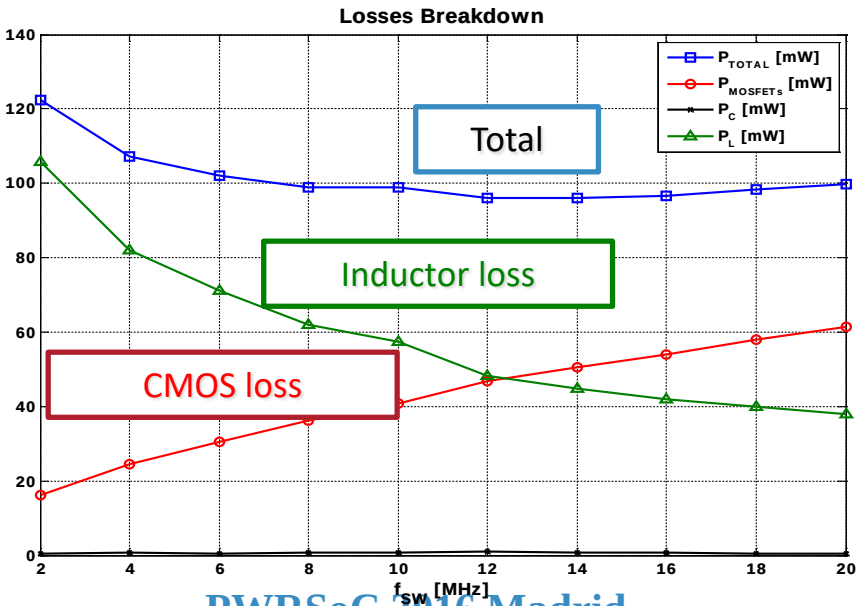
	Cap	ESR	area
C_{IN}	300 nF	17.5 mΩ	1.5 mm^2
C_{OUT}	200 nF	11.7 mΩ	1 mm^2

	Width	Length	R_{ON} (V_{GS}=5V)	R_{ON} (V_{GS}=3.3V)	I_{Drive}
PMOS	12 mm	650 nm	406.7 mΩ	530.9 mΩ	80 mA
NMOS	12.08 mm	560 nm	114.5 mΩ	142.4 mΩ	80 mA

LV DC-DC Optimization Results

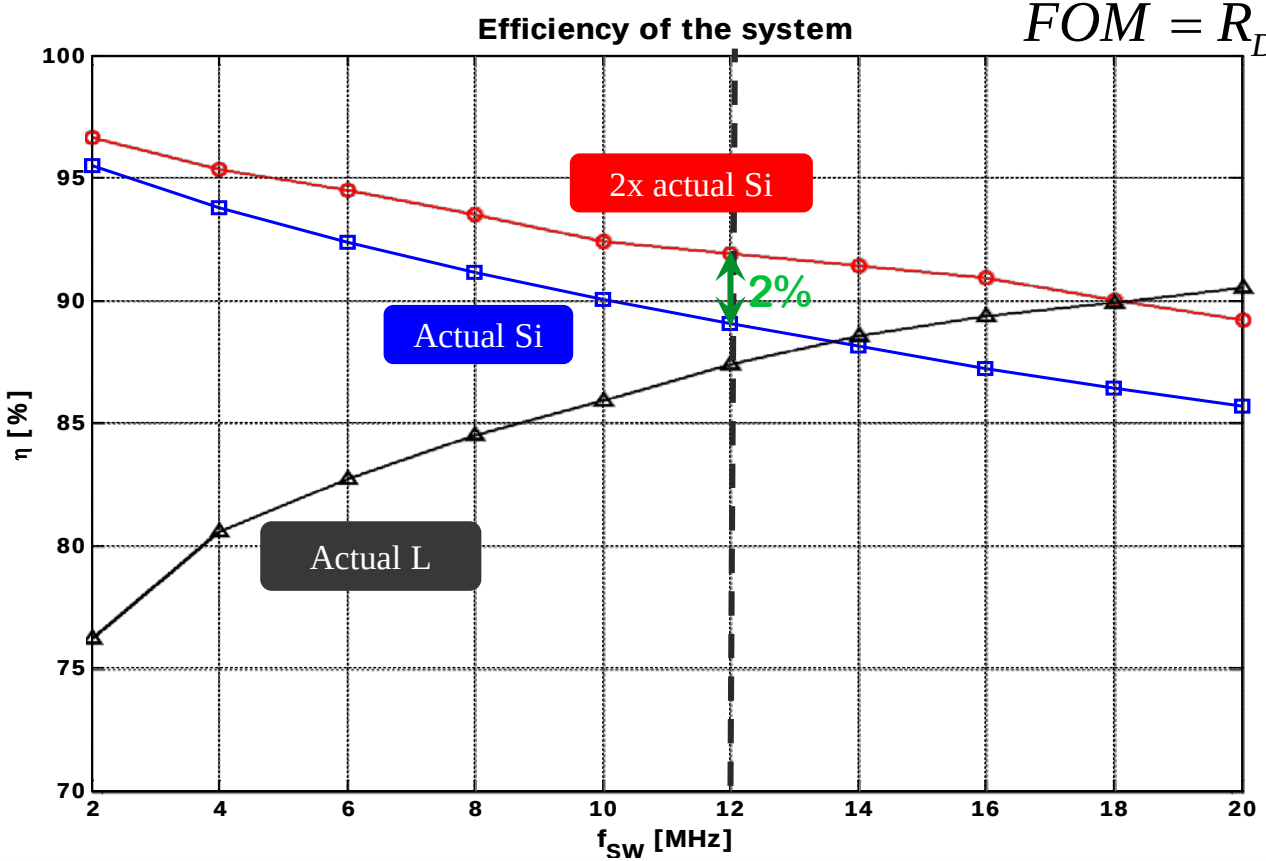


V_{IN}		3.3 V	5 V
f_{SW}		11.86 MHz	11.75 MHz
I_{OUT} = 280 mA	Efficiency	78.71%	75.53 %
	P_{Total}	90.88 mW	108.88 mW
I_{OUT} = 500 mA	Efficiency	73.75%	73.59%
	P_{Total}	213.56 mW	215.29 mW



Evaluation of the Impact of technology

$$FOM = R_{DSON} \cdot Q_G$$



Improvement of Si technology has stronger influence **at high f_{sw}**

A technology two times better, provides 2 % improvement in the efficiency (@ f_{sw} >12MHz)

$\eta_{(tech,\ 12MHz)} = 89\%$

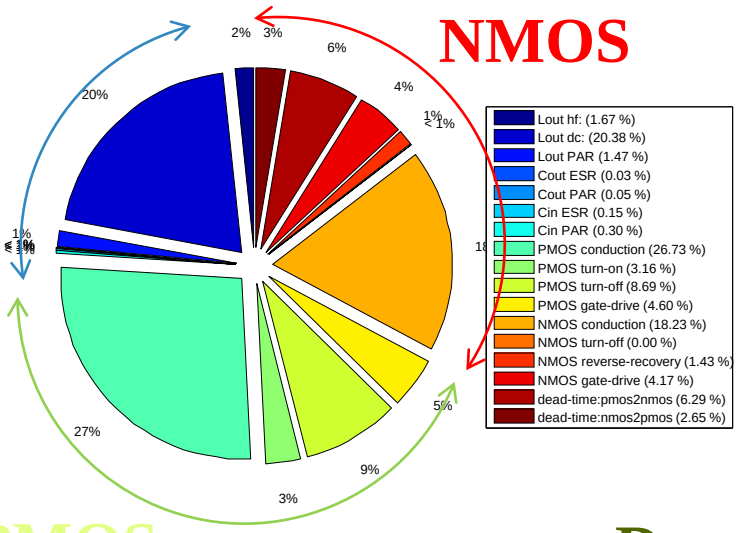
$\eta_{(2xtech,\ 12MHz)} = 91\%$

40% switching losses and 60% conduction losses

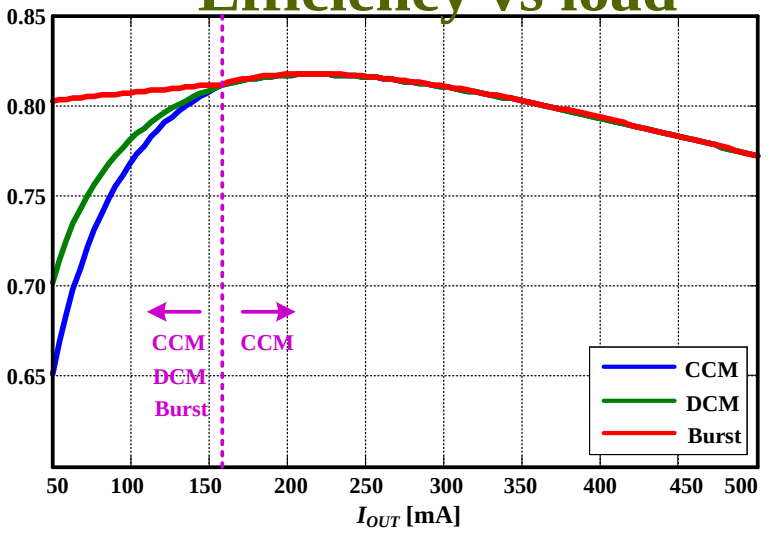
System Level Optimization electrical performance

Efficiency: 77.21%

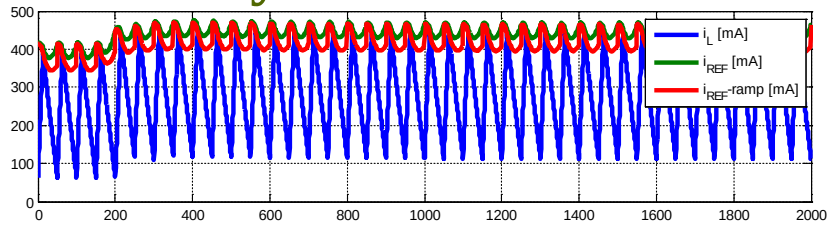
Losses breakdown

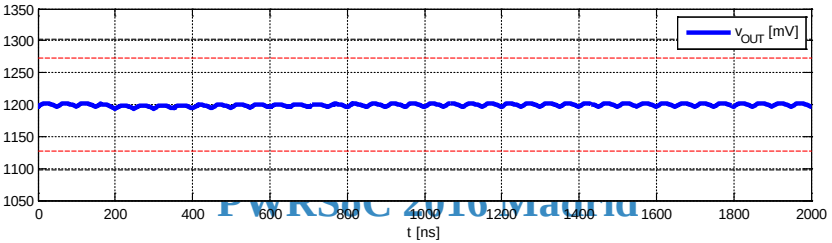


Efficiency vs load



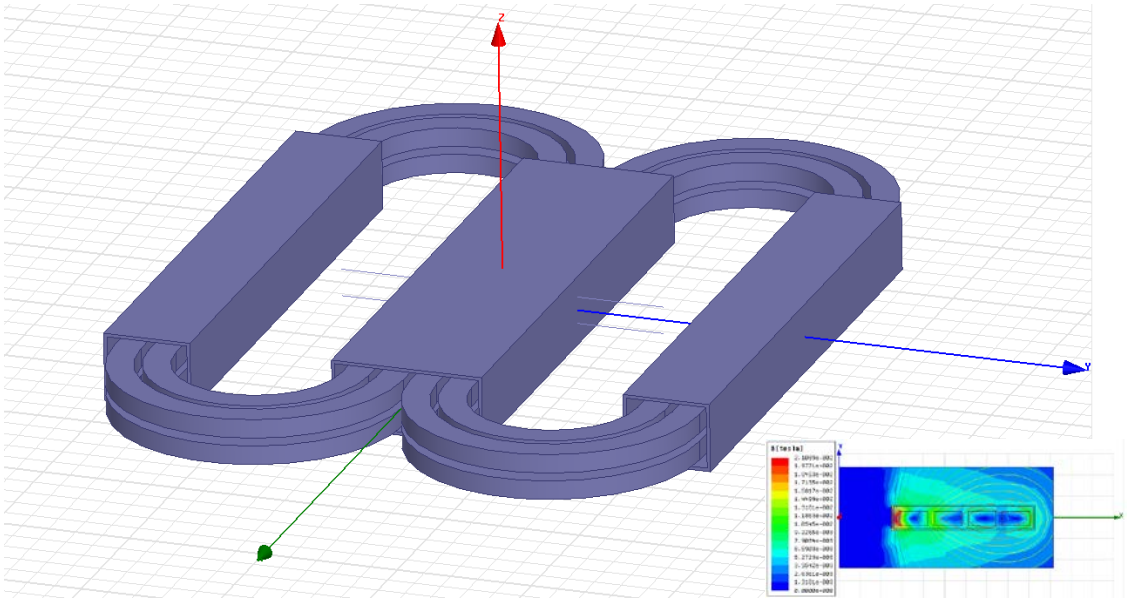
Dynamic behavior





FEA Modeling/Validation of Coupled Inductors

Option A: Maxwell 3D simulations



PARAMETERS

Geometry Parameters	Name	Value
Total area	A_T	xx mm^2
Number of turns	N	4
Core thickness	T_{core}	6 µm
Core width (Inductor)	W_{corel}	157 µm
Core width (Transformer)	W_{corel}	187 µm
Core height	H_{core}	127 µm
Core length	L_{core}	1.00 mm
Copper width	W_{cu}	50 µm
Copper thickness	T_{cu}	35 µm
Vertical spacing	H_{air}	15 µm
Horizontal spacing	W_{air}	15 µm
Distance between cores	D_{core}	264 µm

Material parameters	Value
Resistivity core	45 µΩ*cm
Relative Permeability core	280
Resistivity copper	1.71 µΩ*cm

$L_{Analytical\ (simple)}$
$L_M = 21.14$ nH
$L_K = 31.34$ nH

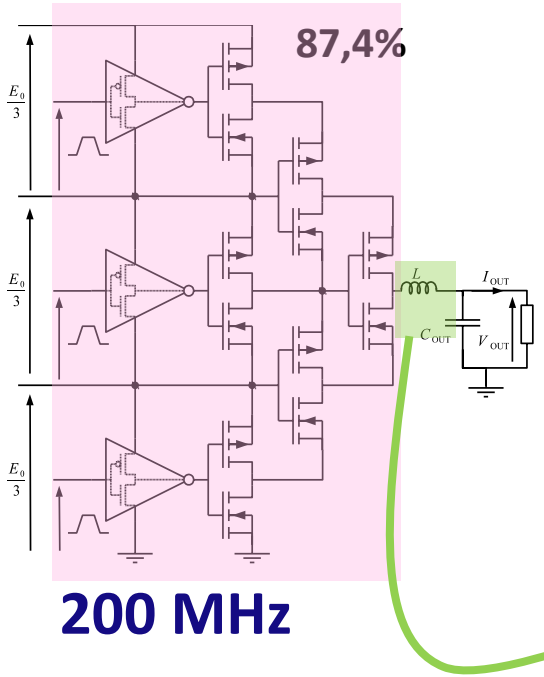
$L_{Analytical\ (complex)}$
$L_M = 21.82$ nH
$L_K = 41.03$ nH

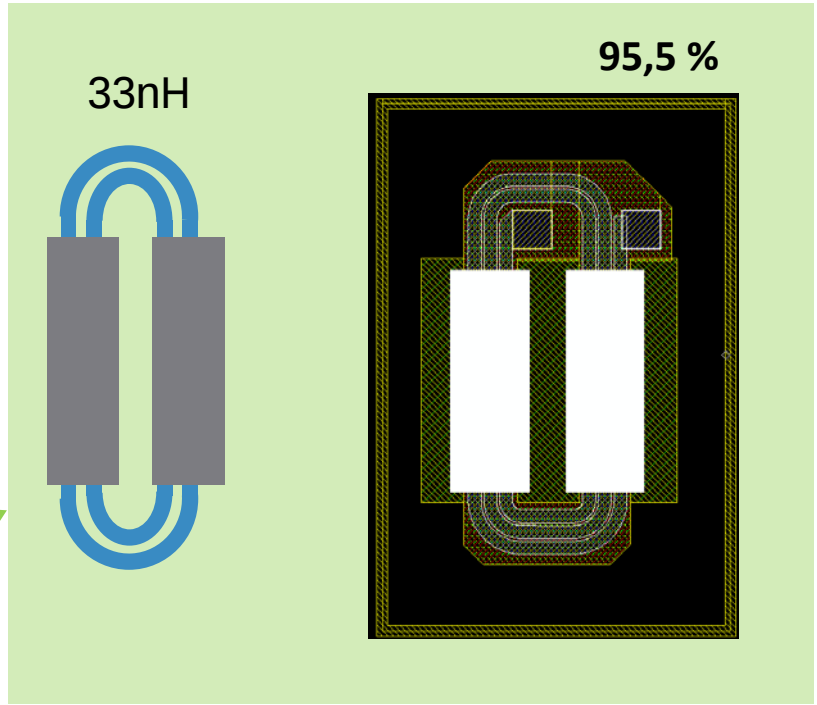
L_{FEA}
$L_M = 22.18$ nH
$L_K = 43.47$ nH

200 MHz Single Inductor (33nH)

Simulation Results

PowerSWIPE ITVs	L (nH)	Core Thickness	Core Length	Copper width	Copper Thickness	DCR (Ohm)	Device Footprint
ITV 2A	33	1.2 µm	1.22 mm	72.2 µm	35 µm	0.084	2 mm^2





Total converter efficiency 83 %

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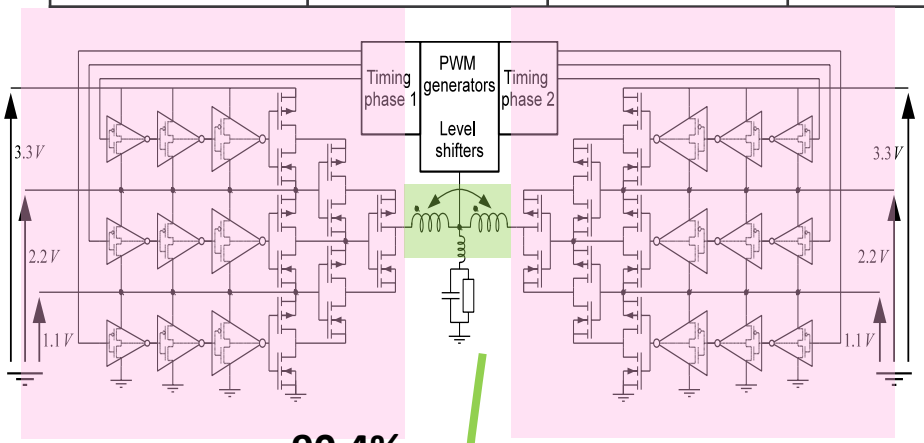
100 MHz Coupled Inductors (47nH)

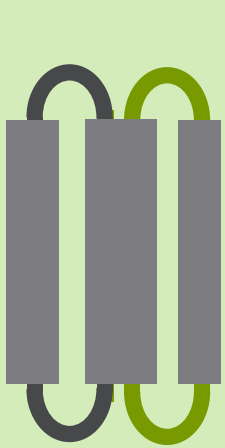
Simulation Results

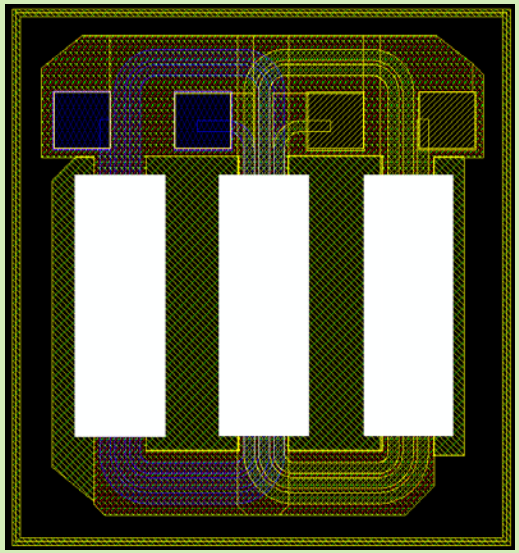
PowerSWIPE ITVs	L (nH)	Core Thickness	Core Length	Copper width	Copper Thickness	DCR (Ohm)	Device Footprint
ITV 2B	47 Coupled (k=0.4)	1.6 µm	1.78 mm	50.62	15 µm	0.3425	2 mm^2



90,4%

90.25%





Total converter efficiency 81 %

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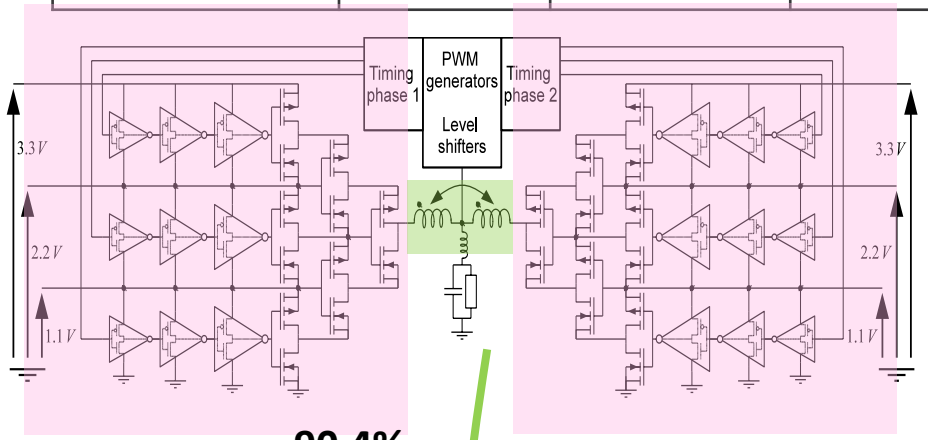
100 MHz Coupled Inductors (35nH) + Single Inductor (20nH)

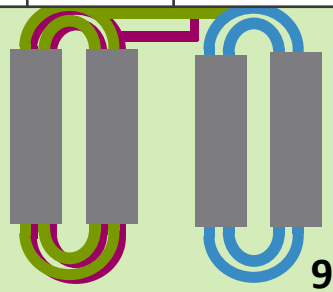
Simulation Results

PowerSWIPE ITVs	L (nH)	Core Thickness	Core Length	Copper width	Copper Thickness	DCR (Ohm)	Device Footprint
ITV 2C	35 nH Coupled k=0.8	1.6 µm	1.83 mm	75.71 µm	15 µm	0.155	2 mm²
	20 nH	1.6 µm	0.78 mm	97 µm	35 µm	0.053	2 mm²



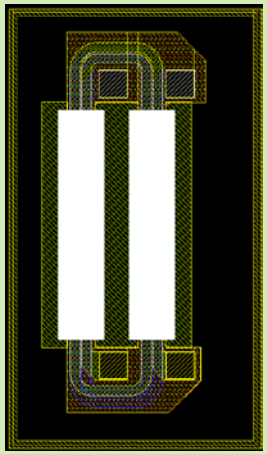
90,4%

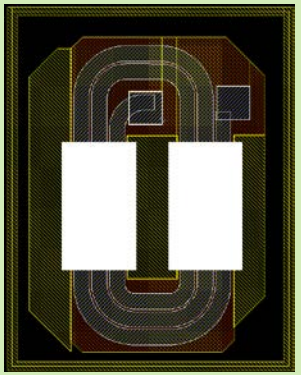
85.6%



90.25%

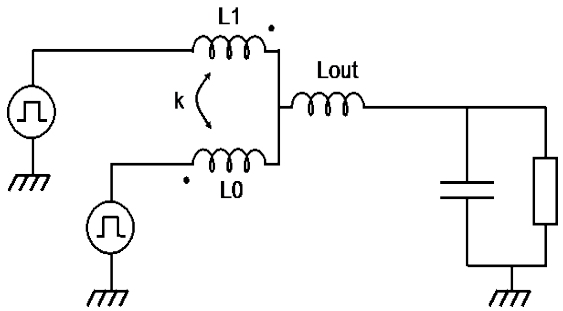
94.8%





Total converter efficiency 77 %

Coupled Inductor Comparison

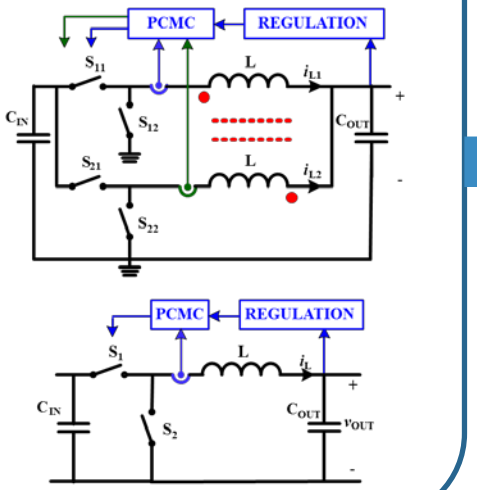


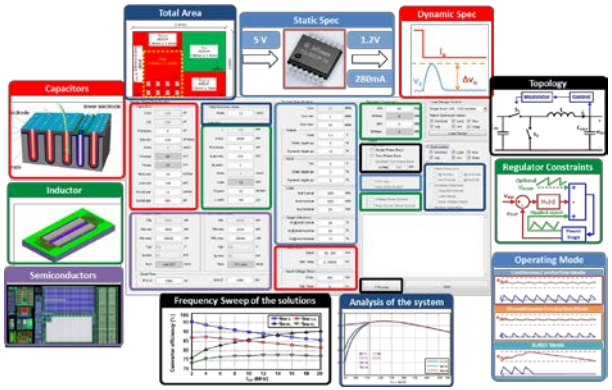
Comparison single-phase and two-phase dc/dc converter

	Inductor design	Freq. (MHz)	L (nH)	Coupling factor	Efficiency (magnetics)	Efficiency (IC)	Total efficiency
ITV2a	Single phase	200	33	--	**95,5 %**	**87,4%**	**83%**
ITV2b	Coupled	100	45	~0.4	**90%**	**90,4%**	**81%**
ITV2c	Coupled +Lout	100	35+21	>0.8	85.6% **(90.25%·94.8%)**	**90,4%**	**77%**

Conclusions

1st Integrated multi-domain optimization tool for PwrSoC

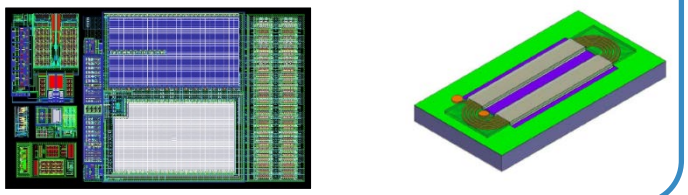




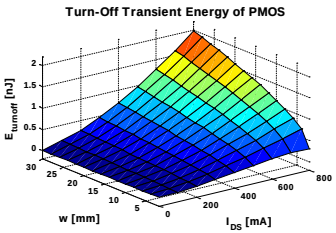
Physical Design

Parameter	Name	Value
Total area	A_T	3.2 mm²
Number of turns	N	4
Core thickness	T_{core}	5.15 µm
Core width	W_{core}	292.79 µm
Core height	H_{core}	75.3 µm
Core length	L_{core}	2993.84 µm
Copper width	W_{cu}	45.62 µm
Copper thickness	T_{cu}	35 µm
Vertical spacing	H_{air}	15 µm
Horizontal spacing	W_{air}	20 µm
Distance between cores	D_{core}	0.35 mm
Electrical Parameters		**Value**
L (analytical)		270 nH
L (FEA tool)		268 nH

Technologies



Minimim LC requirements



Accurate Models

PWRSoC 2016 Madrid


Thank you!