



CEI UPM

Centro de
Electrónica
Industrial

V¹ Control for fast transient response in Power Converters on Chip

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UNIVERSIDAD POLITÉCNICA DE MADRID

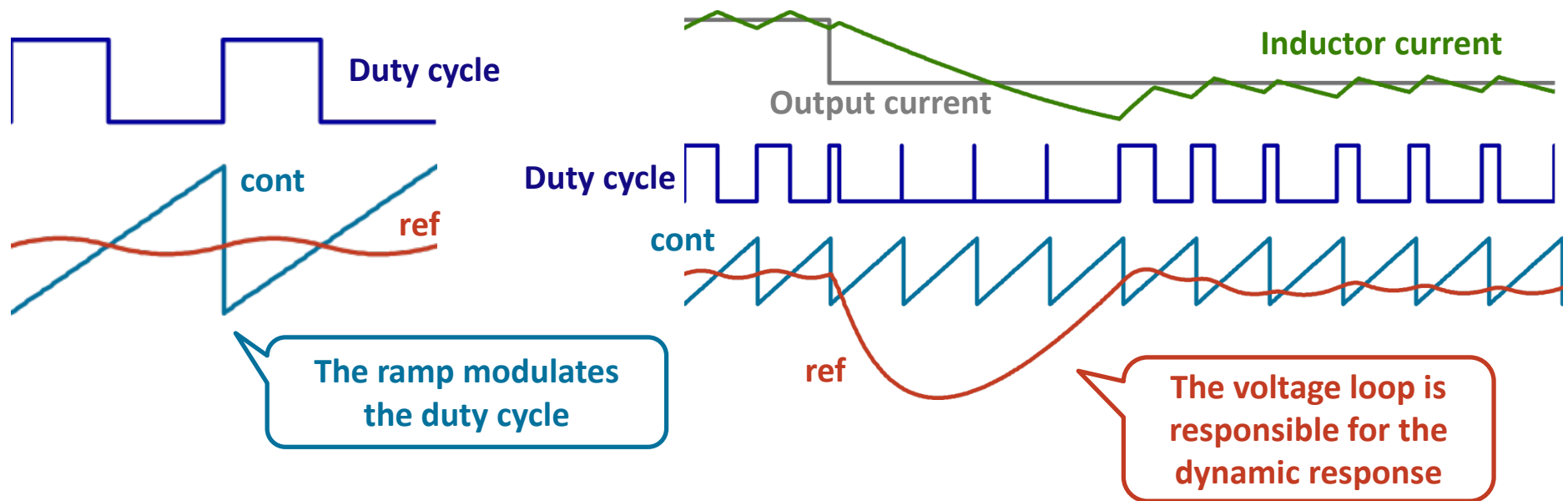
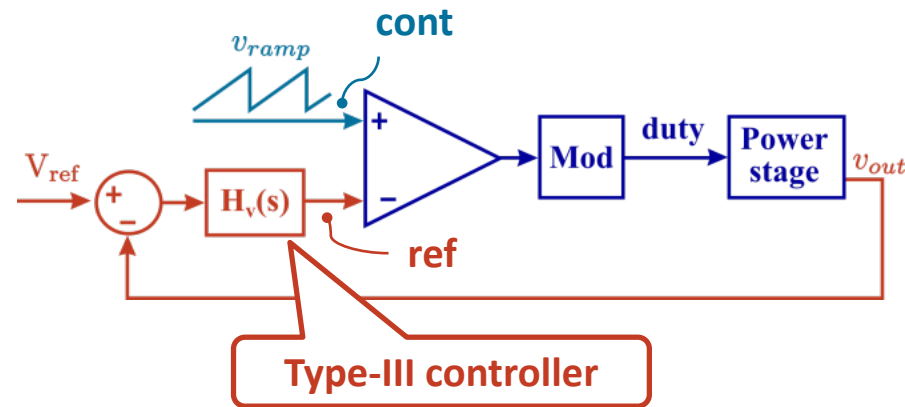


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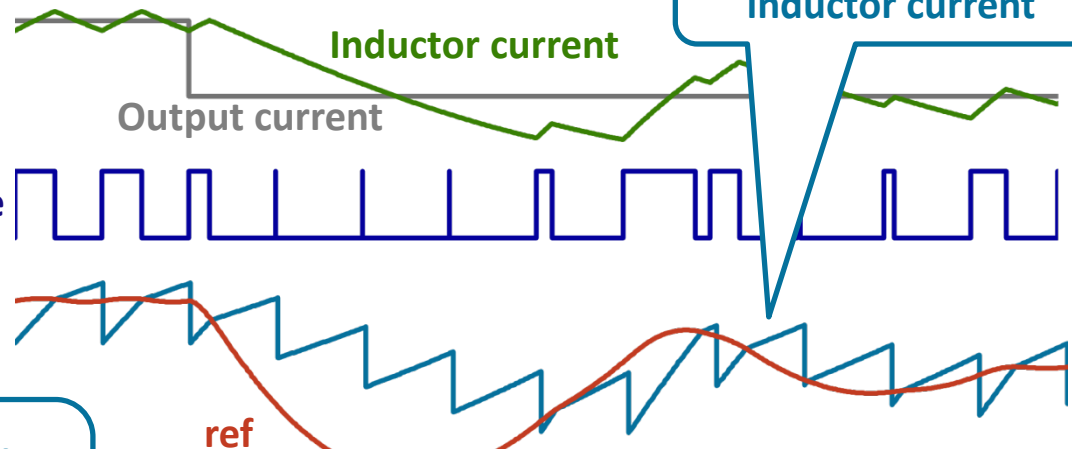
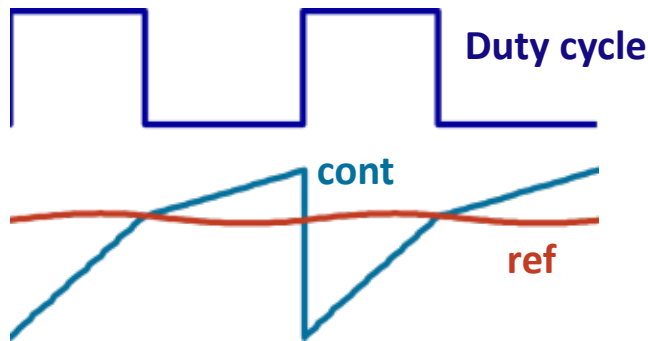
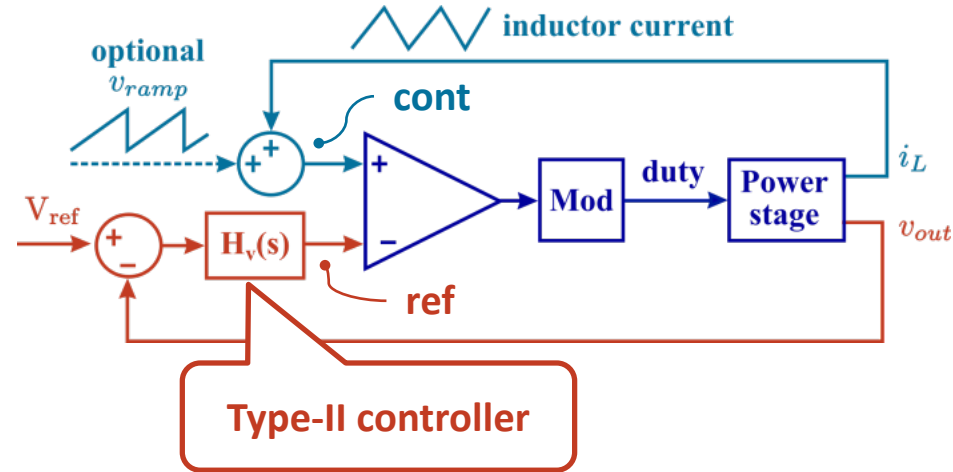


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Introduction: Voltage mode control



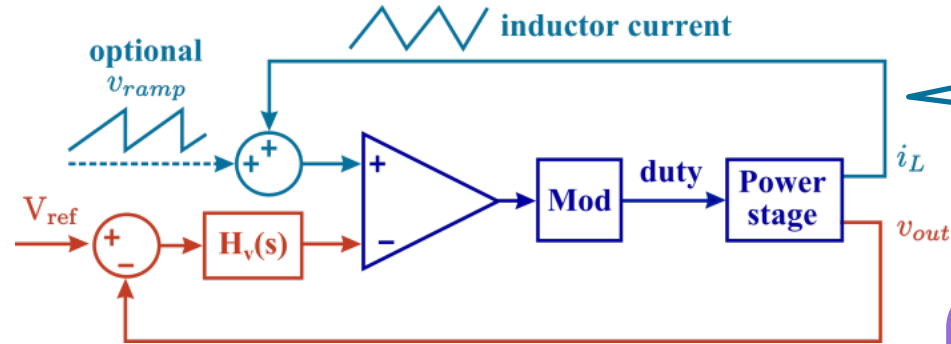
Introduction: Current mode control



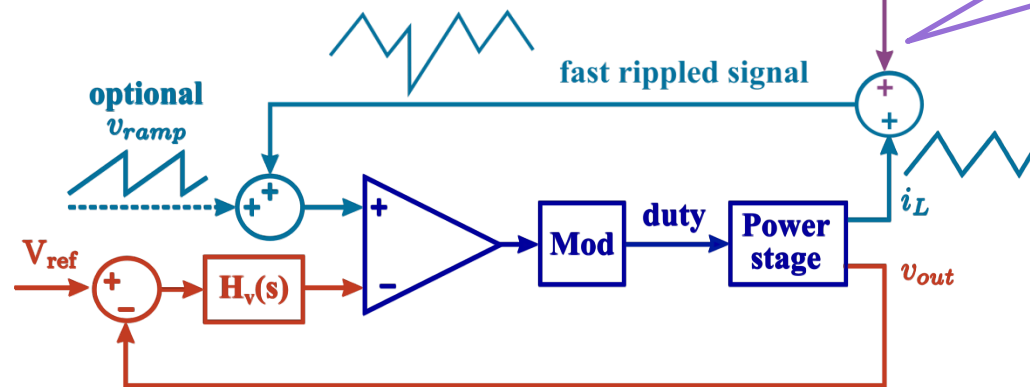
The ripple of the inductor current modulates the duty cycle

The voltage loop is still the main responsible for the dynamic response

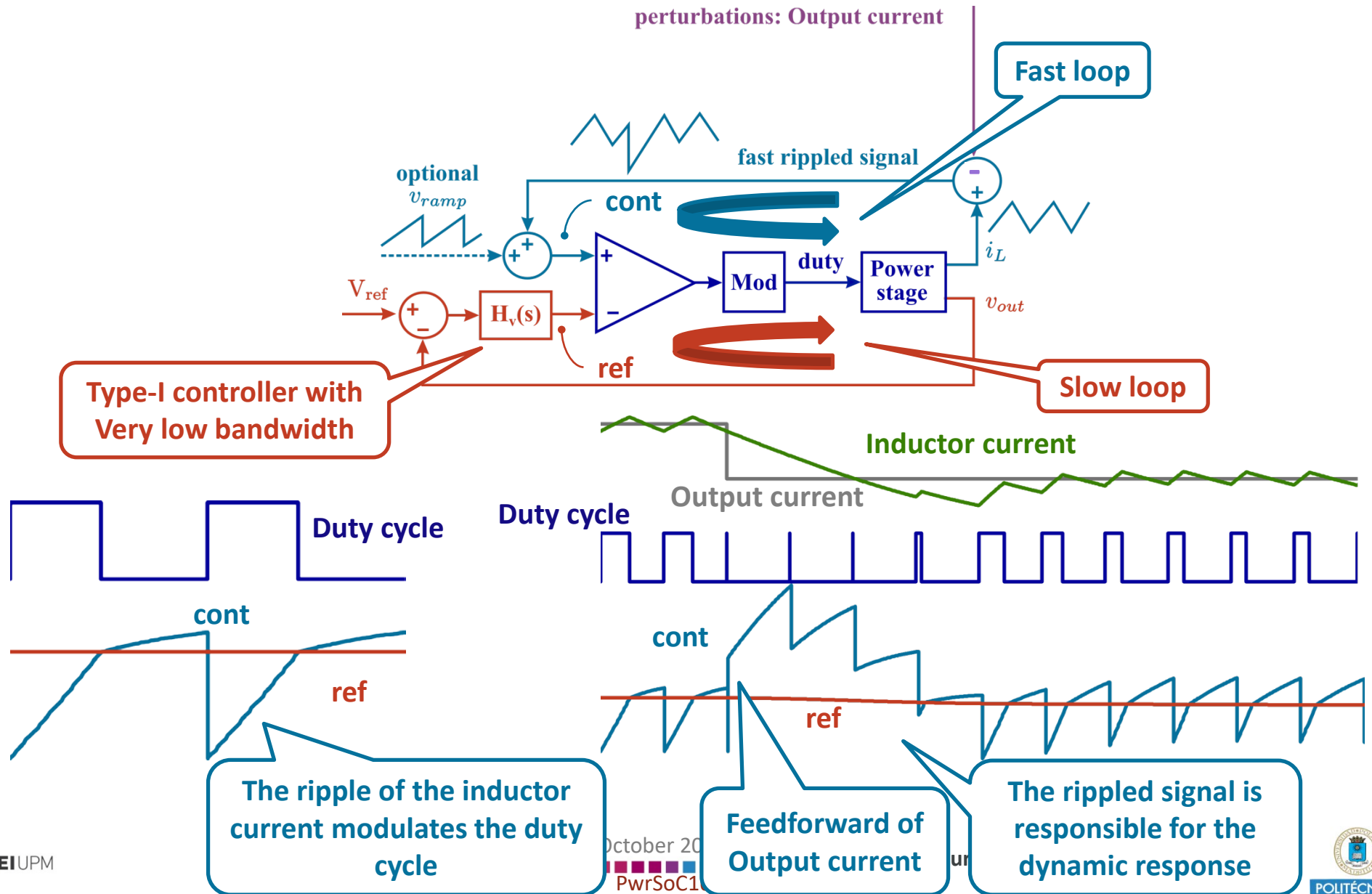
Introduction: Ripple-based control



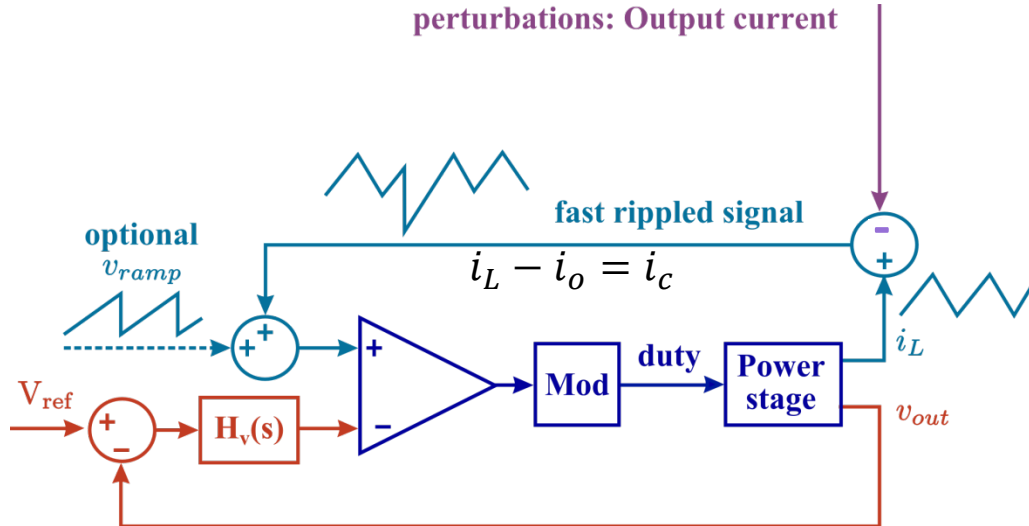
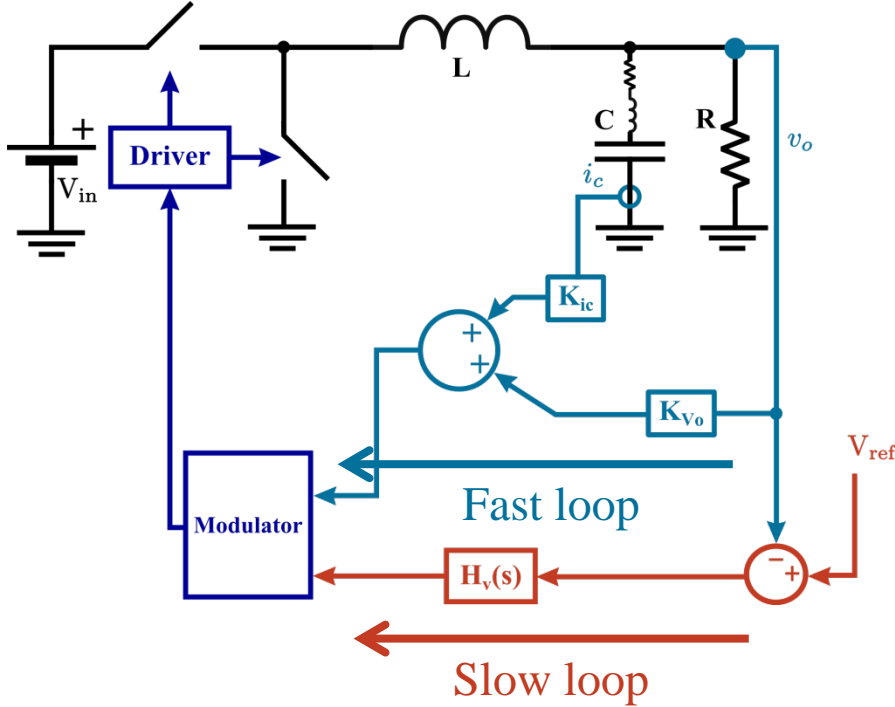
perturbations: Output current
Input voltage
Reference voltage



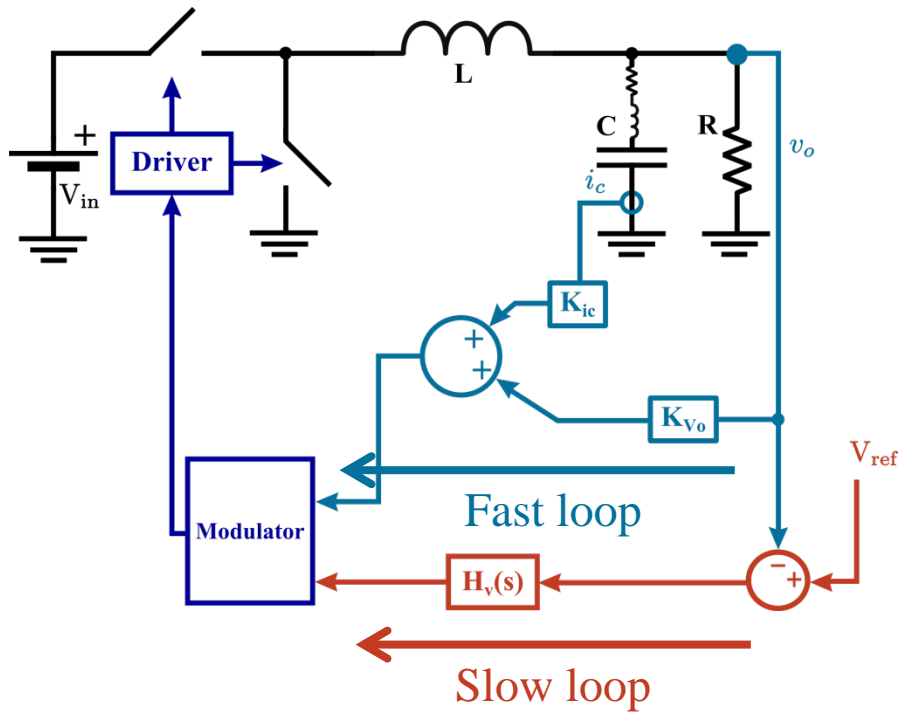
Introduction: Ripple-based control



Introduction: v^2i_c



Introduction: v^2i_c



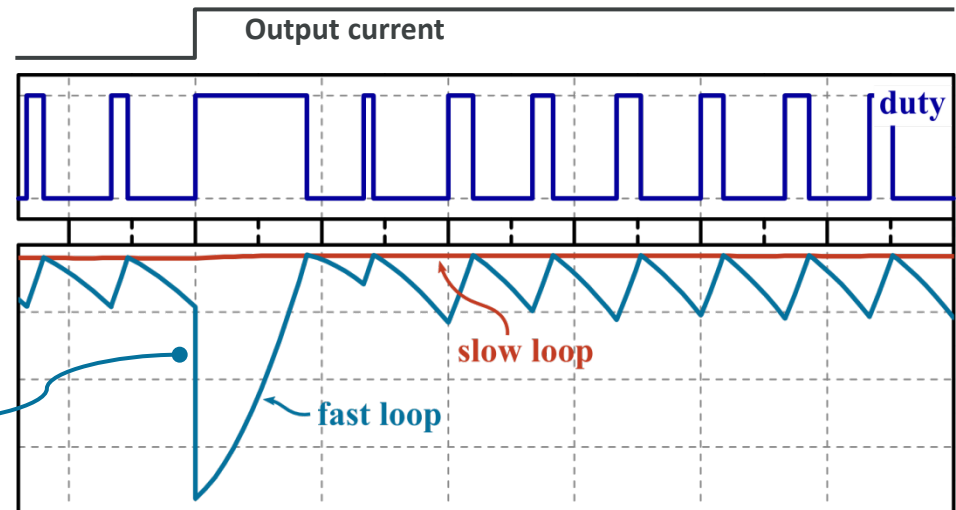
Due to feedforward of output current

Fast loop:

- Responsible for fast dynamic response

Slow loop:

- Responsible to regulate tightly the output voltage.
- Very low bandwidth



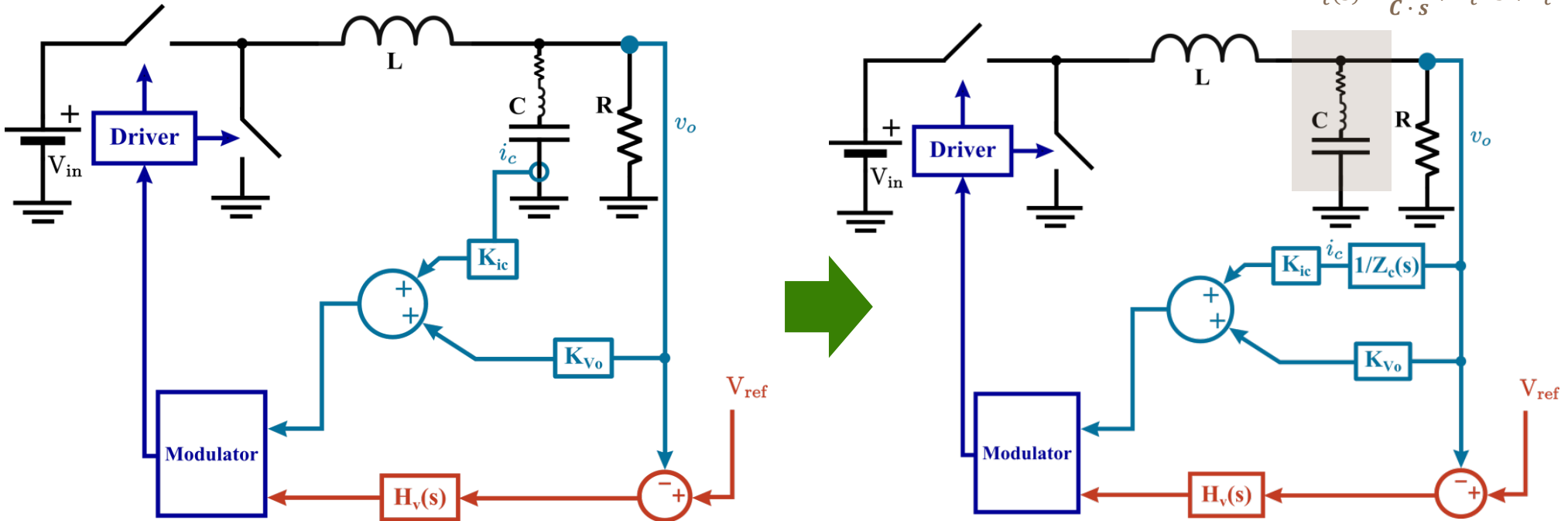
In load perturbances, the feedforward of the output current allows for a fast dynamic response

Introduction: v^2i_c

How can we measure the capacitor current?

We can estimate it by measuring only the output voltage and designing a transfer function $1/Z_c(s)$

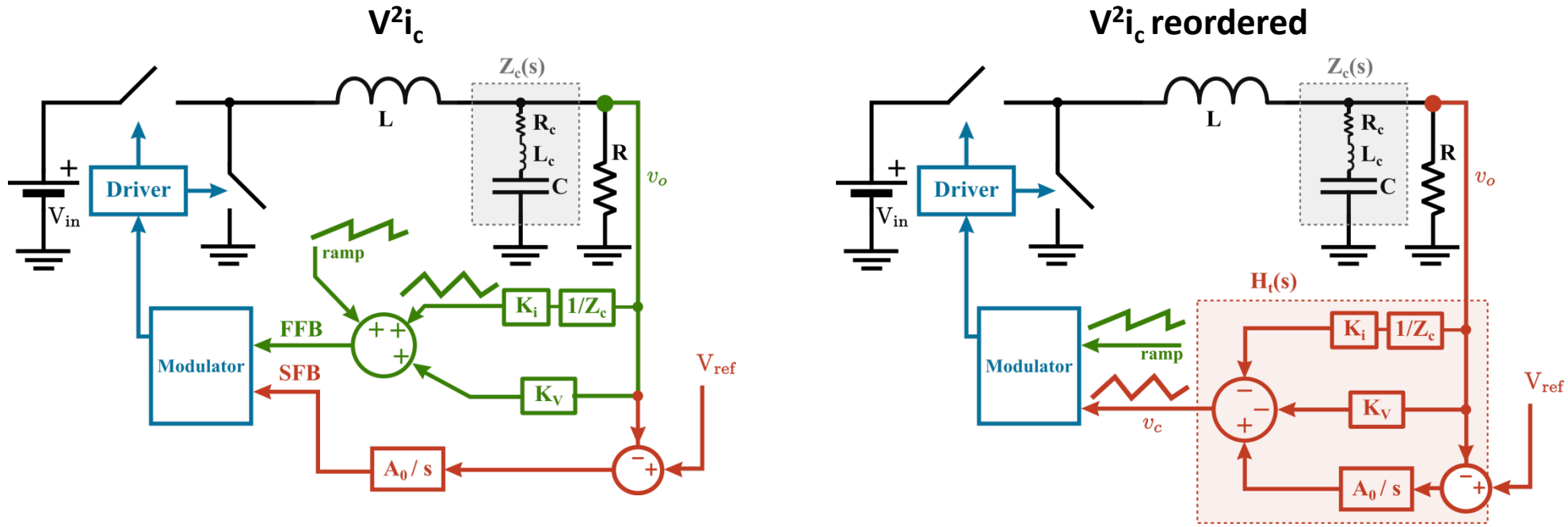
$$Z_c(s) = \frac{1}{C \cdot s} + R_c \cdot s + L_c \cdot s$$



[] M. Del Viejo, P. Alou, J. A. Oliver, O. Garcia, and J. A. Cobos, "V2IC control: A novel control technique with very fast response under load and voltage steps," in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2011, pp. 231–237.

[] Y. Yan, P.-H. Liu, F. Lee, Q. Li, and S. Tian, "V2 control with capacitor current ramp compensation using lossless capacitor current sensing," in *2013 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2013, pp. 117–124.

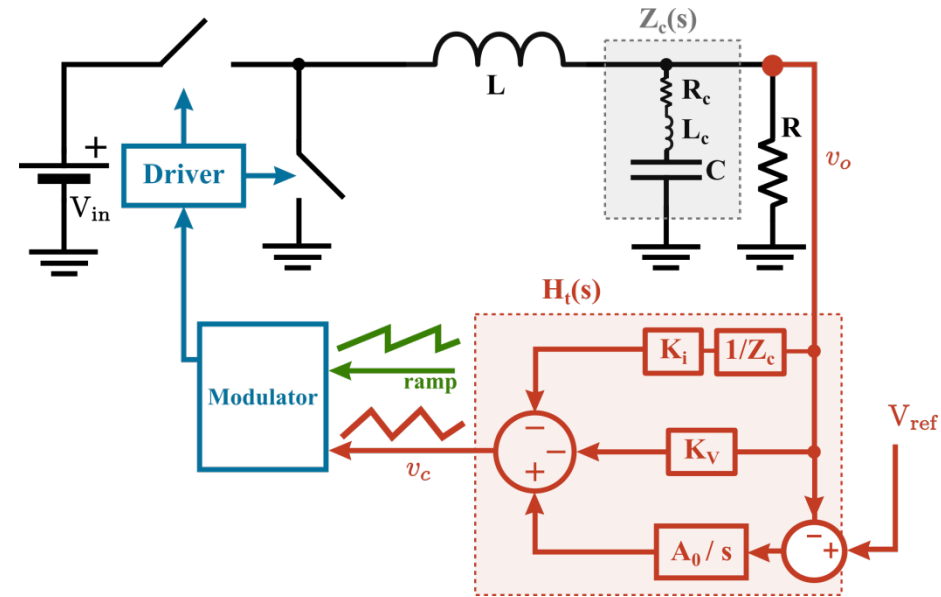
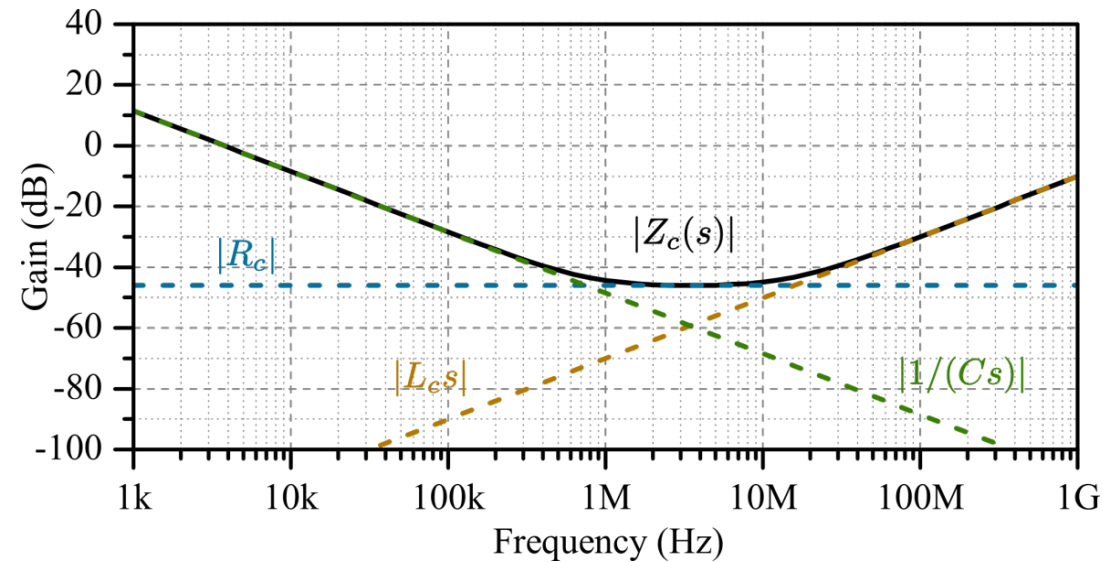
v¹ concept



Is it possible to replicate V^2i_c in voltage mode?

v¹ concept

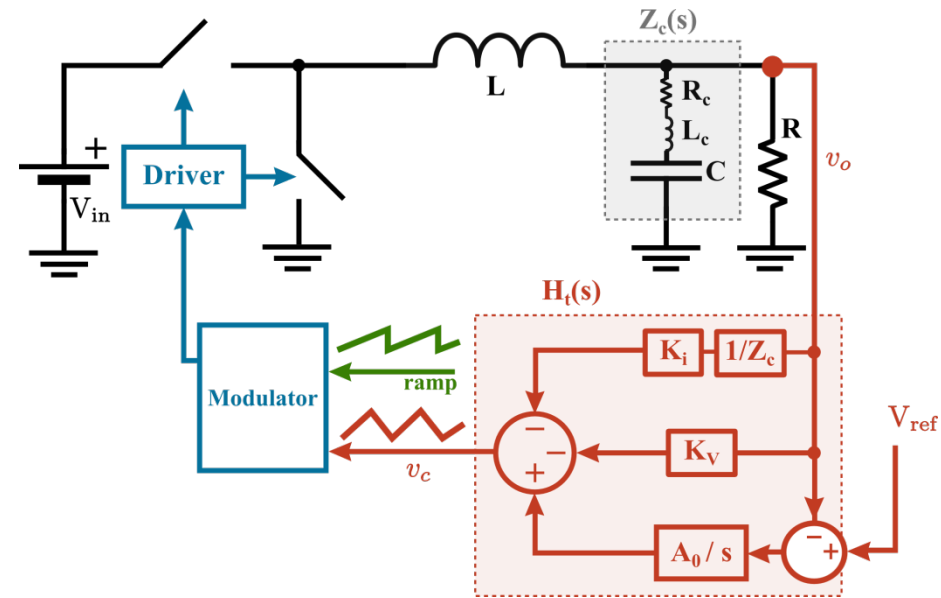
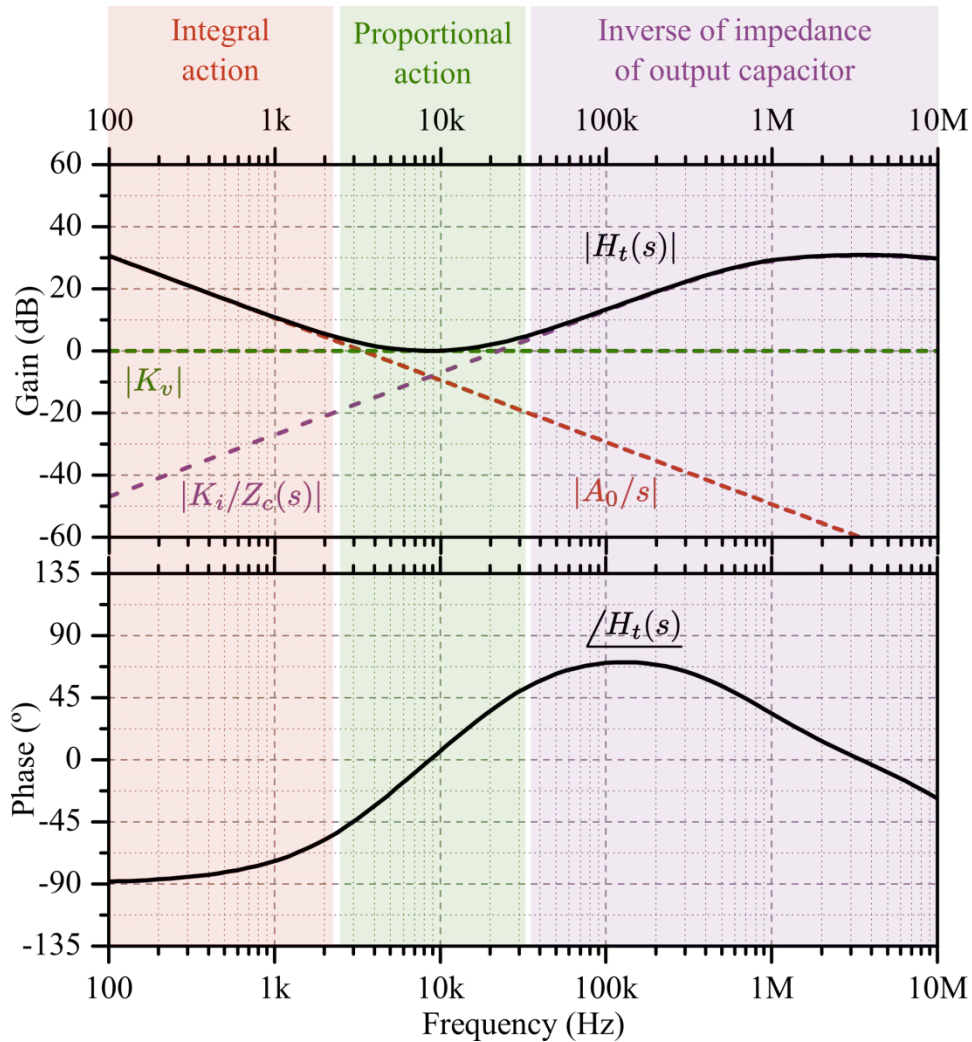
Low-Q output capacitor



$$Z_c(s) = \frac{(1 + sCR_c) \left(1 + s \frac{L_c}{R_c}\right)}{Cs}$$

$$H_t(s) = \frac{A_o}{s} + K_v + K_i \frac{1}{Z_c(s)}$$

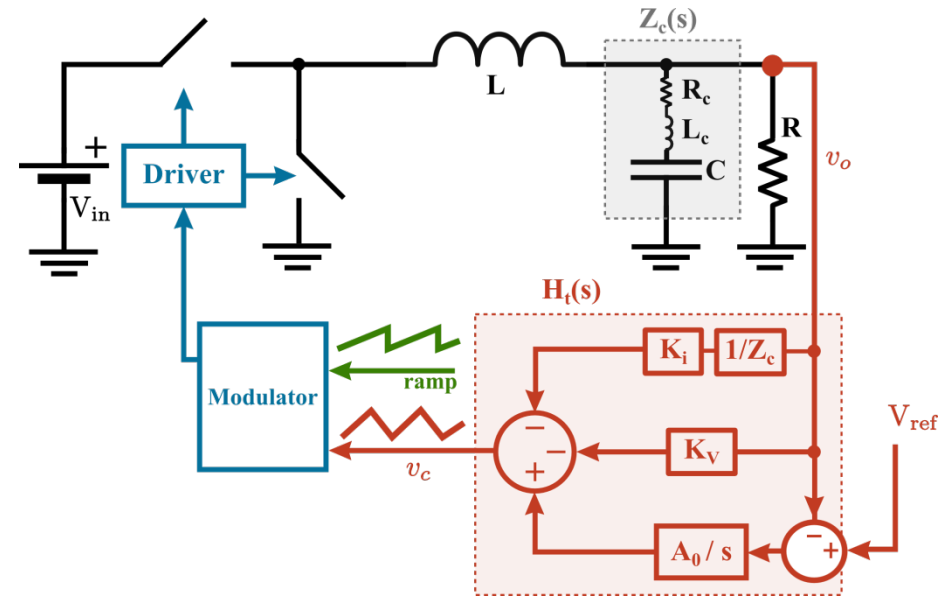
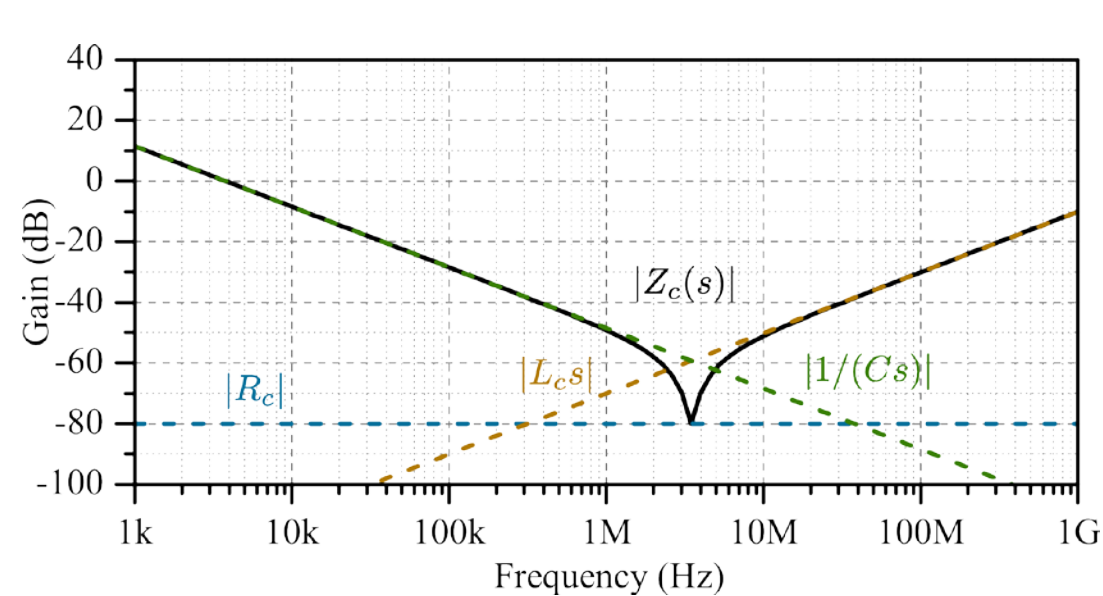
v¹ concept



$$H_t(s) = \frac{A_o}{s} + K_v + K_i \frac{1}{Z_c(s)}$$

v¹ concept

High-Q output capacitor



$$Z_c(s) = \frac{s \left(1 + \frac{1}{Q\omega_c} s + \frac{1}{\omega_c^2} s^2 \right)}{Cs}$$

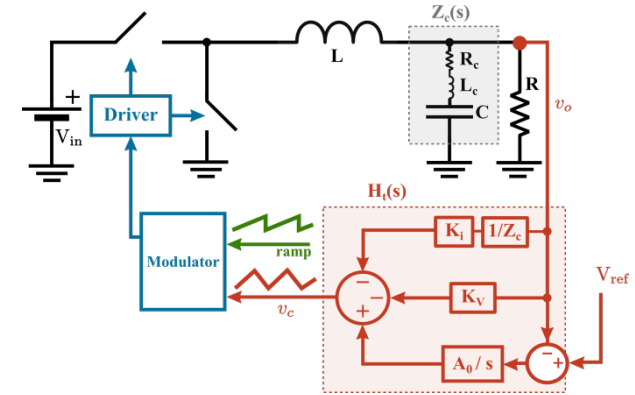
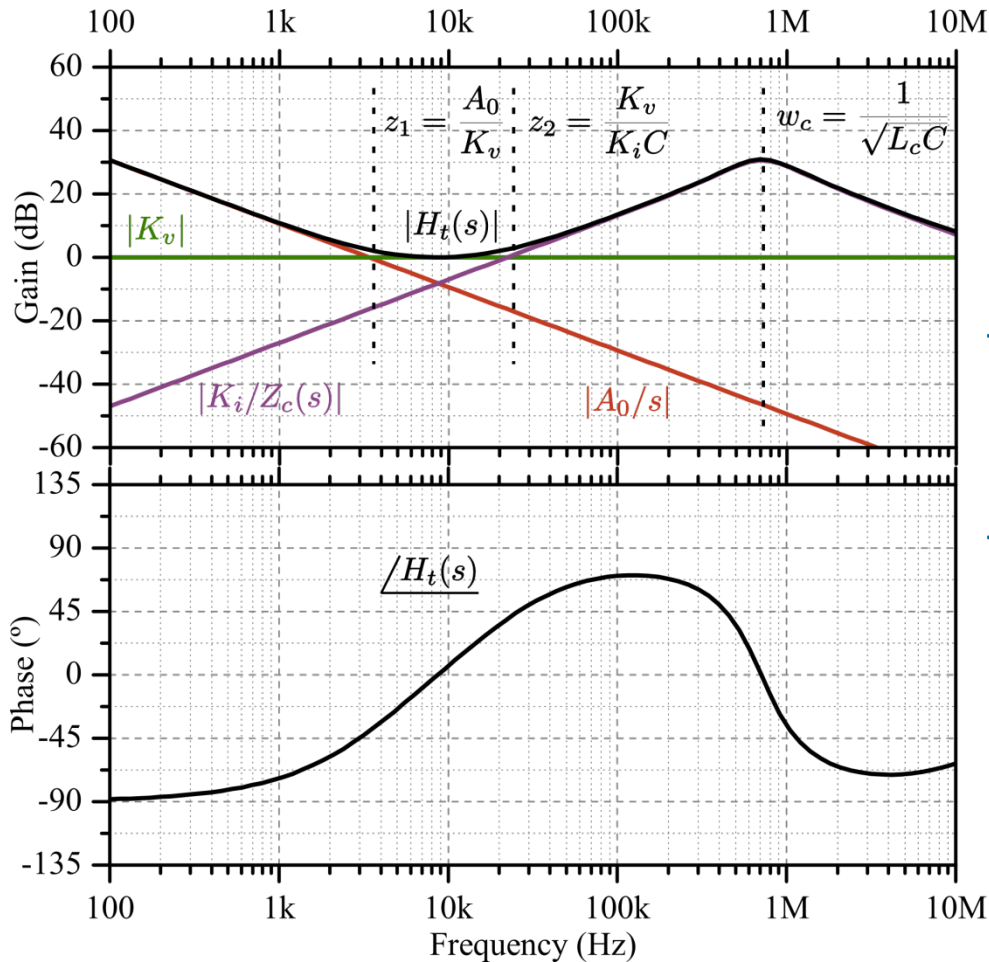
$$Q = \frac{\sqrt{L_c/C}}{R_c} \quad \omega_c = \frac{1}{\sqrt{L_c C}}$$

$$H_t(s) = \frac{A_o}{s} + K_v + K_i \frac{1}{Z_c(s)}$$

v¹ concept

High-Q output capacitor

$$H_t(s) = A_o \frac{(1 + s/z_1)(1 + s/z_2)}{s \left(1 + \frac{1}{Q\omega_c} s + \frac{1}{\omega_c^2} s^2 \right)}$$



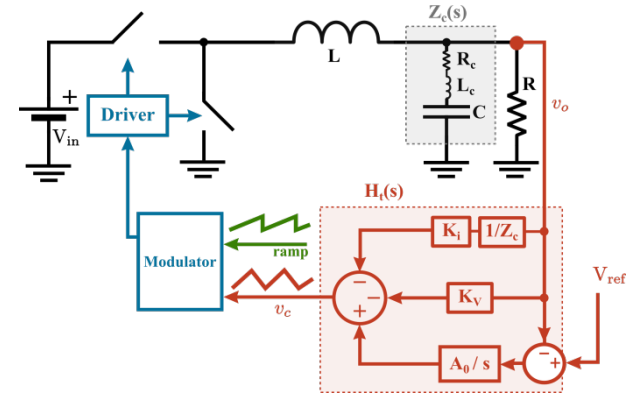
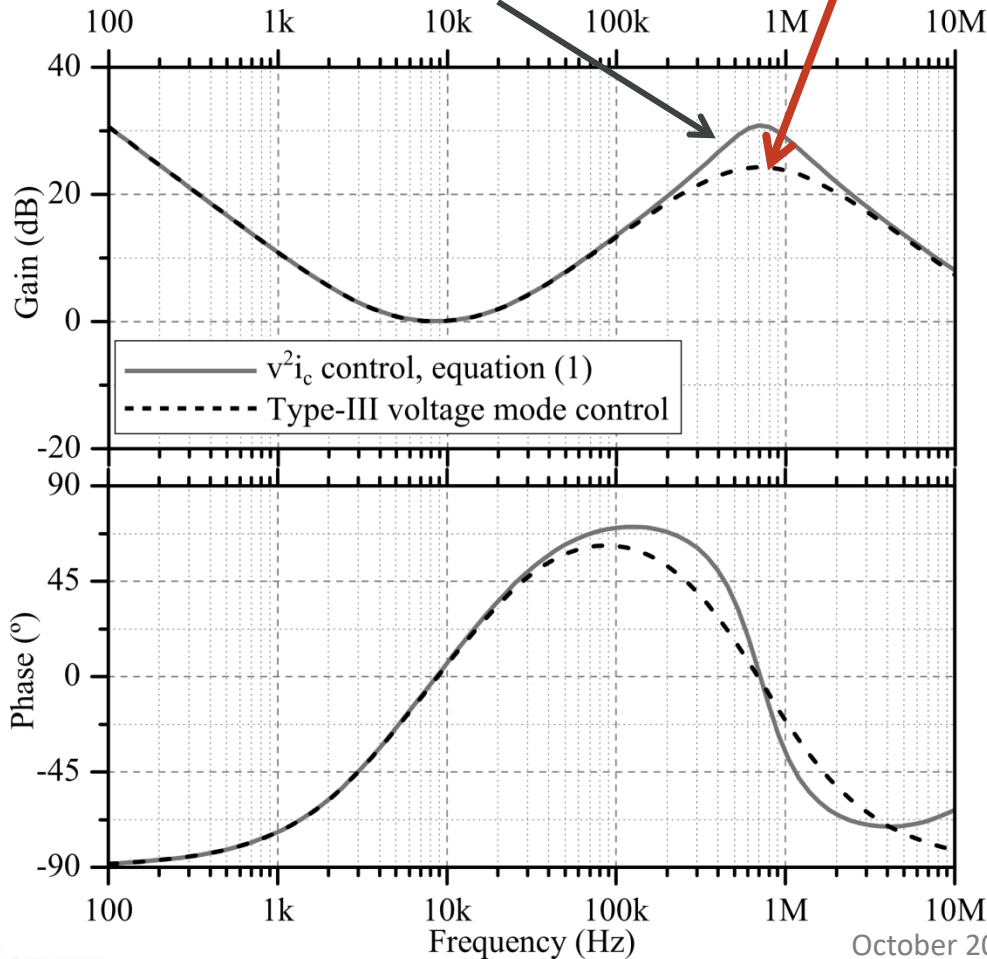
- $H_t(s)$ has complex poles. It cannot be implemented as a type-III controller!
- But it can be approximated if $\Delta B < \omega_c/10$

v¹ concept

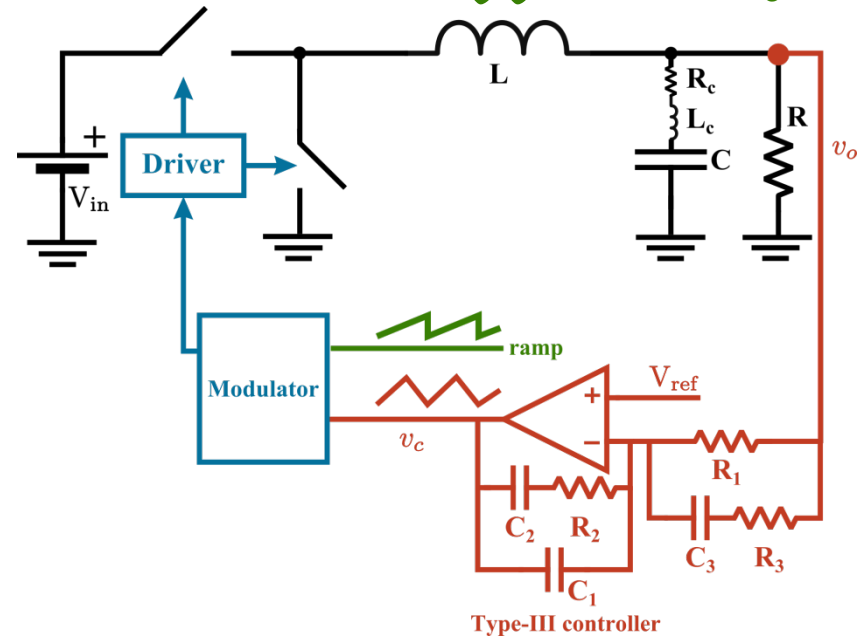
High-Q output capacitor

$$H_t(s) = A_o \frac{(1 + s/z_1)(1 + s/z_2)}{s \left(1 + \frac{1}{Q\omega_c} s + \frac{1}{\omega_c^2} s^2\right)}$$

$$H_{type-III}(s) = A_o \frac{(1 + s/z_1)(1 + s/z_2)}{s \left(1 + \frac{1}{\omega_c} s\right)^2}$$



⌋ If $\Delta B < \omega_c/10$



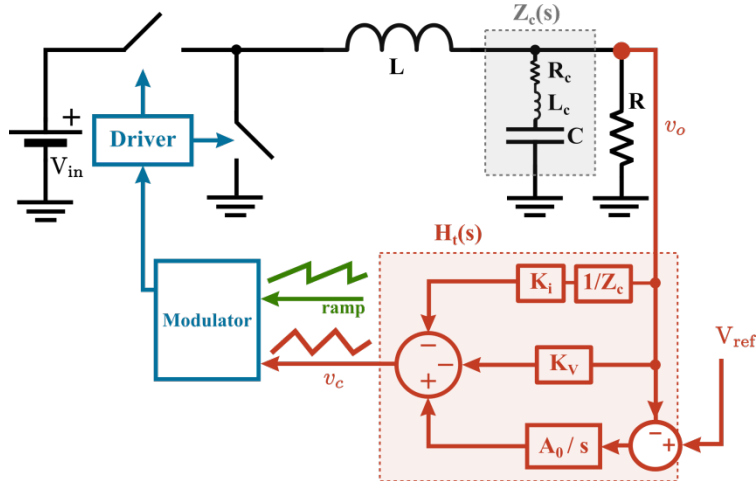
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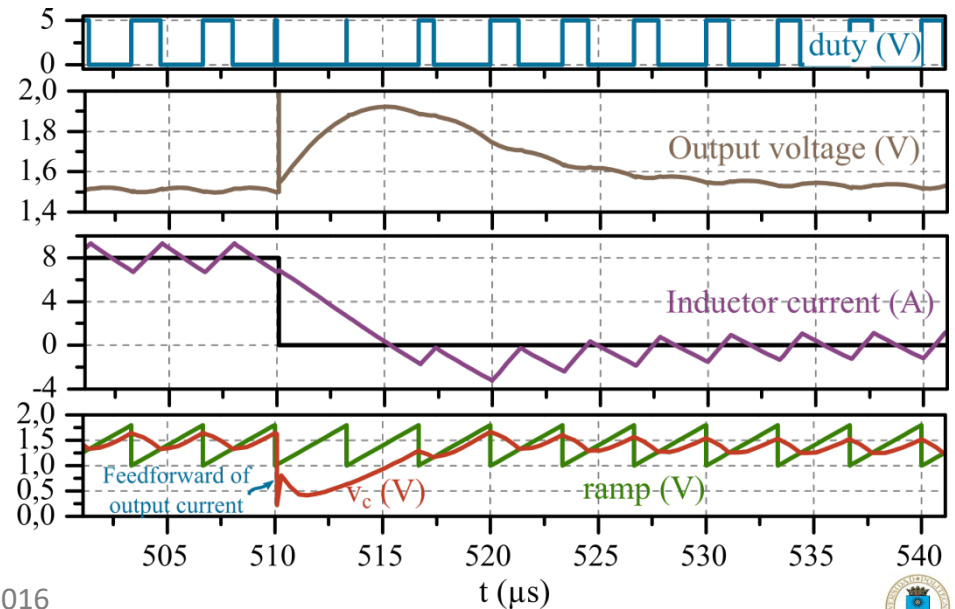
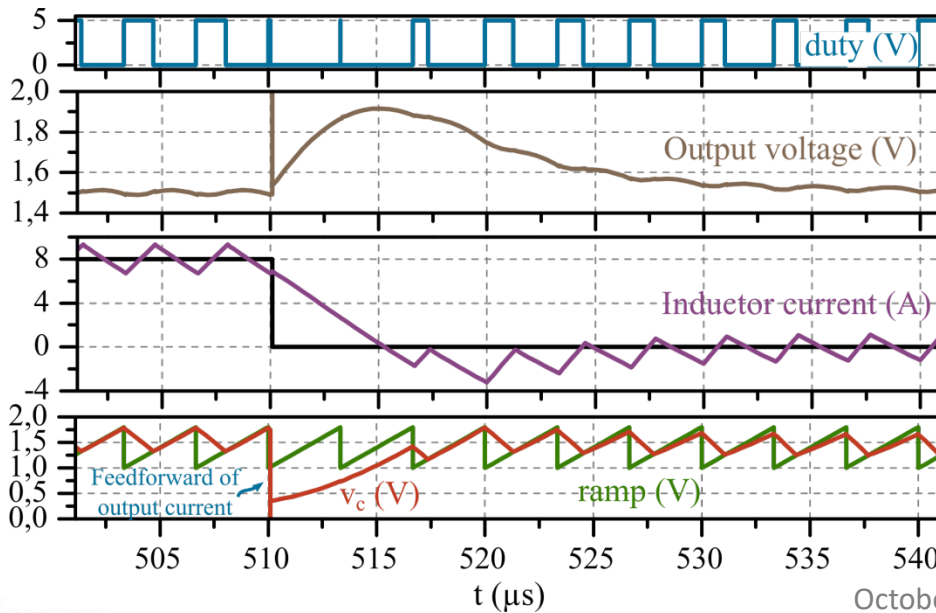
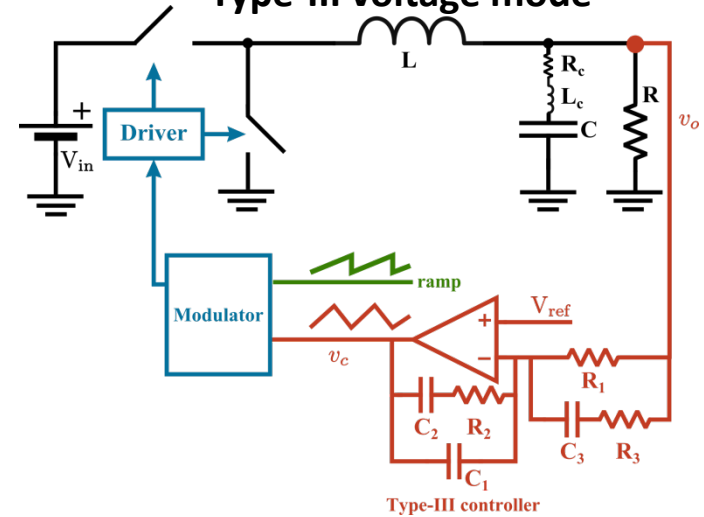
v¹ concept

High-Q output capacitor

V²i_c reordered



Type-III voltage mode



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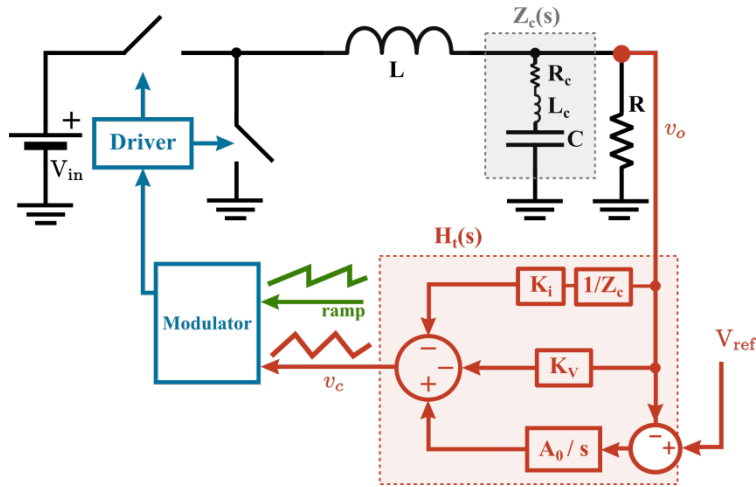


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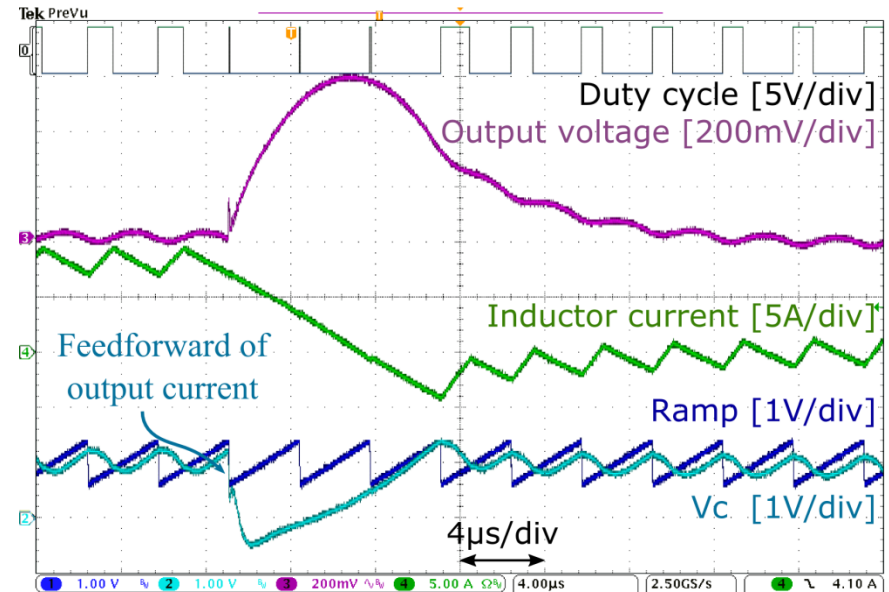
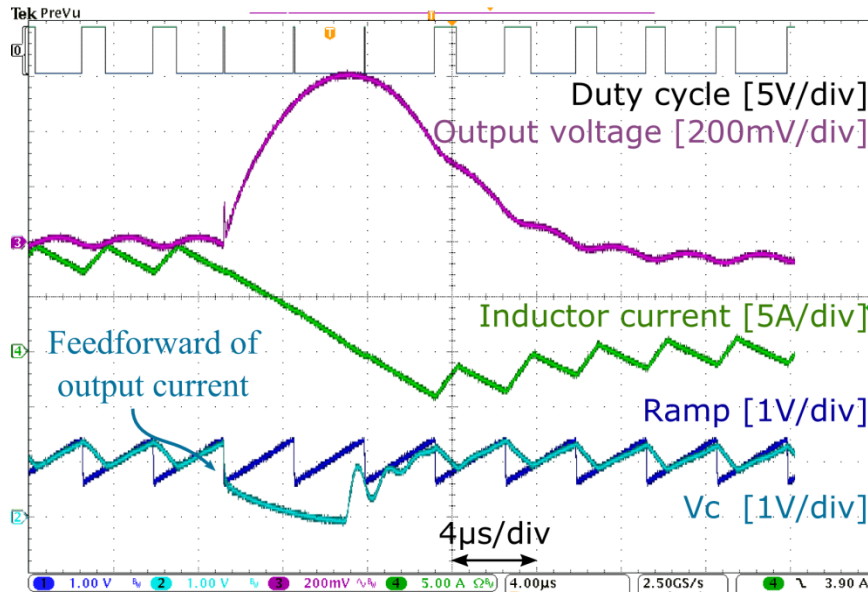
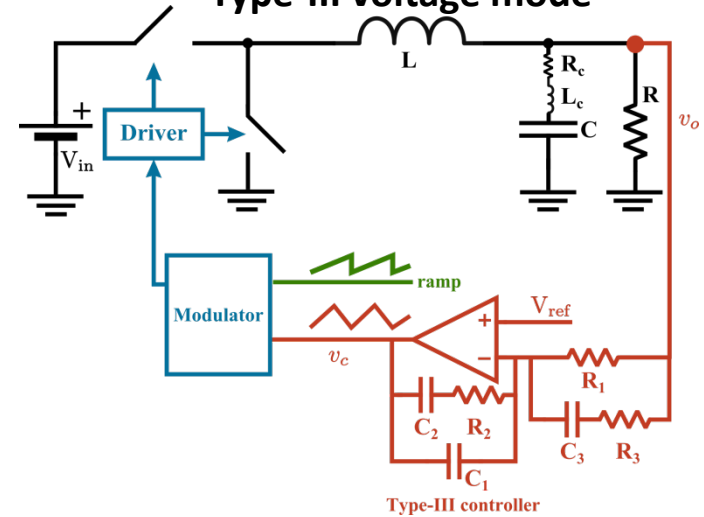
v¹ concept

High-Q output capacitor

V²i_c reordered



Type-III voltage mode

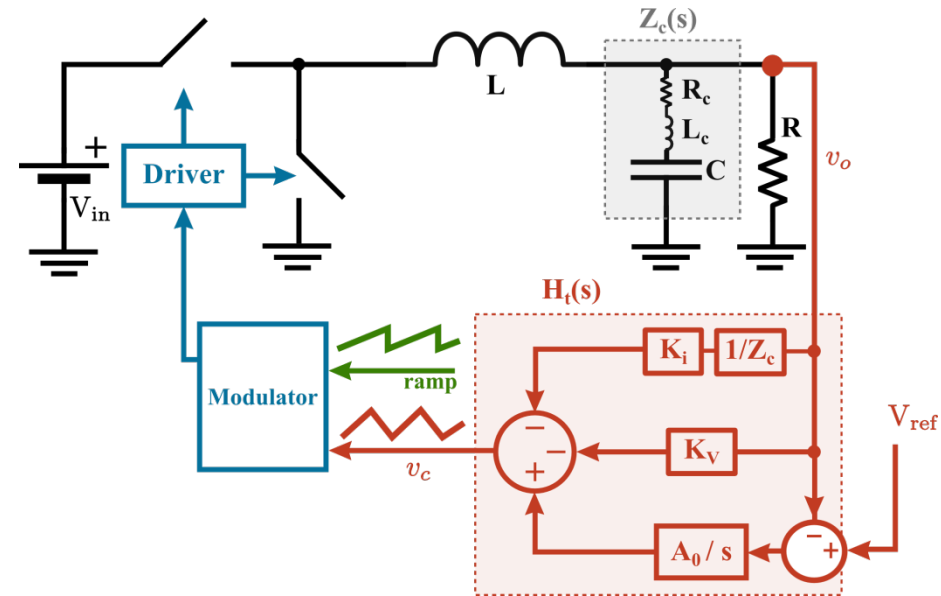
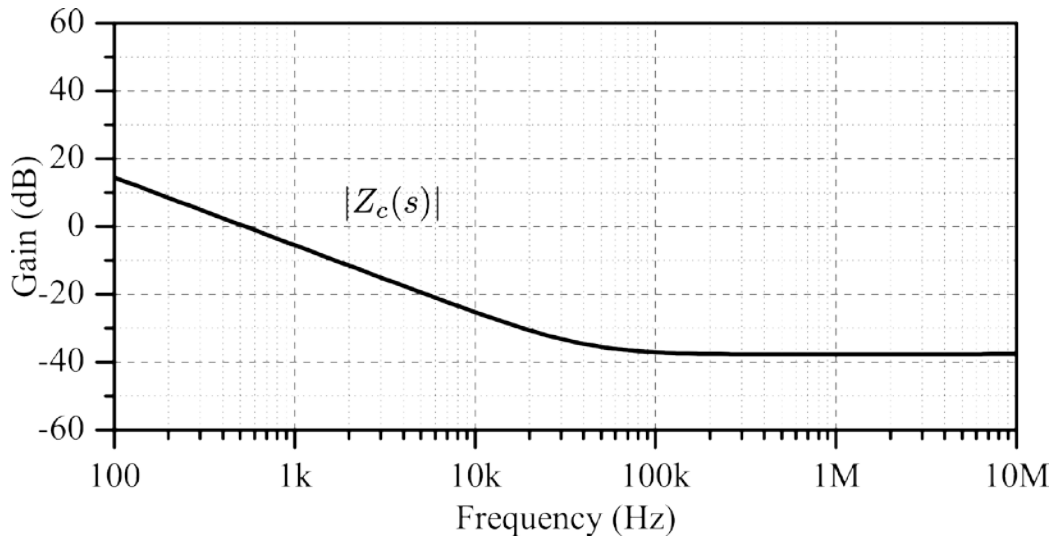


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v¹ concept

Low-ESR zero output capacitor

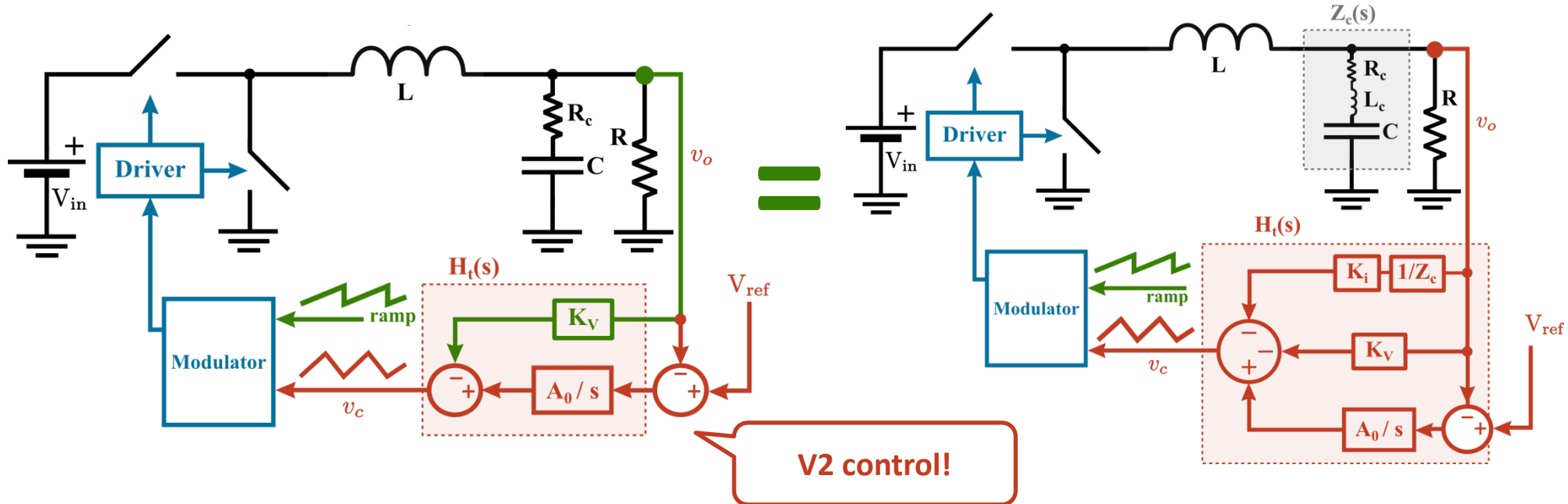


$$Z_c(s) = R_c \text{ (For the frequencies of interest!)}$$

$$H_t(s) = \frac{A_o}{s} + K_v + K_i \frac{1}{Z_c(s)}$$

v¹ concept

Low-ESR zero output capacitor



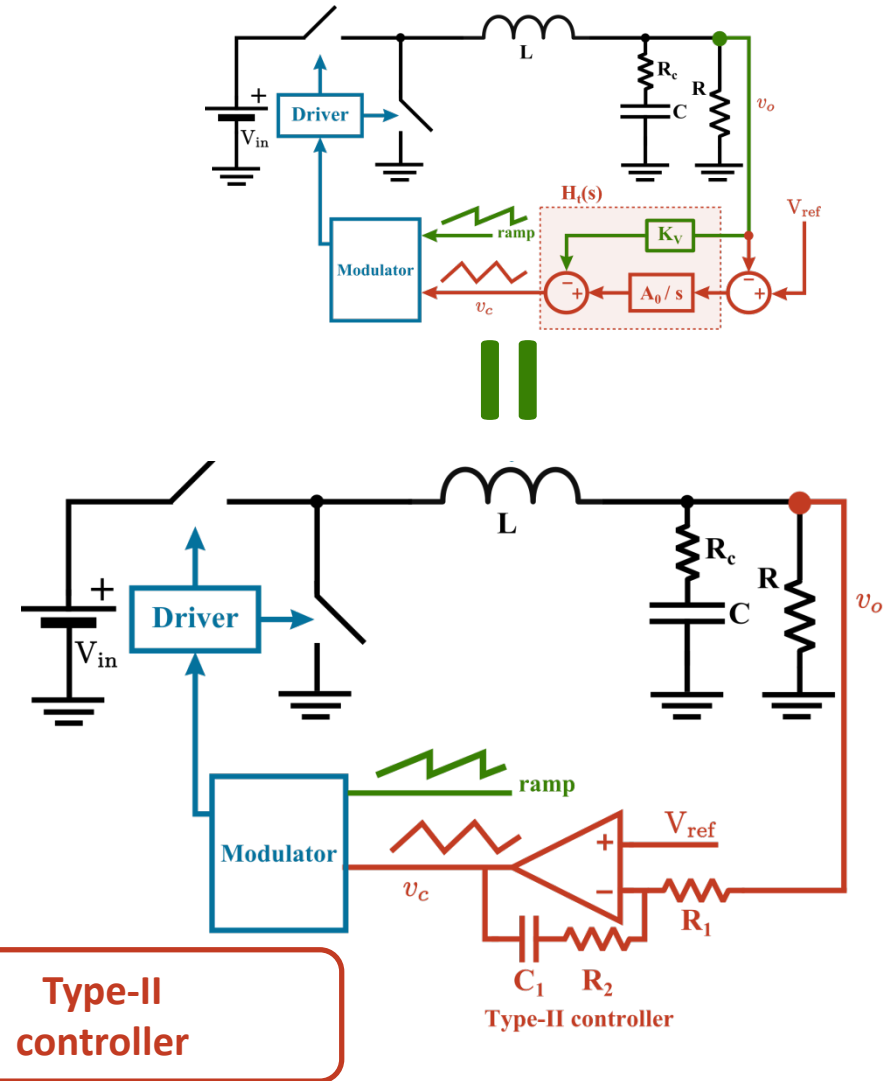
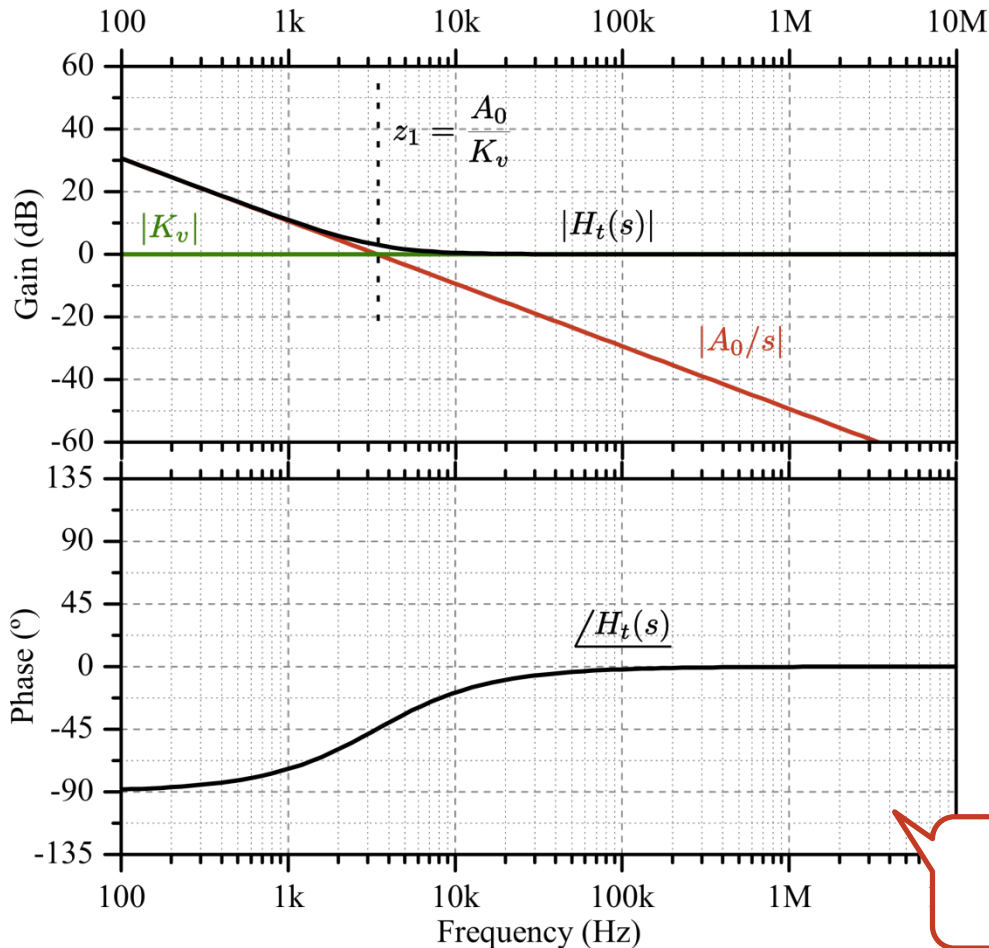
$Z_c(s) = R_c$ (For the frequencies of interest!)

$$H_t(s) = \frac{A_0}{s} + K_v + K_i \frac{1}{Z_c(s)}$$

v¹ concept

Low-ESR zero output capacitor

$$H_t(s) = A_o \frac{(1 + s/z_1)}{s}$$

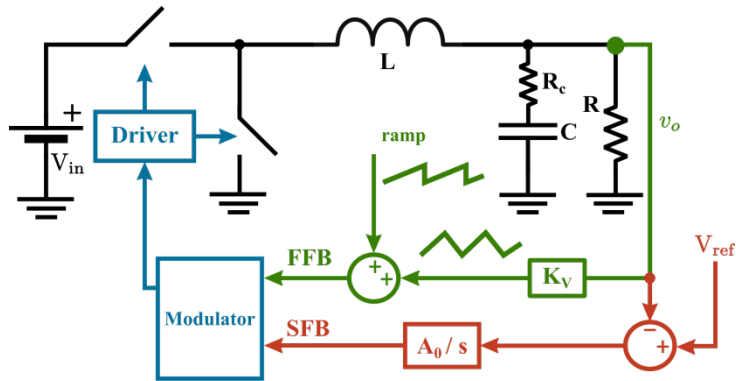


Type-II controller

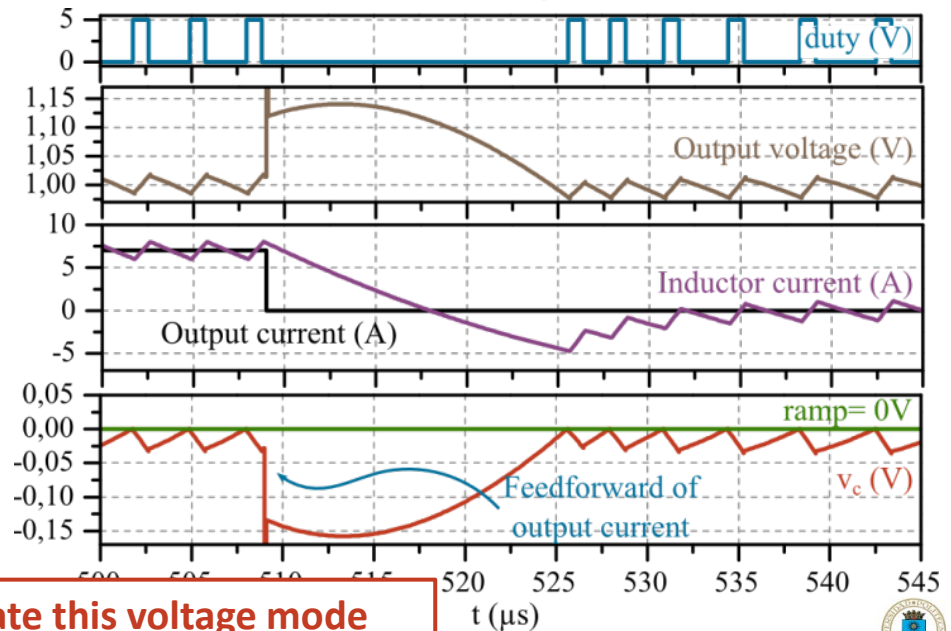
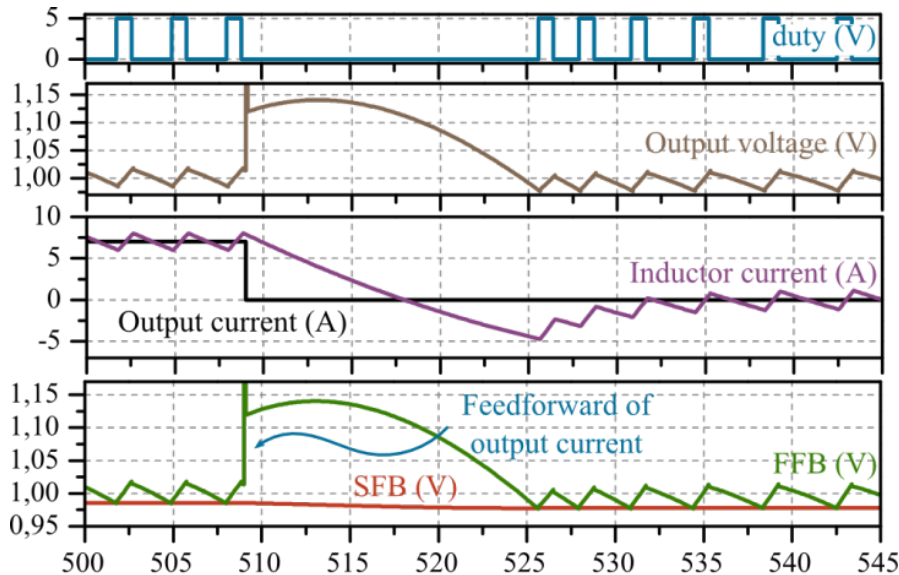
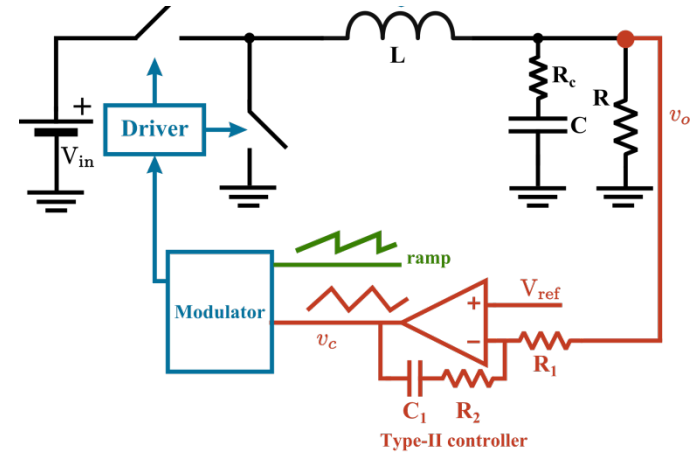
v¹ concept

Low-ESR zero output capacitor

v²



Type-II voltage mode

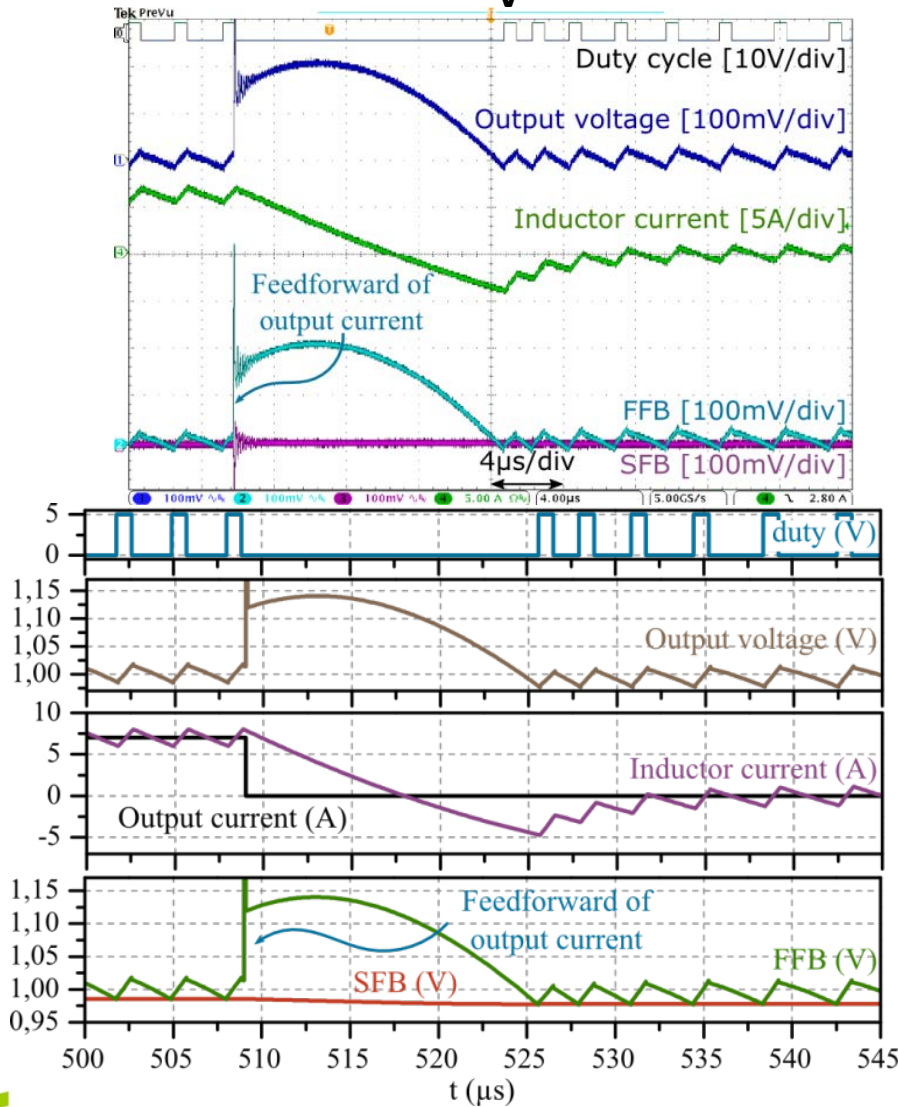


Again, it is possible to modulate this voltage mode control with constant on-time and no ramp!

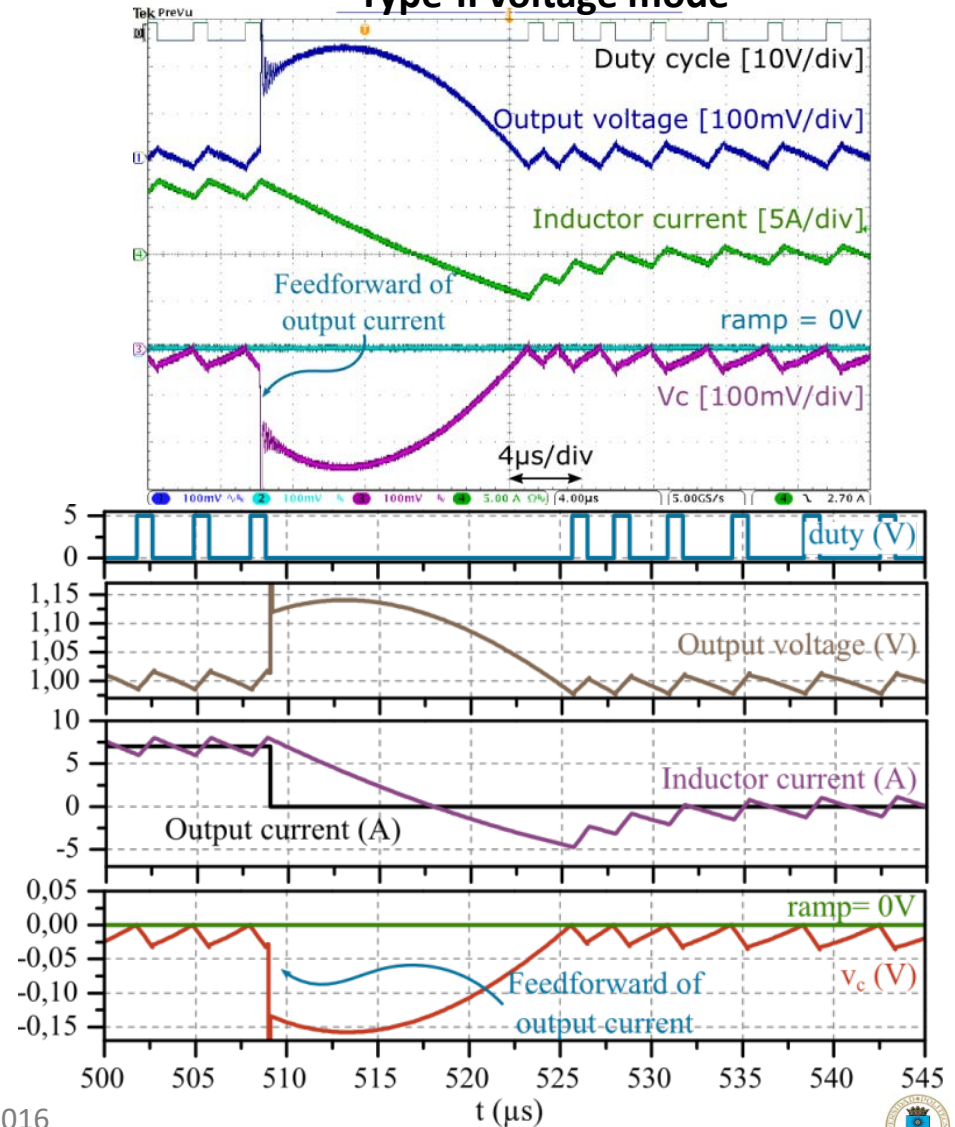
v¹ concept

Low-ESR zero output capacitor

v²



Type-II voltage mode



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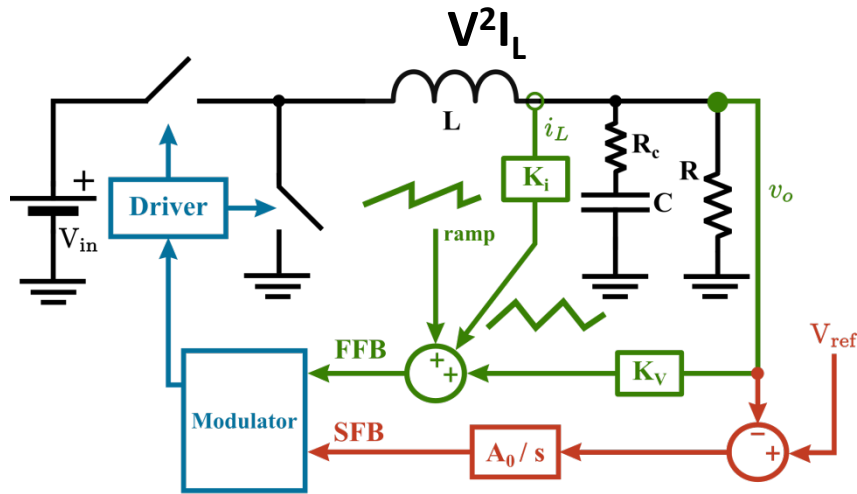


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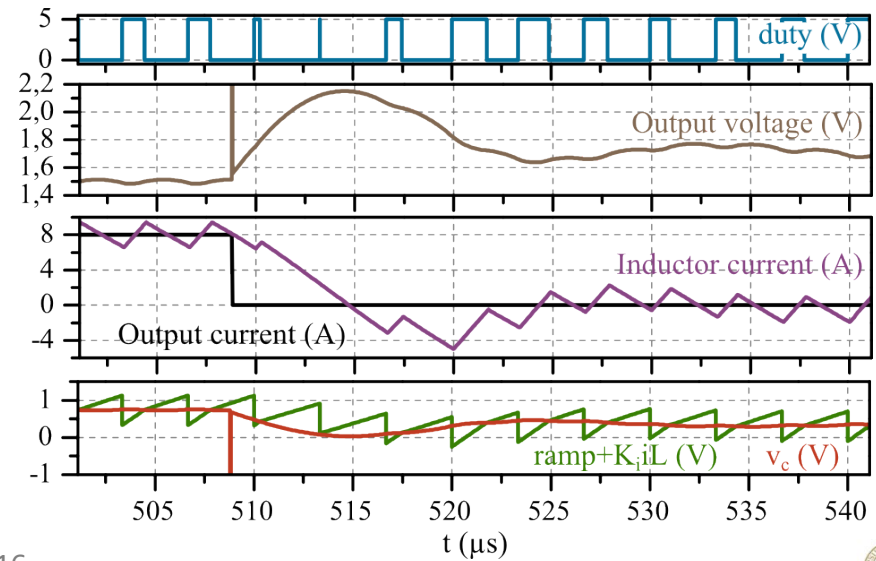
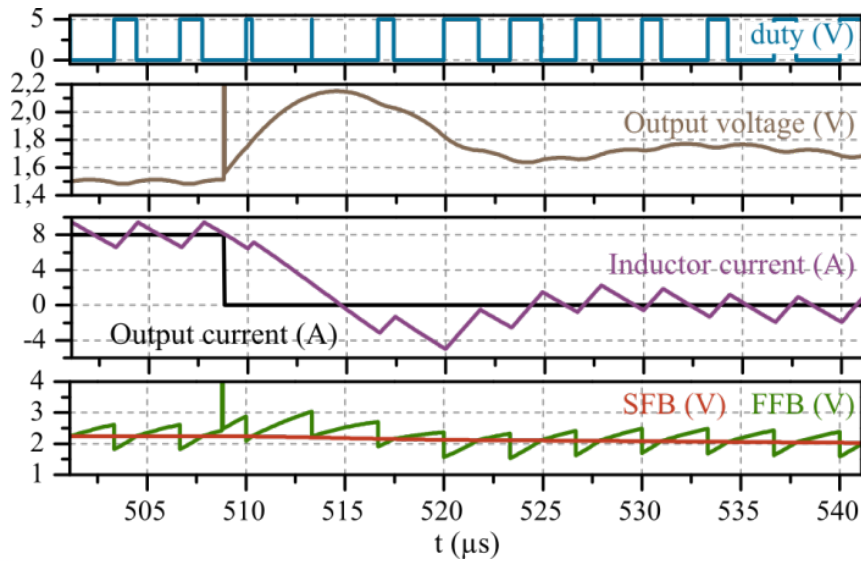
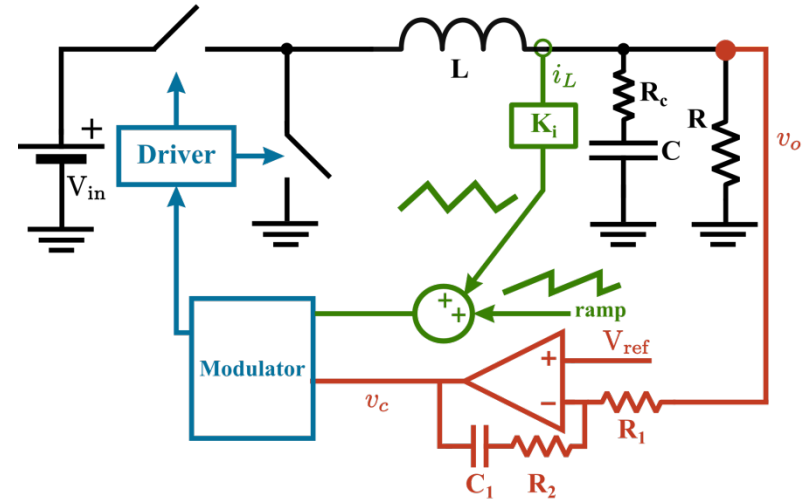
v¹ concept

V² control compensated with the inductor current



=

Type-II current mode



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v¹ concept

$$H_t(s) = \frac{A_o}{s} + K_v + K_i \frac{1}{Z_c(s)}$$

POSSIBLE IMPLEMENTATIONS OF H_t ACCORDING TO OUTPUT CAP

Low-Q cap ($Q < 0.5$)

$v^2 i_c$
type-III voltage mode

High-Q cap ($Q > 0.5$)

If $\Delta B < \omega_c/10$
 $v^2 i_c$
type-III voltage mode (approx)

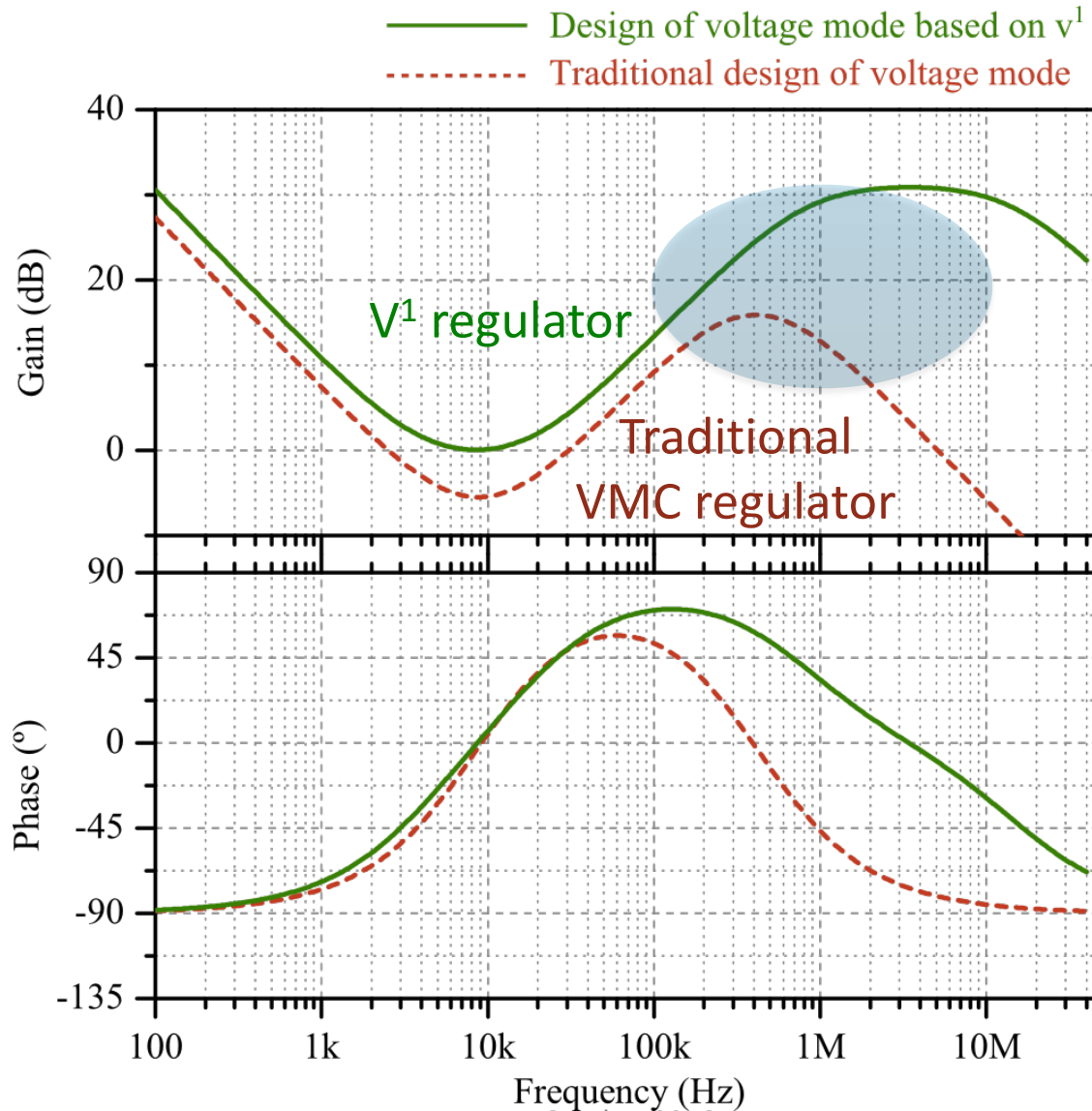
If $\Delta B > \omega_c/10$
 $v^2 i_c$

Low-ESR zero cap

$v^2 i_c$
 v^2
type-II voltage mode

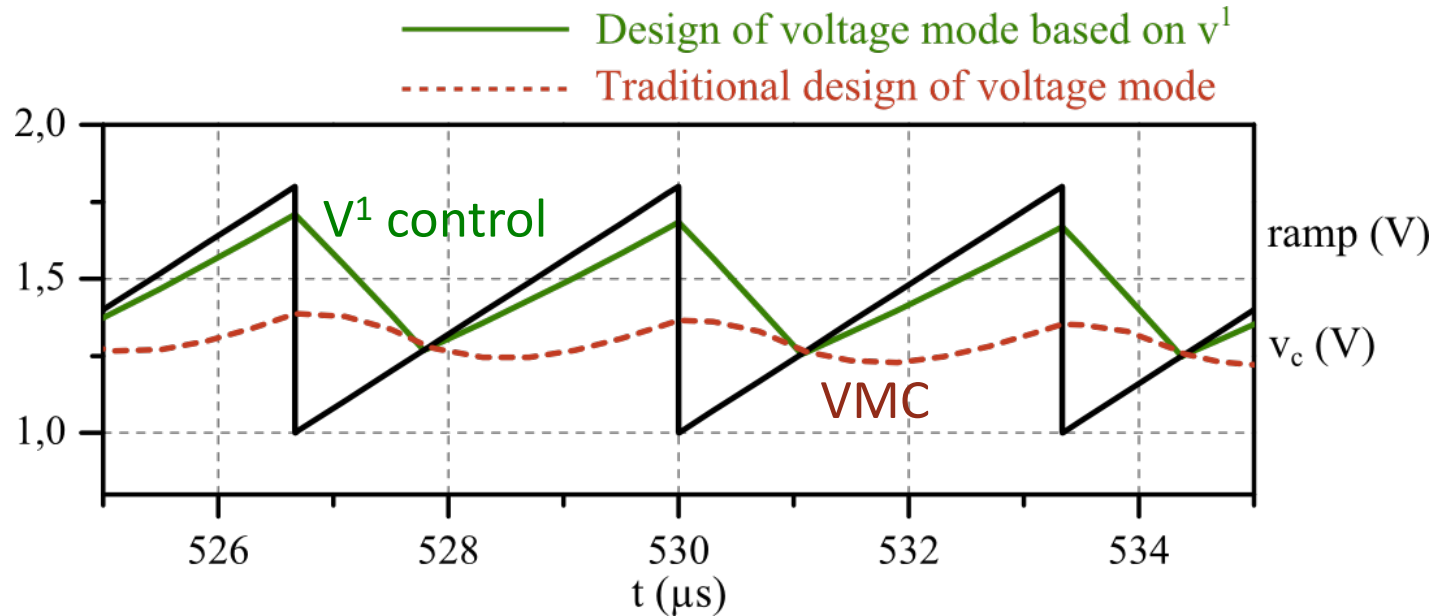
- V^2 , $V^2 i_c$, $V^2 i_L$ and V^1 are just different implementations of $H_t(s)$.
- By using only the output voltage, it is possible to emulate a current mode control with feedforward of output current $\rightarrow V^1$ concept
- Keep the ripple information in the loop!!!

Comparison of traditional VMC design and V1 concept



Keep the ripple information in the loop!!!

V1 concept is a ripple based control: subharmonic oscillations!!



... BUT accurate models are needed to design with robustness....

Discrete modelling and Floquet theory

- Robustness analysis and optimization
- High accuracy

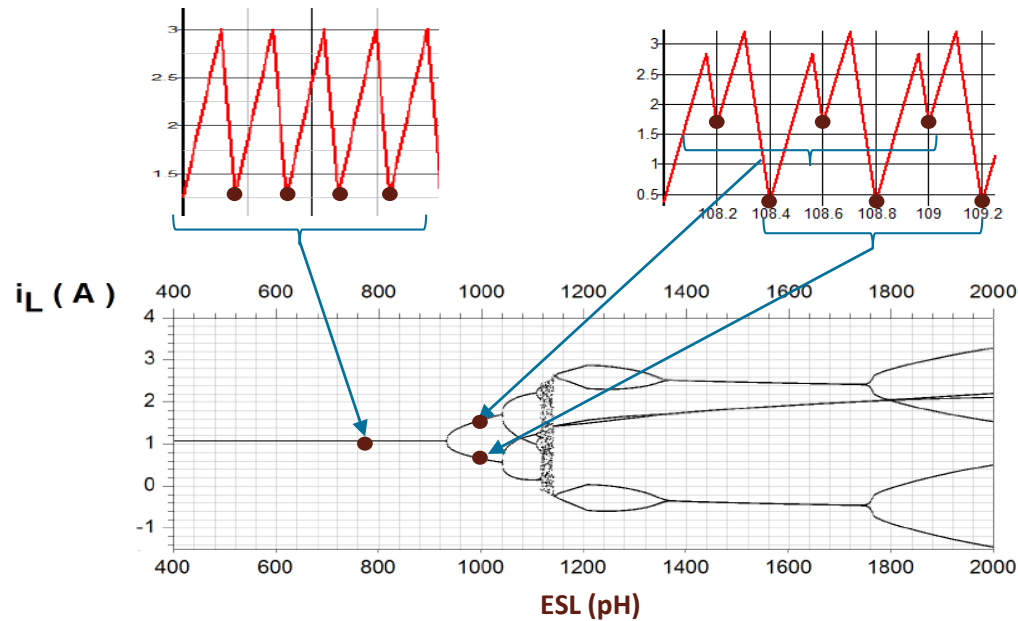


Cortes, J.; Svikovic, V.; Alou, P.; Oliver, J.; Cobos, J.; Wisniewski, R., "Accurate analysis of sub-harmonic oscillations of V2 and V2lc controls applied to Buck converter," Power Electronics, IEEE Transactions on , early access

Floquet theory

Bifurcation phenomena

- Sub-harmonic oscillations can be seen as a bifurcation where the system is unable to maintain a T-periodic solution



Bifurcation diagram

Floquet theory

Bifurcation phenomena

- Sub-harmonic oscillations can be seen as a bifurcation where the system is unable to maintain a T-periodic solution

Stability is analyzed by Floquet theory.

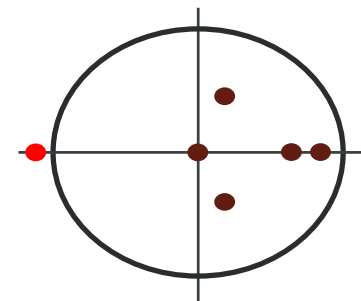
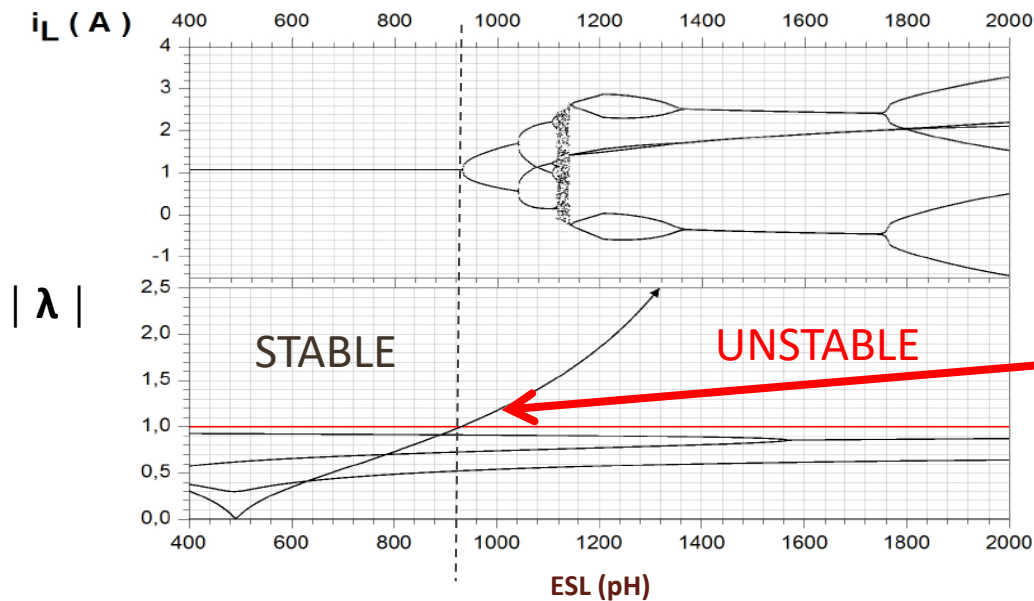
- If a perturbation grows over a period \rightarrow unstable

$$\Delta x_{k+1} = \Phi_{cycle} \cdot \Delta x_k$$

λ = eigenvalues of Φ_{cycle}

$|\lambda| < 1$, stable

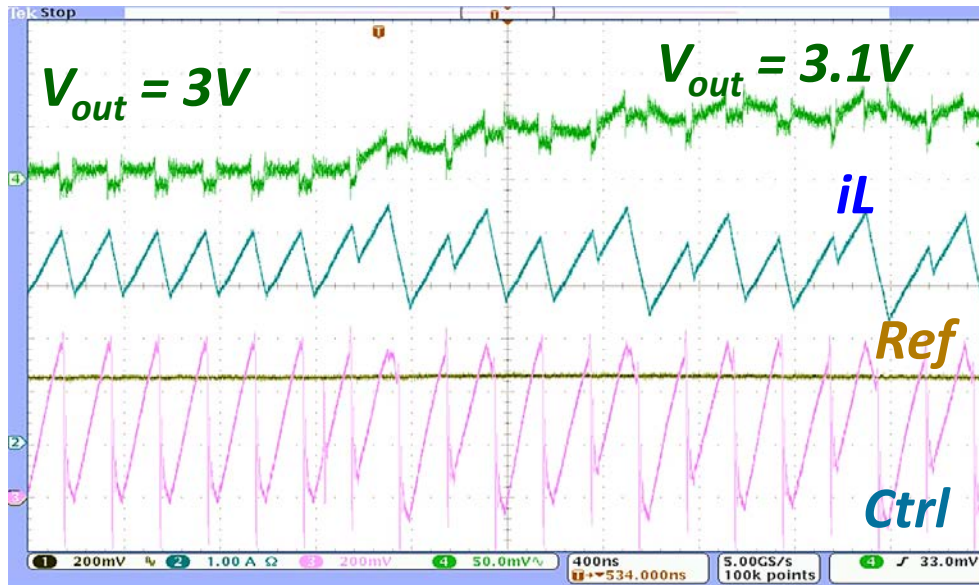
$|\lambda| > 1$, sub-harmonic oscillation



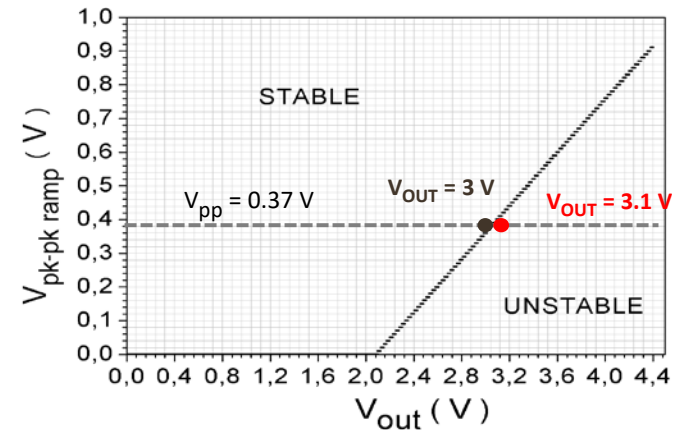
Floquet multipliers

Floquet Theory: robust design regarding all the tolerances

V^2I_c



Experimental sub-harmonic oscillation on V^2I_c control



Predicted stability behavior

The Floquet theory predicts accurately the oscillation!

$$V_{out} = 3V \rightarrow \lambda = -0.966$$

$$V_{out} = 3.1V \rightarrow \lambda = -1.06$$

Out of unit circle!

v¹ concept

$$H_t(s) = \frac{A_o}{s} + K_v + K_i \frac{1}{Z_c(s)}$$

POSSIBLE IMPLEMENTATIONS OF H_t ACCORDING TO OUTPUT CAP

Low-Q cap ($Q < 0.5$)

$v^2 i_c$
type-III voltage mode

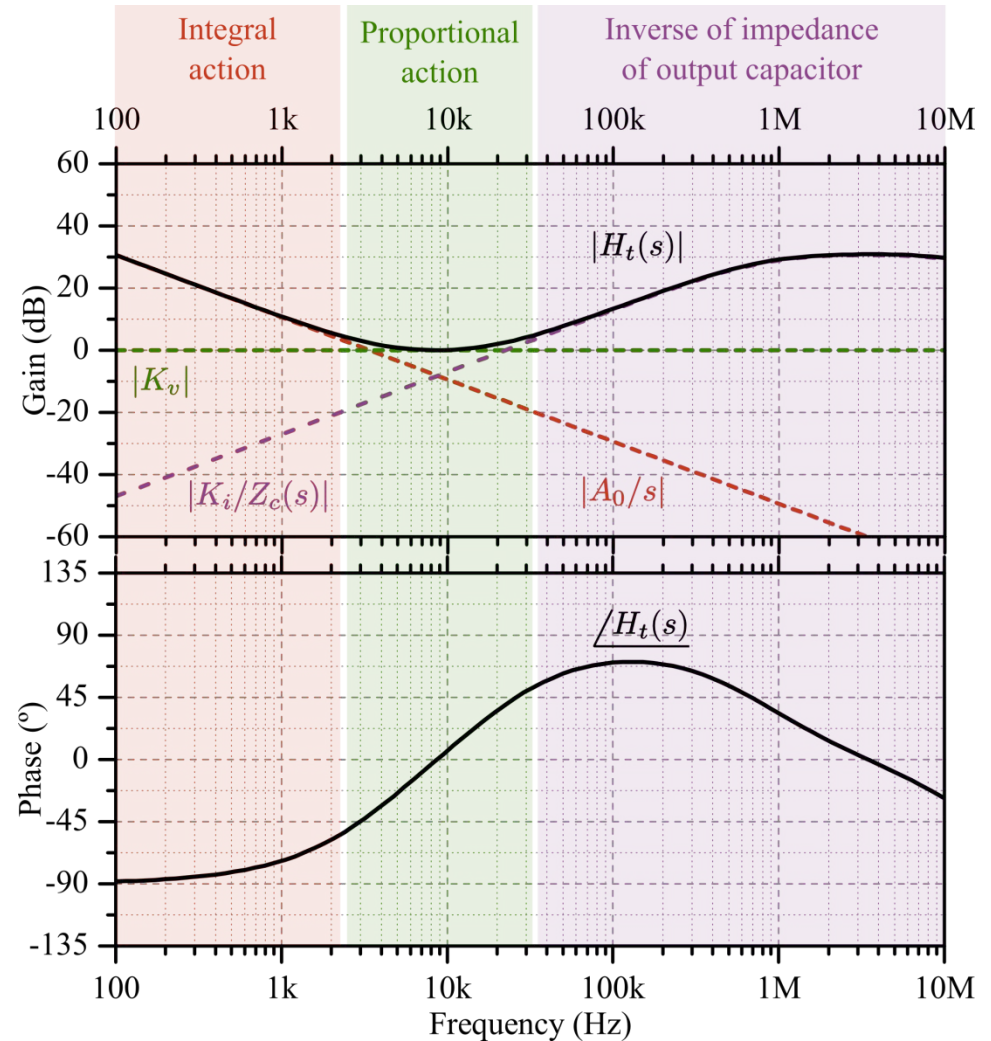
High-Q cap ($Q > 0.5$)

If $\Delta B < \omega_c/10$
 $v^2 i_c$
type-III voltage mode (approx)

If $\Delta B > \omega_c/10$
 $v^2 i_c$

Low-ESR zero cap

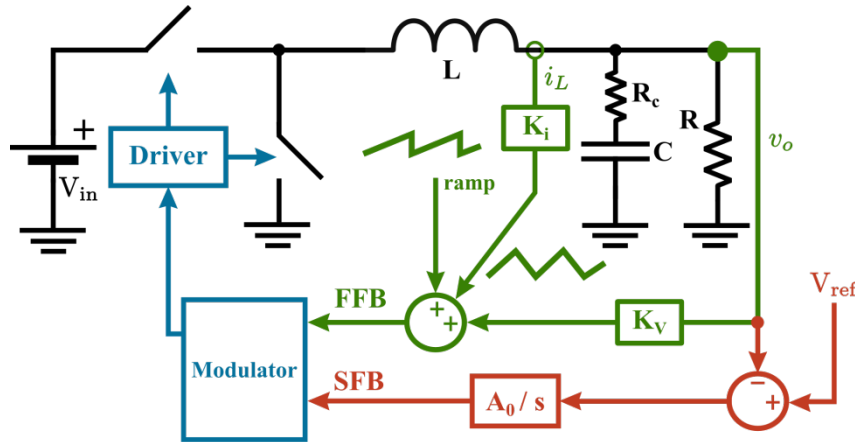
$v^2 i_c$
 v^2
type-II voltage mode



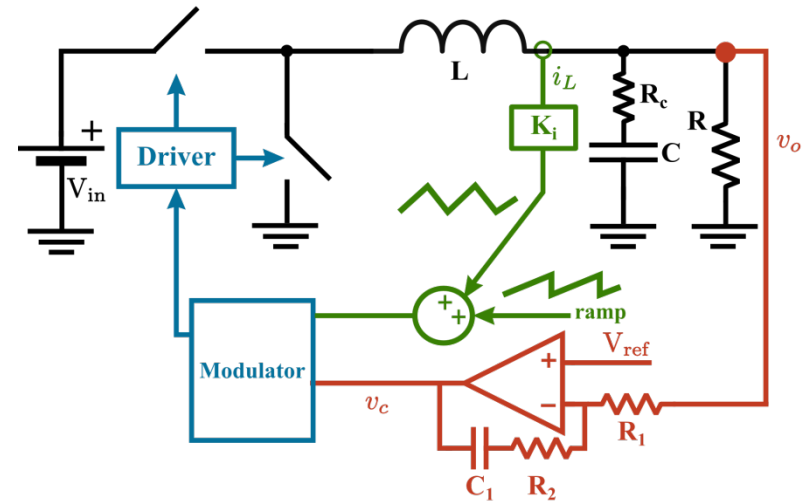
v¹ concept

And what happens to the v² control compensated with the inductor current?

v² compensated with the inductor current



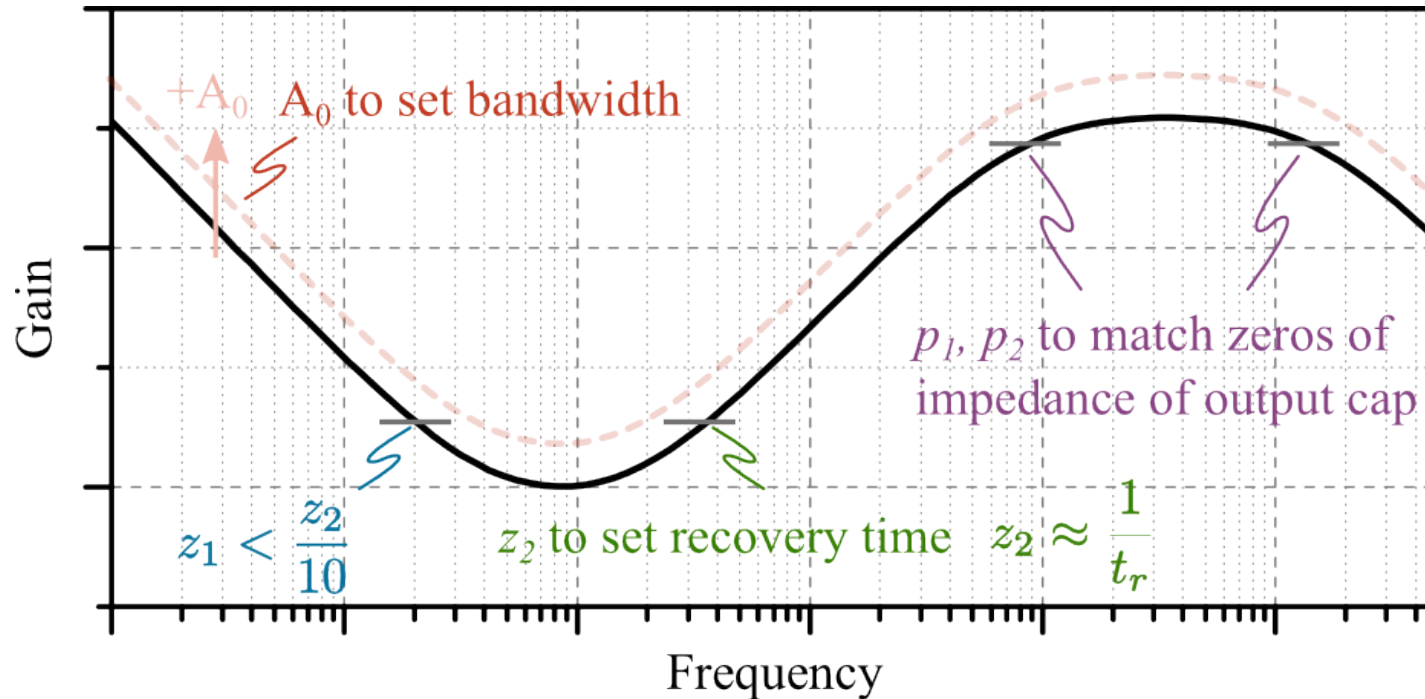
Type-II current mode



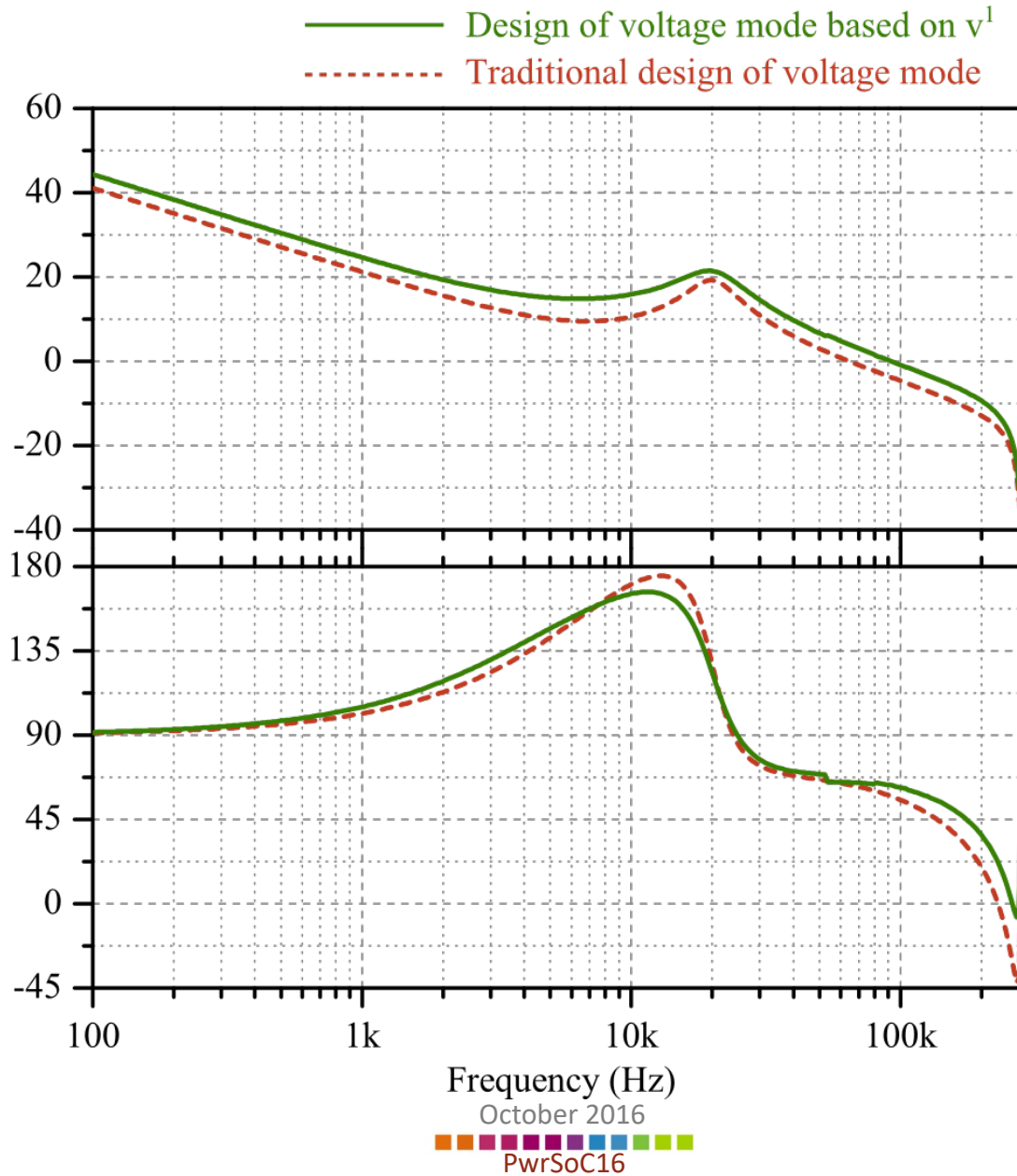
- As seen, the v² control is equivalent to a type-II control. In a Buck converter, the control relies on the ESR of the output capacitor to boost the phase of the loop gain.
- If the ESR is not dominant in the output voltage ripple, the phase margin is poor because the type-II controller cannot add any phase and the response is oscillatory or unstable.
- The v² control is commonly compensated with the inductor current for improved response for non-dominant ESR capacitors. What we are essentially doing is turning the v² control into a conventional current mode control that can now be regulated with a type-II controller.

v¹ concept: design guidelines

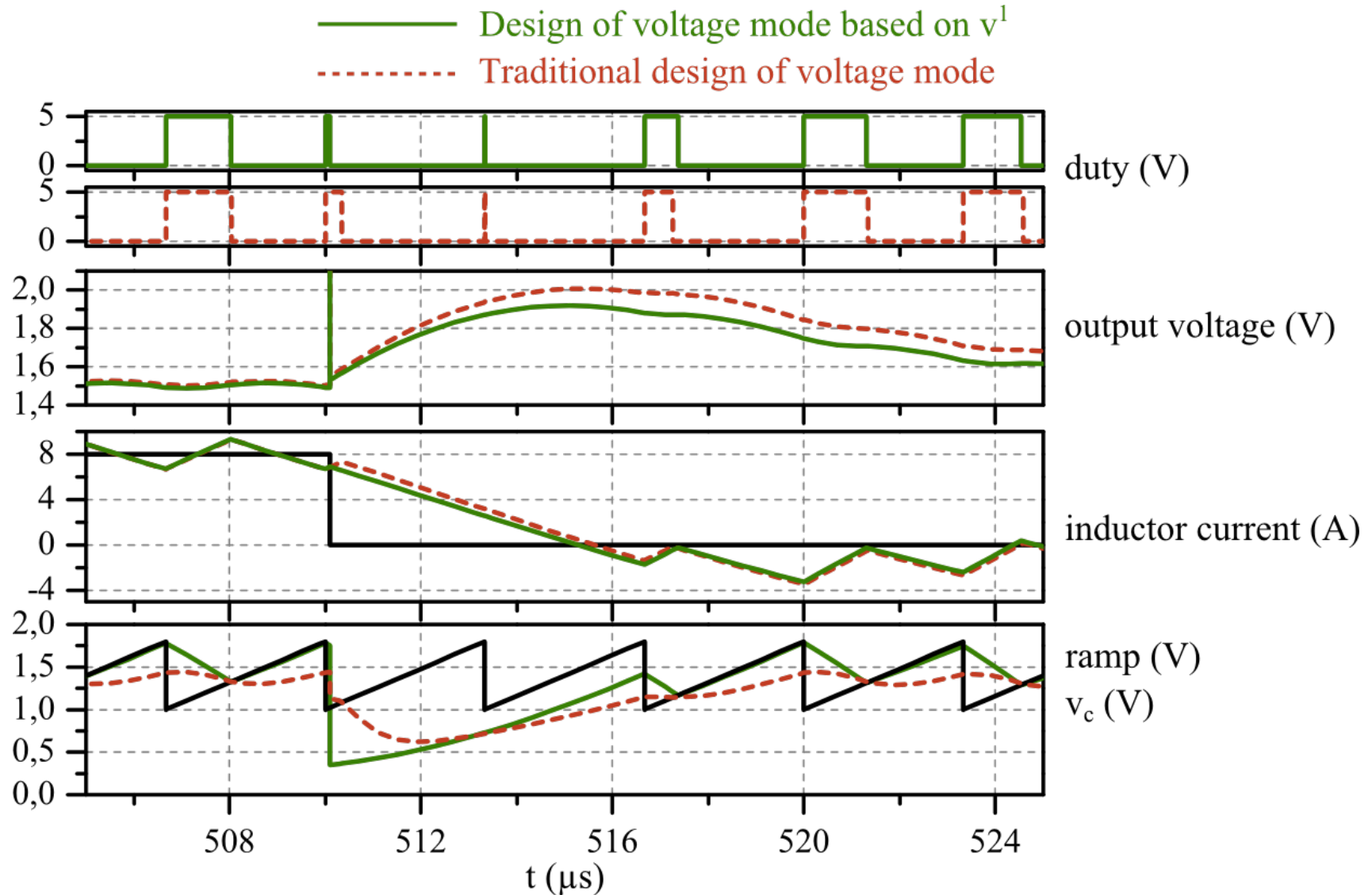
Proposed design of a type-III voltage mode control based on the v¹ concept



Comparison of traditional VMC design and V1 concept



Comparison of traditional VMC design and V1 concept



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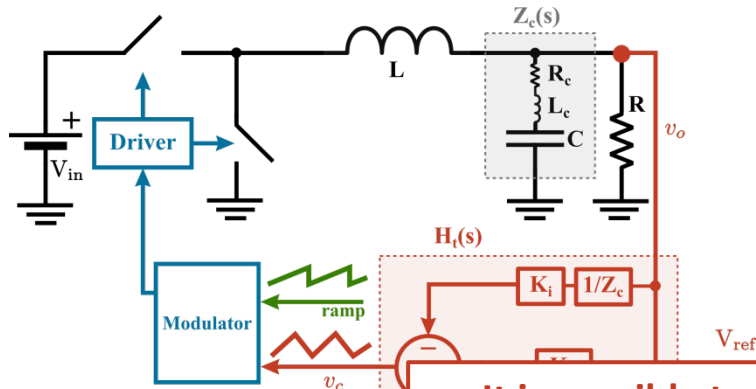


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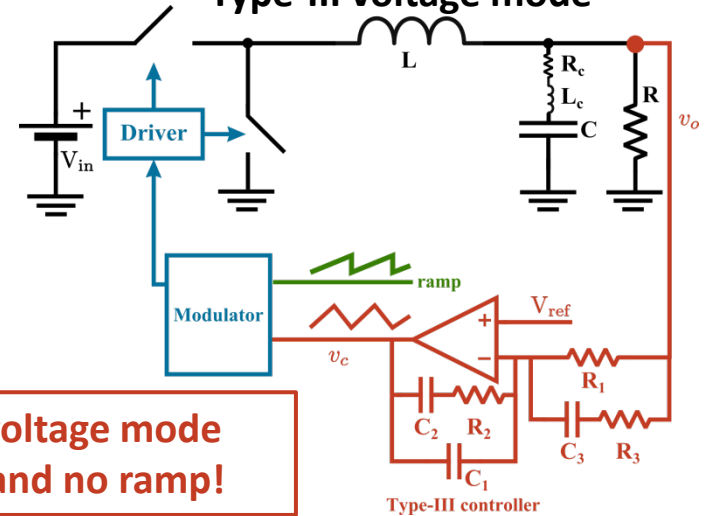
v¹ concept

Low-Q output capacitor

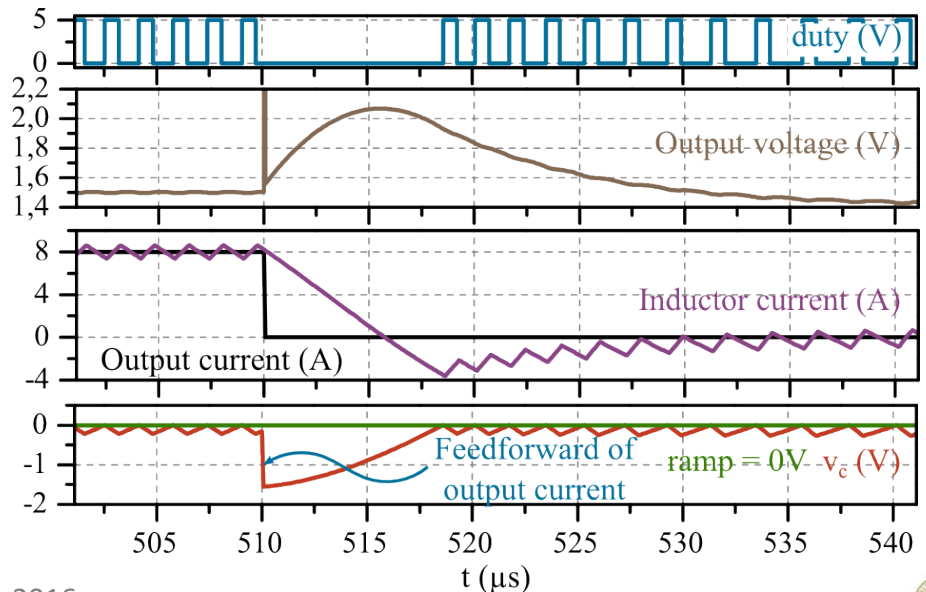
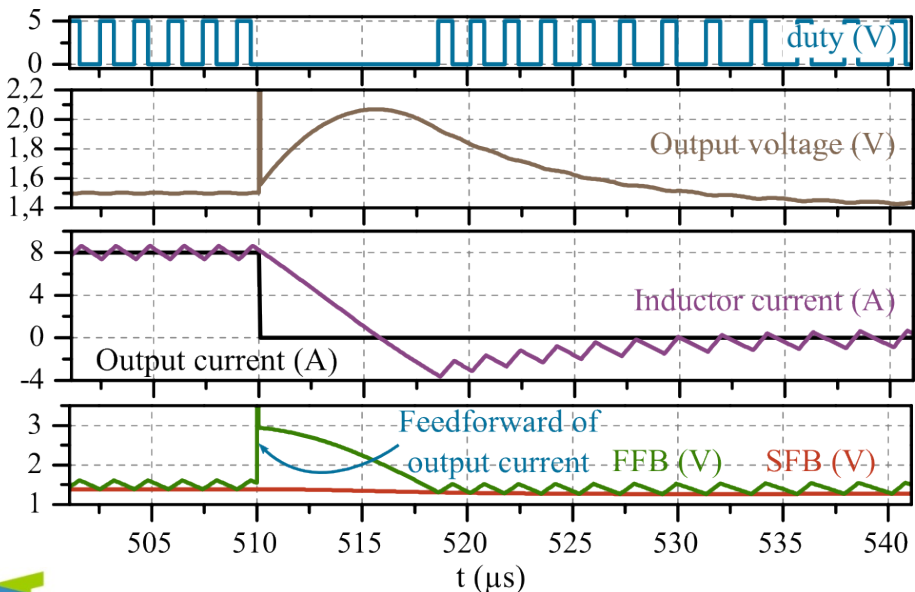
V²i_c reordered



Type-III voltage mode



It is possible to modulate this voltage mode control with constant on-time and no ramp!



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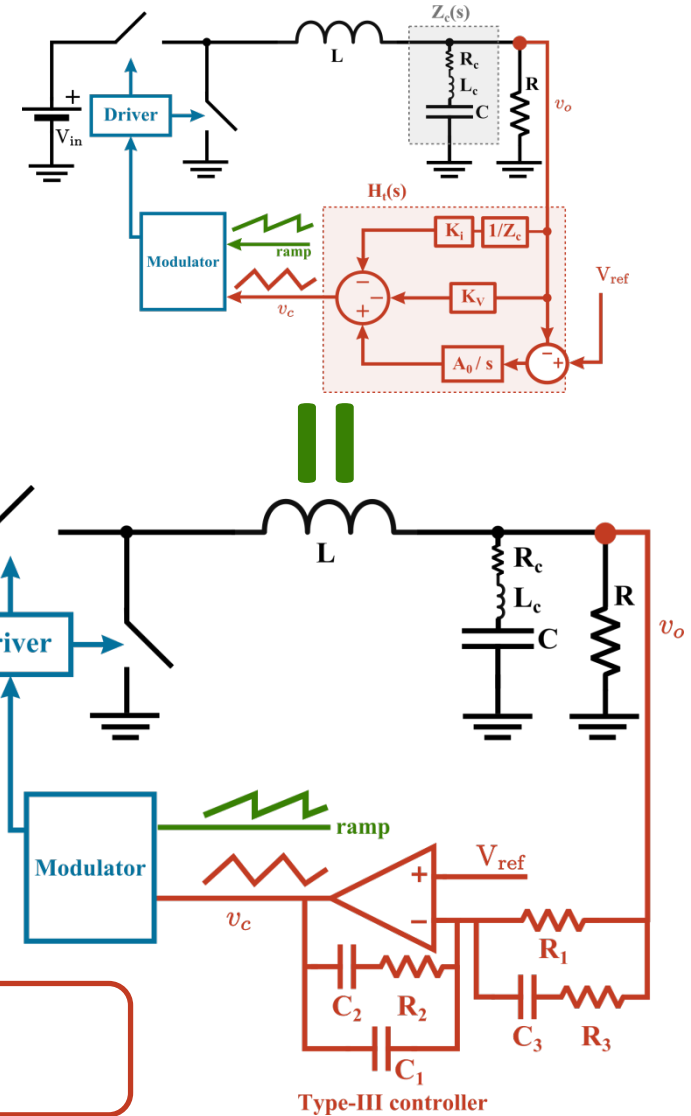
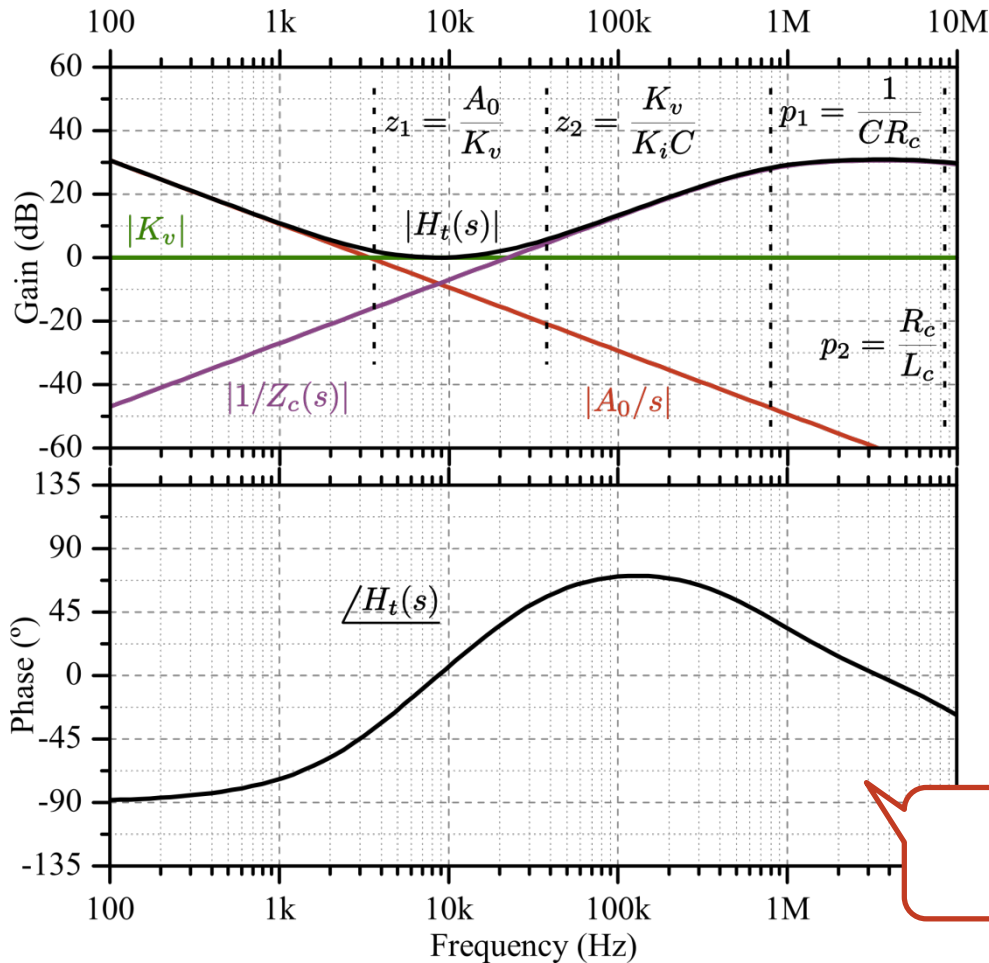


PwrSoC16

v¹ concept

Low-Q output capacitor

$$H_t(s) = A_o \frac{(1 + s/z_1)(1 + s/z_2)}{s(1 + s/p_1)(1 + s/p_2)}$$



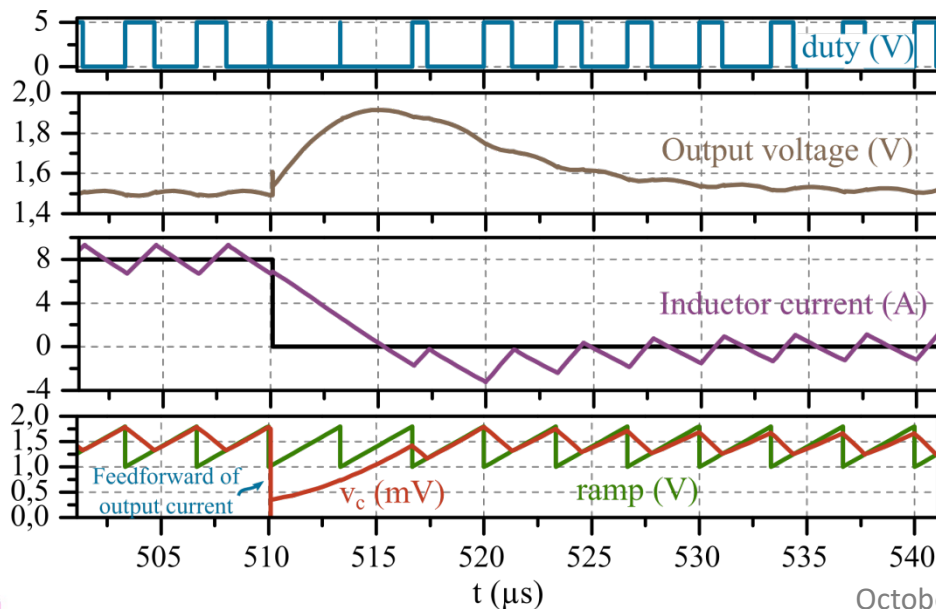
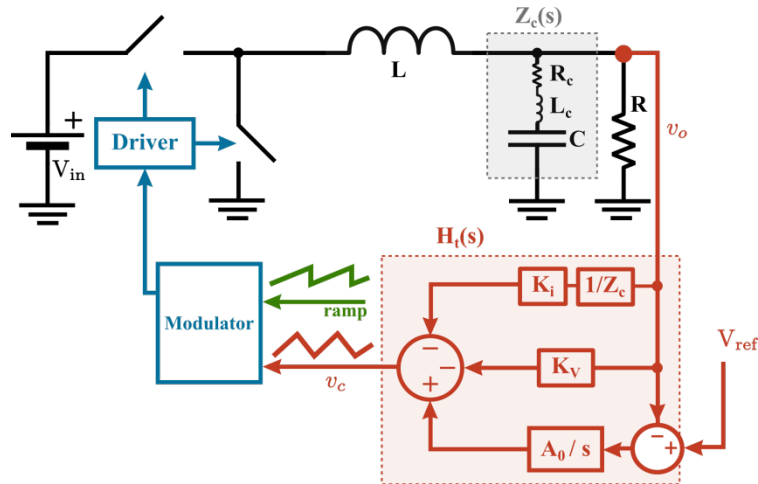
Type-III controller

Type-III controller

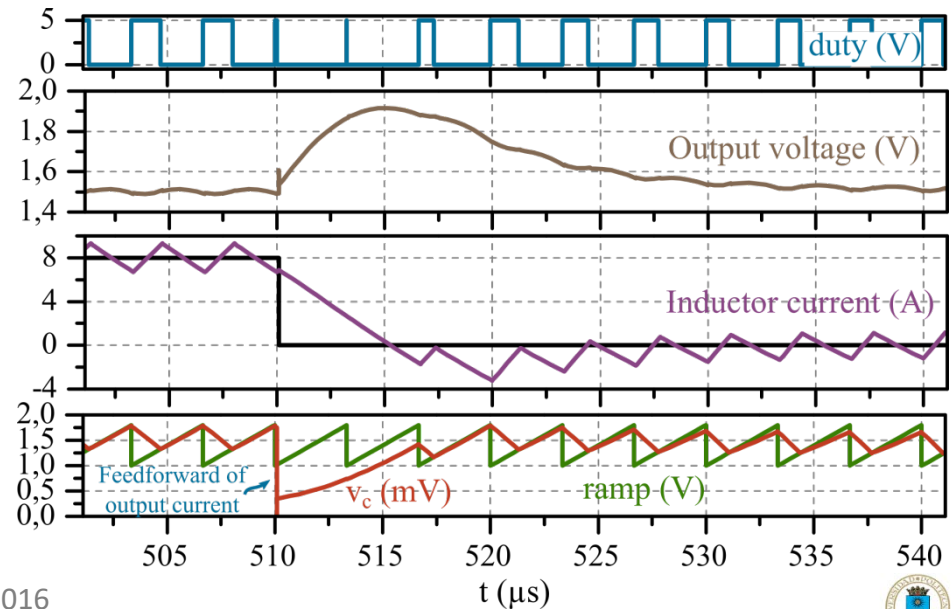
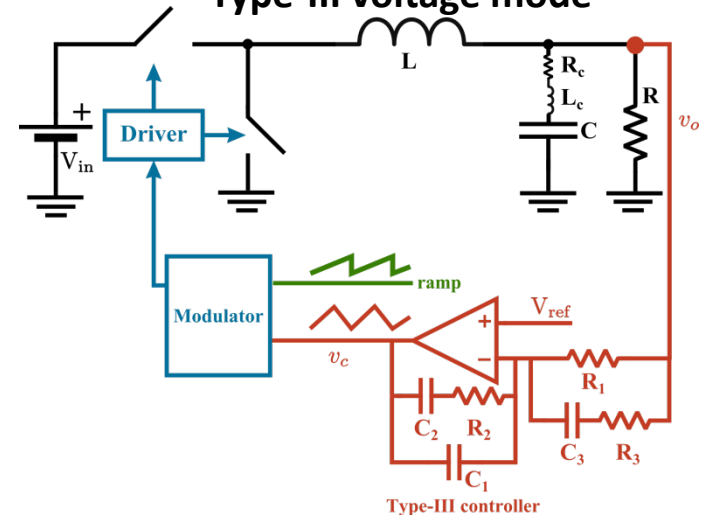
v¹ concept

Low-Q output capacitor

V²i_c reordered



Type-III voltage mode

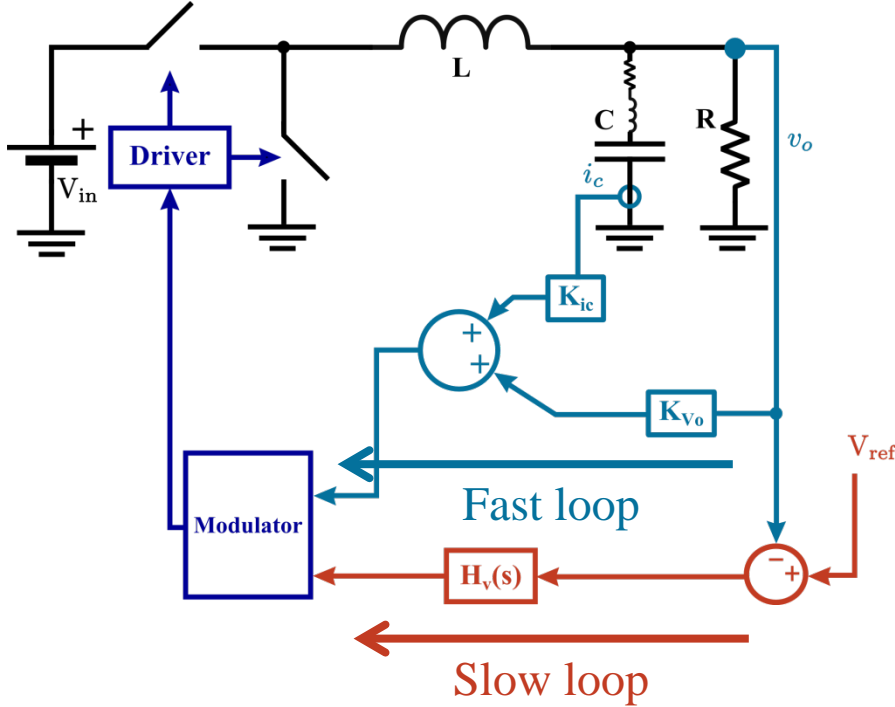


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Introduction: v^2i_c

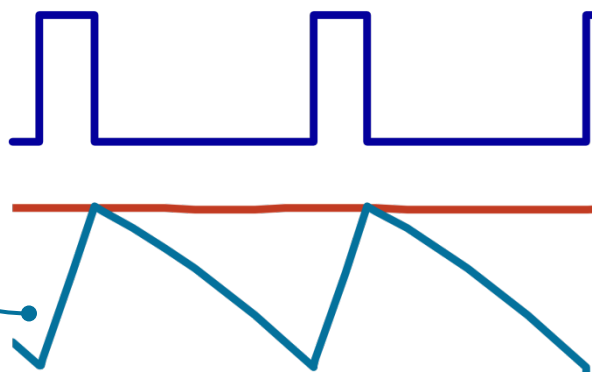


Fast loop:

- Responsible for fast dynamic response

Slow loop:

- Responsible to regulate tightly the output voltage.
- Very low bandwidth



In steady-state, it behaves like a current mode control