Analyzing Power-Clock Network Parasitic on Adiabatic Logic

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1. Context and objectives

Adiabatic logic is novel architecture design style to reduce the power consumption of digital cores. Its main characteristic is that the power supply is also the clock signal. A lot of work on different adiabatic logic families has been done but the impact of the power supply and the power-clock network still remains to be studied. In this work, we investigate the power-clock network effect on adiabatic energy dissipation. Experiments, based on simulation, show that the power-clock network has an effect on the magnitude and the phase shifting of each node voltages, which eventually leads to higher energy dissipation.

Advantages of the adiabatic logic:

- The energy loss is **proportional** to the frequency. $E = \frac{\pi^2}{8}\frac{R_{GATE}C}{\mathbf{T}}CV_{DD}^2$
- The energy stored in the capacitor is **recovered** in the power supply.

Issues:

- The energy loss is dependent of the gate resistance.

Objectives

How does the power-clock network impact on the energy efficiency?
Can we derivate an expression to quantify its impact?

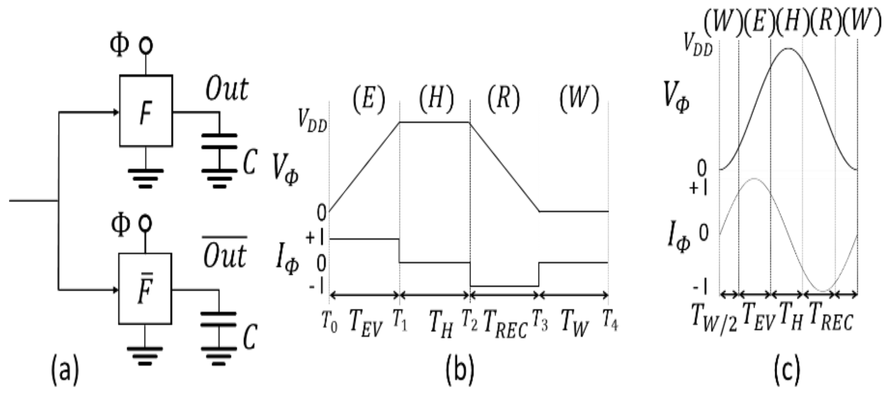

Fig.1 (a) Adiabatic Logic Gate,
(b) Voltage and current of a 4-phases adiabatic clock,
(c) Sinusoidal power-clock

2. Modelling

Power-Clock Network Model

To model the impact of the power clock network (PCN), we describe the network as a resistive and capacitive network. The power clock is an ideal sinusoidal signal(fig.1.c), and the adiabatic logic gate is modeling as the on-state resistance and the output capacitor of an adiabatic buffer.

Energy Loss Model

We derive the voltage and the current from each node of the analytical model (fig.2), then we derive the resistor voltages and finally we compute the .

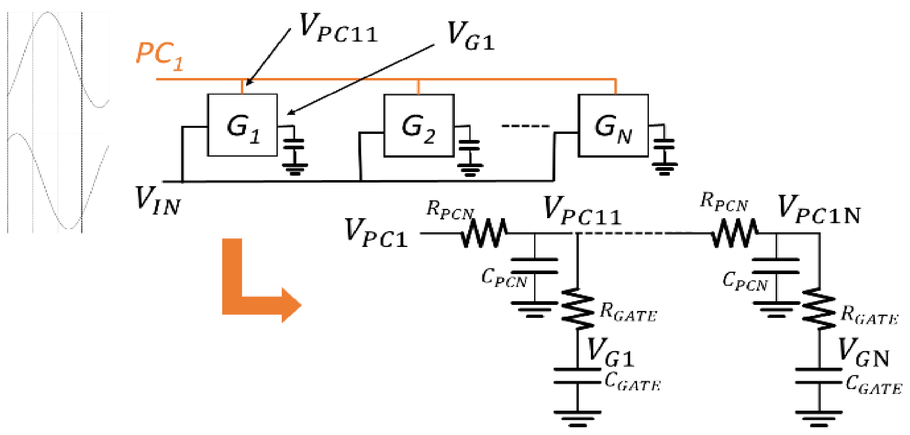

Fig.2 Modelling of one power-clock of an ideal pipeline

3. Results

3.1 Energy loss

In fig.4, the energy dissipation of 1000 gates with an on-state resistance of 100Ω and a gate capacitance of 7fF. The power-clock is running at 50Mhz. Experiments highlight three points:

- The energy dissipation is proportional to the number of gates.
- The most dissipating resistor is always the parasitic resistor which connect the power-clock supply and the first gate.
- The parasitic resistance has an higher impact on the energy dissipation than the parasitic capacitance.

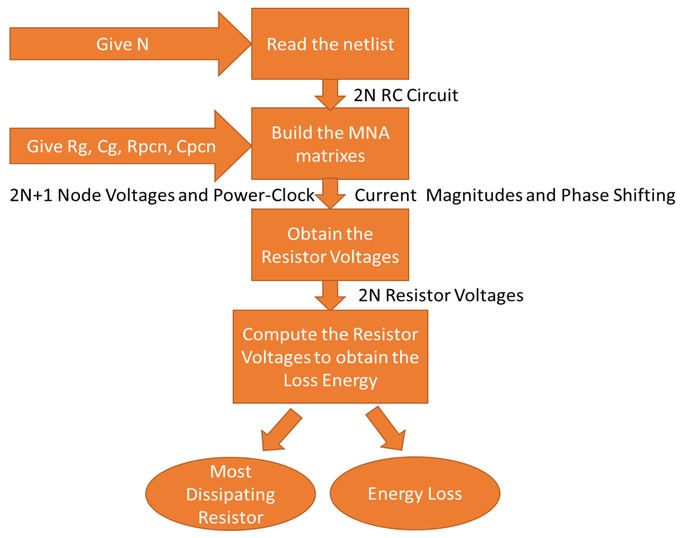

Fig.3 Process to determine the energy dissipation

3.2 Conclusion

We have analyzed the impact of the Power Clock Network (PCN) on an analytical model regardless of the value of the PCN parasitic. In order to design very low power adiabatic logic circuits, designers have to give the same consideration to the design of the PCN for limiting the energy loss than the design of the Power-Clock supply.

3.3 Key contributions

- We describe the Power-Clock Network, its gates and its Power-Clock supply as a small signal circuit.
- We build a MNA matrix to obtain each node voltage from this circuit.
- We derive the loss energy thanks to the resistor voltages computing from the node voltages.

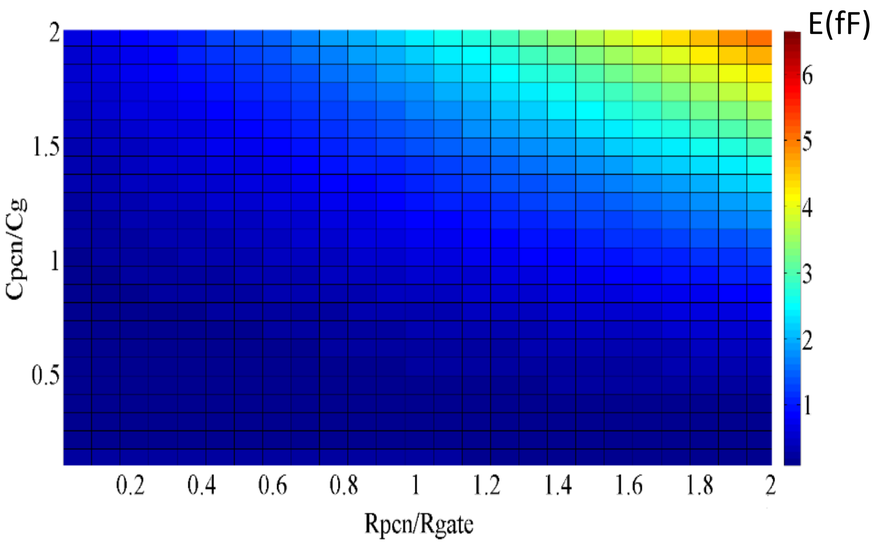

Fig.4 Energy Loss vs the PCN Parasitic

4. Ongoing work and perspectives

- Effect of the Power-Clock Network with the four networks.
- Effect of the non ideal power supply on the energy efficiency of an adiabatic logic circuit.

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