Integrated Boost Converter for Low-Voltage, Low-Power Energy Harvesting Source

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Inductor-on-silicon Design for Energy Harvesting Power Conversion

The purpose of this work is to investigate the possibility of using integrated inductors-on-silicon in DC-DC converters for low-voltage, low-power energy harvesting (EH) applications. This involves:

- Examining existing power conversion solutions for low power EH sources such as dye-sensitised solar cells (DSSCs).
- Proposing 2 different inductor structures, racetrack [1] and solenoid inductor [2], as seen in Figure 1.
- Examining the loss breakdown and efficiencies of the inductors and the overall efficiency of the boost converter.

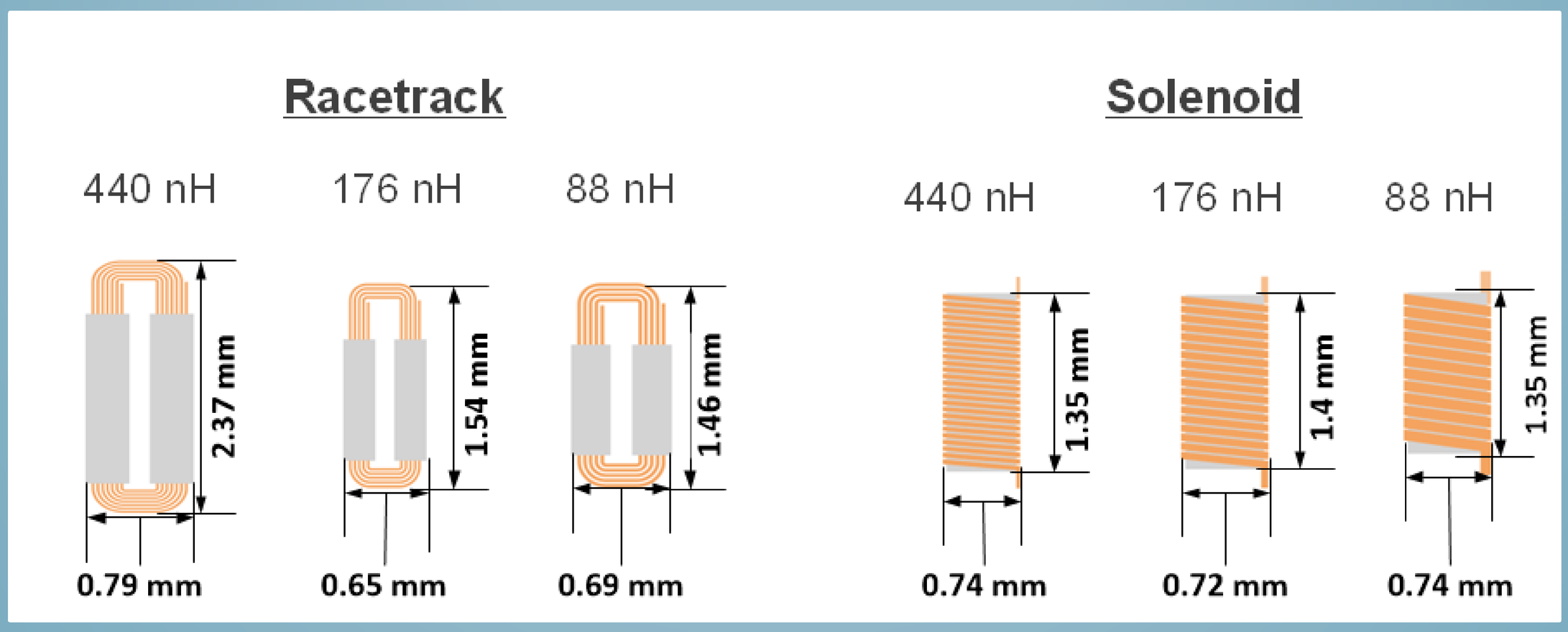

Figure 1: Comparison of racetrack and solenoid inductors for various inductance values.

Converter Operation

Inductor based switching converters have been found to have high efficiencies, up to 77%, for low-power, low-voltage energy harvesting sources. However, to date, the inductor is a limiting factor to full integration in power-supply-on-chip due to the relatively low switching frequencies considered (< 1MHz) and therefore the high inductance values required.

Due to the low-power levels involved in an energy harvesting powered system, measures to improve conversion efficiency include discontinuous conduction mode (DCM) of the inductor and burst mode operation of the converter. Burst mode control is often based on maintaining the source voltage at its maximum power point (MPP) as shown in Figure 2 for a DSSC source. Current mode control is applied to ensure DCM operation during the converter on-time.

The combination of DCM and burst mode operation enable the selection of a smaller inductor than with CCM converter operation, because the ripple current is very high relative to the source current.

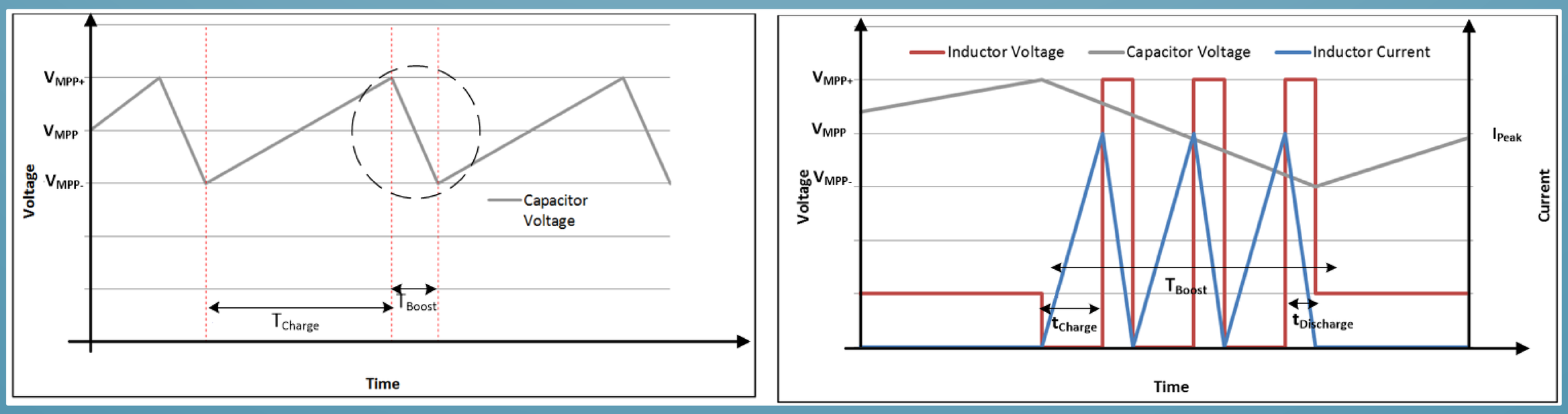

Figure 2: Boost converter DCM operation (a) input capacitor voltage, (b) detailed circuit waveforms during T_{boost}.

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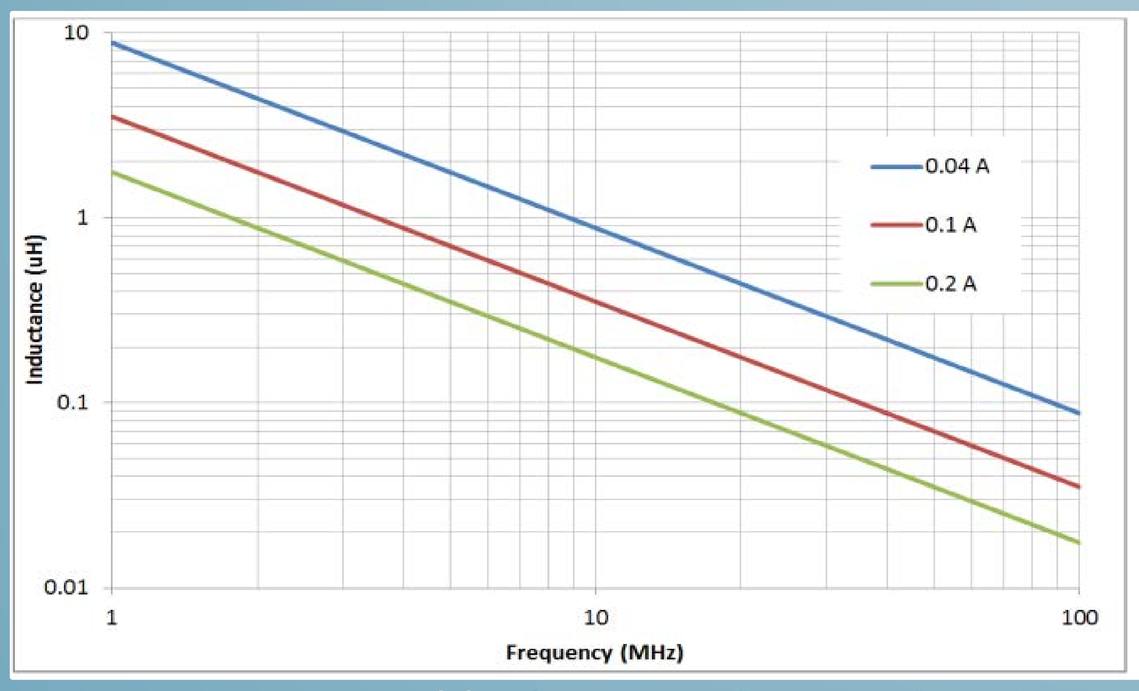
Inductor Designs

As discussed, by increasing the converter switching frequency and the peak current of the inductor, the inductance required is reduced. Figure 3 shows the inductance required for different peak inductor currents and switching frequencies to maintain boundary conduction mode for an input voltage of V_{in} = 0.4 V and an output voltage of V_{out} = 3.3 V with different peak current settings of a current controller.

It should be noted that due to burst mode operation, the source current, I_s, may be quite low relative to the peak current, ΔI; e.g. I_s = 1 mA for a 25 cm^2 DSSC. Therefore, magnetic saturation, B_{sat}, and AC winding and core losses tend to be limiting factors in inductor design. Figure 3 (b) shows design equations for the inductor where v_k is the core thickness to skin depth ratio at the switching frequency, f_{sw}; H_k is the AC magnetic field amplitude at the k^{th} harmonic; ρ_c is the resistivity of the core and ΔB_{pp} is the peak-to-peak core flux density.



Inductor Losses [1]

- $\Delta B_{max} = B_{sat} \cdot \frac{\Delta I}{I_{dc} + {}^{\Delta I}/_{2}}$
- $P_{ac} = \sum_{k=1}^{k\,max} R_{ac,k}\ I_{k,rms}^2$
- $P_{dc} = R_{dc} . I_{dc}^2$
- $P_e = 2\frac{\rho_c .(C_w + D_h)C_1}{C_t} \sum_{k=1}^{k\,max} v_k \frac{\sinh(v_k) - \sin(v_k)}{\cosh(v_k) + \cos(v_k)} H_k^2$
- $P_{hys} = K . f_{sw} . (\frac{\Delta B_{pp}}{2})^{\beta} . V_C$

Figure 3: (a) Inductance vs. frequency for various peak inductor currents, (b) inductor-on-silicon design equations.

Comparison of Designs

Table 1 shows key parameters for three inductor designs each for racetrack and solenoidal structures, corresponding to peak currents of 40, 100 and 200 mA at 20 MHz. To enable a fair comparison between inductors the winding thickness/winding spacing of the racetrack inductor is set to 30 µm/ 15 µm and the solenoid is set to 15 µm/ 15 µm. The racetrack inductor has a single core lamination with a maximum thickness of one skin depth (4.5 µm) while the solenoid inductor has two core laminations (up to 2 × 4.5 µm). This means that both the racetrack and solenoid inductors are similar in terms of processing steps required to produce a core and overall device height.

All inductors were optimised for full load efficiency within a fixed footprint area of 1 mm^2 with the exception of the 440 nH racetrack inductor. The number of turns, winding width, core thickness, and core aspect ratio were optimised using the Ferrochip Design Studio.

An interesting point to note is that the 440 nH racetrack inductor cannot be achieved within a footprint area of 1 mm^2 due the required inductance and core material constraints.

Table 1: Key inductor parameters for the different structures and designs.

	Racetrack			Solenoid		
Inductance (nH)	440	176	88	440	176	88
Footprint (mm^2)	1.87	1	1	1	1	1
DC Resistance (Ω)	0.942	0.89	0.339	1.31	0.525	0.24
Turns	7	5	5	26	18	12
Core Thickness (µm)	4.5	4.5	2.46	2.87	2.42	2.5

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Circuit Analysis

The inductor-on-silicon loss equations featured in Figure 3 are taken from [1] while the standard boost converter losses of Figure 4 include MOSFET conduction and switching losses.

Boost Converter Losses

- $P_{MOS\_cond} = I_{RMS}^2 R_{DS(on)}$
- $P_{pmos} = \frac{t_{sw,on} V_{out} I_{Peak} F_{sw}}{2}$
- $P_{nmos} = \frac{t_{sw,off} V_{out} I_{Peak} F_{sw}}{2}$

Figure 4: Equations for boost converter loss analysis.

Loss Analysis

Figure 5(a) shows a breakdown of the inductor losses and (b) the inductor and boost converter efficiencies operating in DCM burst mode with the inductors of Table 1. It is clear to see that the solenoid inductor outperforms the racetrack inductor for all inductance values, peak current values and footprint sizes considered.

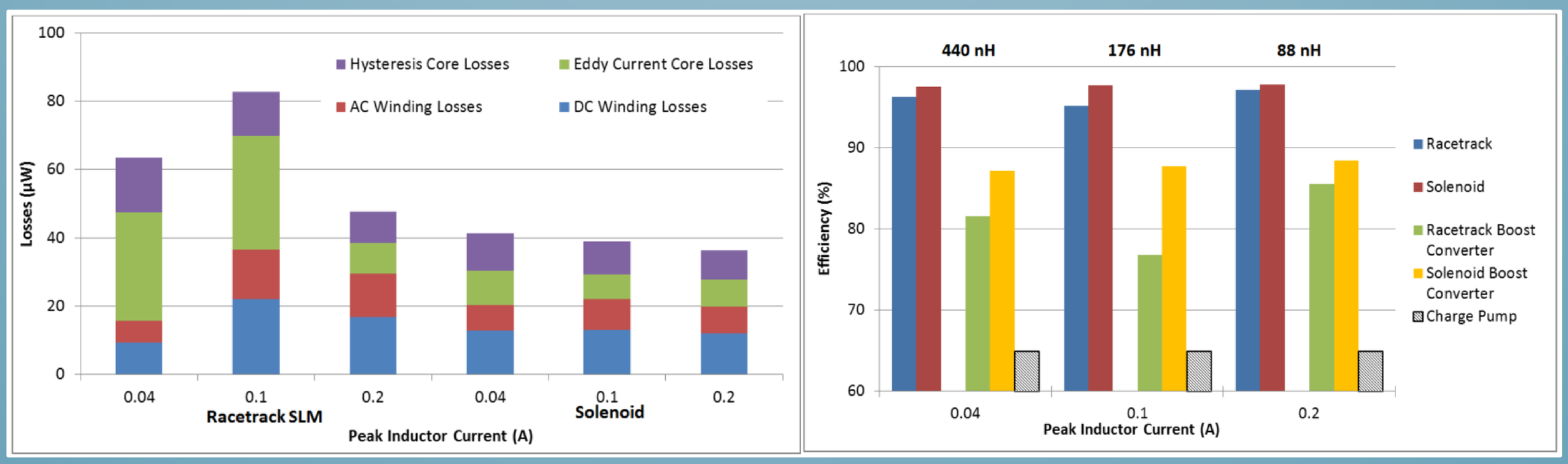

Figure 5: (a) Inductor loss breakdown and (b) inductor efficiency and overall converter efficiency vs peak current.

Conclusions

The efficiency values shown in Figure 5(b) show that a boost converter featuring a racetrack or solenoid inductor can achieve higher efficiency values than the existing boost converters efficiency (with discrete inductors) of 72-77%, and the efficiency of other on-chip solutions such as a charge pump design with an efficiency of 50-65%. Solenoidal designs are superior to racetrack designs, mostly due to their improved core performance within a footprint of 1 mm^2.

Future work will investigate the feasibility of integrating the inductors with suitable semiconductor switches.

References

[1] C. Feeney, N. Wang, S. Cian O Mathuna, and M. Duffy, “Design Procedure for Racetrack Microinductors on Silicon in Multi-MHz DC-DC Converters,” *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6897–6905, 2015.
[2] D. W. Lee, K. P. Hwang, and S. X. Wang, “Design and fabrication of integrated solenoid inductors with magnetic cores,” *Proc. - Electron. Components Technol. Conf.*, pp. 701–705, 2008.