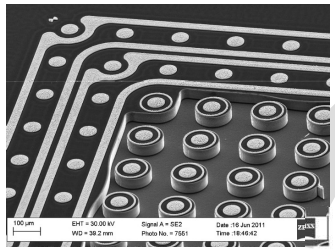
Control and Implementation Aspects of a Multiphase Inductor-Based FIVR in 14 nm Bulk CMOS for Microprocessor Applications

Project info

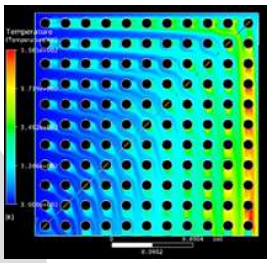
- EU FP7 project
  - Project: 619488
- Begin: Jan. 2014
- End: June 2017

CarrICool

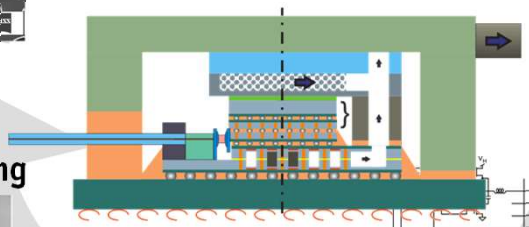
WP5: Interposer platform



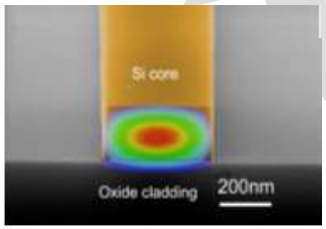
WP2: Heat removal



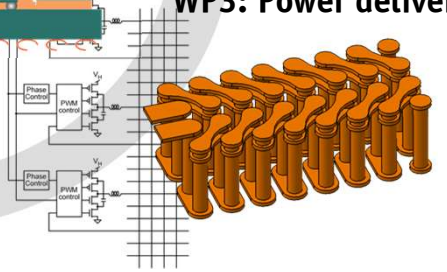
WP6: Demonstrator



WP4: Optical signaling



WP3: Power delivery



Project Partners:

- **IBM Research Zurich**, Switzerland
- **Tyndall National Institute**, Ireland
- **Fraunhofer**, Germany
- **ETH Zurich**, Switzerland
- **IPDiA**, France
- **Optocap**, Scotland
- **TU Chemnitz**, Germany
- **AMIC**, Germany

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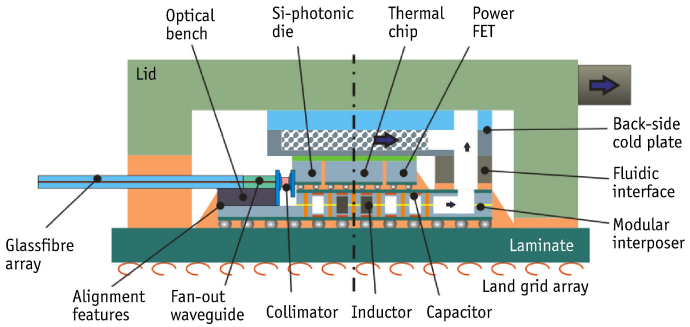
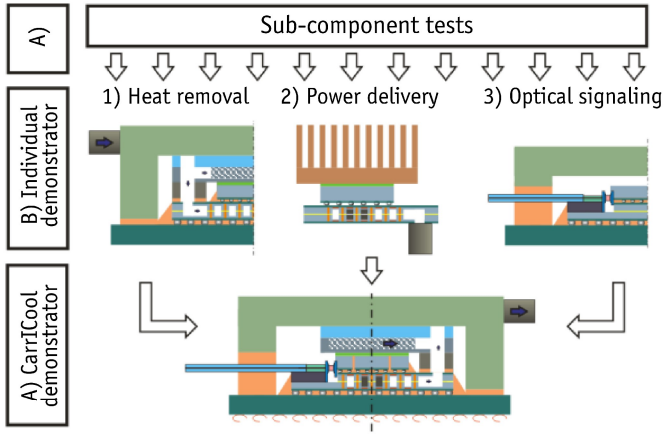
[1] Power Electronic Systems Laboratory (PES), ETH Zurich, Zurich, Switzerland
[2] IBM Research, Ruschlikon, Switzerland

CarrICool project objectives

CarrICool Demonstrator



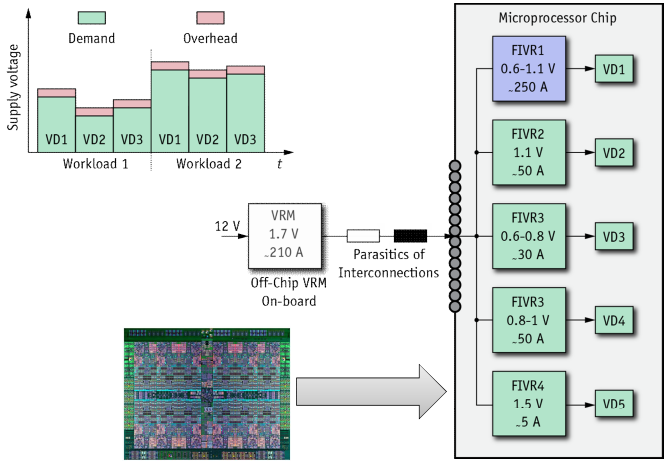
Individual Subcomponents



Main Research Challenges

- **Power Delivery**
  Highly granular voltage conversion using distributed on-die buck converters with interposer integrated passives.
- **Heat Removal**
  Increasing heat removal and improving device reliability.
- **Optical Signaling**
  Cost-effective and robust optical coupling using precise MEMS processing on the silicon interposer.
- **Interposer Platform**
  Improving interconnect density and reducing stress in solder balls and back-end layers of the IC stack.

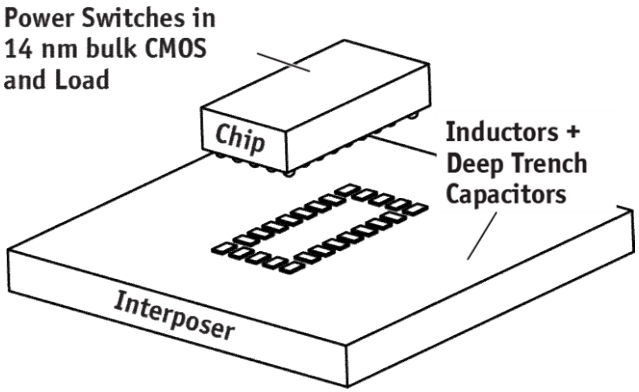
Granular Power Delivery



Power Converter Research Aspects

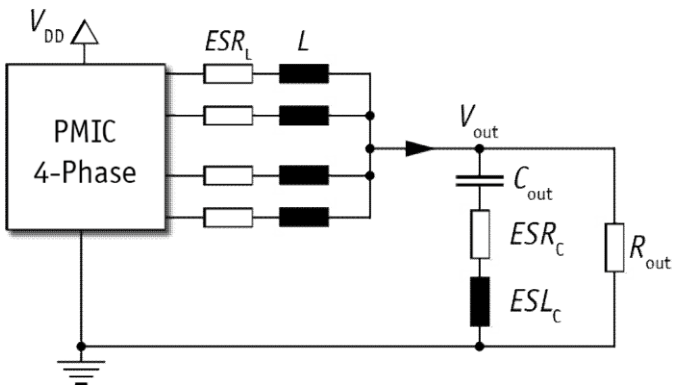
- **Power Management Integrated Circuit**
  - Implemented using GlobalFoundries' 14 nm bulk CMOS technology (FinFETs)
  - Dynamic DC voltage conversion
  - High efficiency
  - Possibility of operation with different inductors
- **Interposer Platform**
  - 3D inductors using TSVs and magnetic core material
  - Deep Trench Capacitors
  - Process compatibility, reliability and mechanical integrity of all the packaging elements involved.

Chip On Interposer Platform

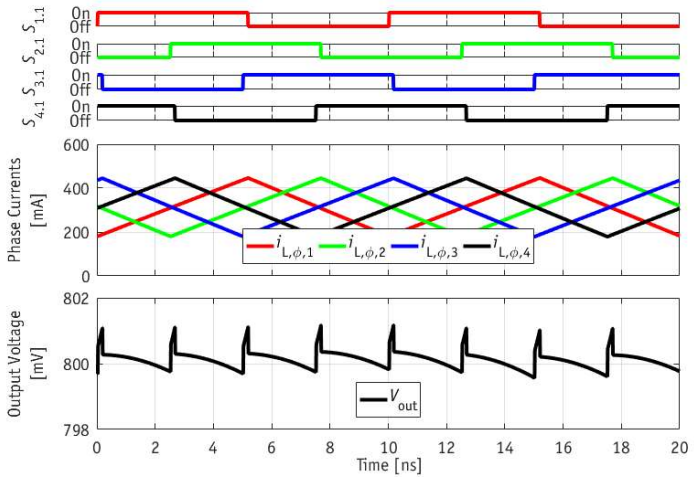


Power Delivery and Control Objectives

Converter Topology



Steady State Waveforms



Control Requirements

- Fast transient recovery
- Robust and stable voltage regulation
- Adaptive Voltage Positioning
  (Requires knowledge of the output current)
- Zero steady-state output voltage error
- Small area consumption
- Possibility of operation with different inductor types in the presence of tolerances/parasitics

Converter Specifications

Parameter		Value
V_{in}	Input Voltage	1.6 V
V_{out}	Nominal Output Voltage	0.8 V
$V_{out,min}$	Min. Output Voltage	0.6 V
$V_{out,max}$	Max. Output Voltage	1.1 V
P_{out}	Output Power	1 W
N_ϕ	Number of Phases	4
f_{sw}	Switching Frequency	100 - 150 MHz

Switches/Passives Parameters

Parameter		Value
L_ϕ	Phase Inductance	14 nH
$ESR_{L,\phi}$	Inductor DC Resistance	81 mΩ
C_{out}	Output Capacitance	40 nF
ESR_C	Capacitor ESR	36.2 mΩ
ESL_C	Capacitor ESL	7.6 pH
$R_{DS,ON}$	Switches On-Resistance	94 mΩ

Transient Performance Requirements

Parameter		Value
ΔV_{ref}	Maximum voltage reference step	500 mV
$t_{sett,ref}$	Max. settling time for ΔV_{ref} = 500 mV	100 ns
ΔI_{load}	Maximum load current step	625 mA
$t_{sett,load}$	Max. settling time for ΔI_{load} = 625 mA	70 ns
$V_{droop,load}$	Max. voltage droop for ΔI_{load} = 625 mA	70 mV

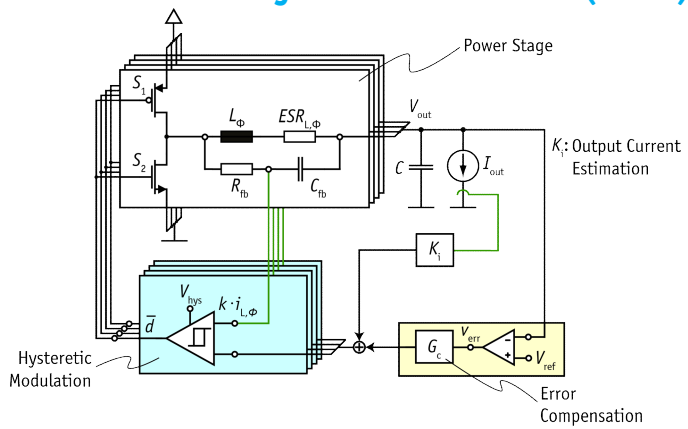
Control Scheme Selection

Control Scheme Comparison

	Requirement	CMHC	VMC	V_1I_L	$V_1I_L+I_o$
Steady State Performance	Fixed Frequency	-	+	+	+
	Current Sharing	+	-	+	+
Transient Performance	Load Current Step	+	-	-	+
	Reference Voltage Step	+	+	-	-
	Input Voltage Step	+	+	+	+
	Peak Current Protection	+	-	+	+
Implementation	Low ESR Cap Support	+	+	+	+
	Low BW Error Compens.	+	-	-	+
	Analog only	+	+	+	+

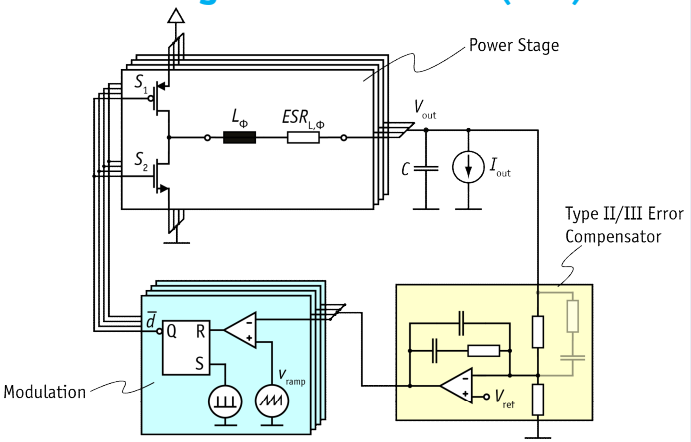
⇒ **The $V_1I_L+I_o$ controller is preferred** over CMHC since it inherently operates at constant switching frequency, which ensures high efficiency and is expected to allow for a more straight-forward filtering of EMI.

Current Mode Hysteretic Control (CMHC)



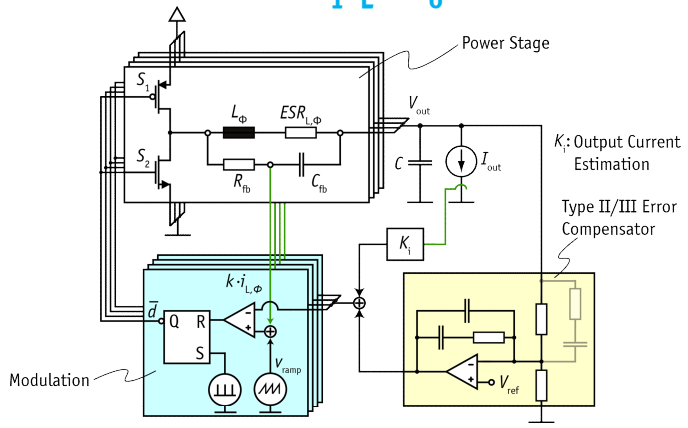
M. K. Song, M. F. Dehghanpour, J. Sankman and D. Ma, "A VHF-level fully integrated multi-phase switching converter using bond-wire inductors, on-chip decoupling capacitors and DLL phase synchronization," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014, pp. 1422-1425.

Voltage Mode Control (VMC)



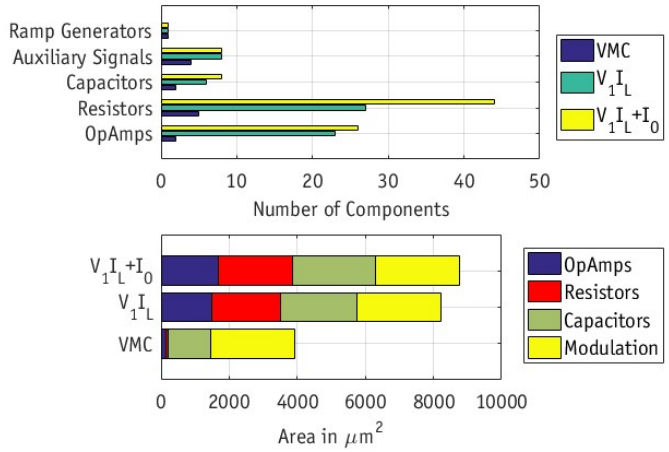
L. Cheng, Y. Liu and W. H. Ki, "A 10/30 MHz Fast Reference-Tracking Buck Converter With DDA-Based Type-III Compensator," in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2788-2799, Dec. 2014.

Multi-Phase $V_1I_L + I_o$ Control



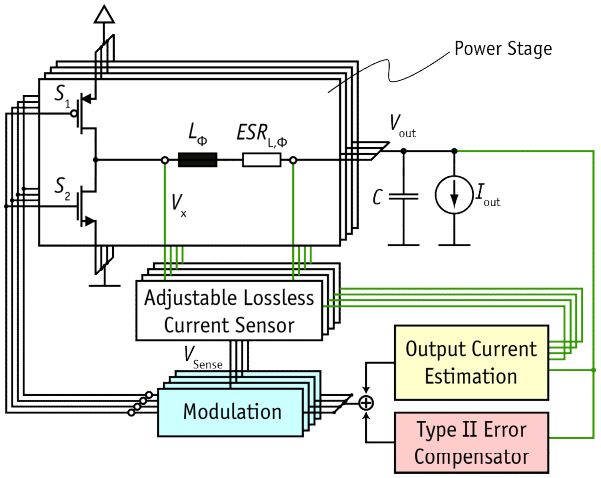
A. V. Peterchev and S. R. Sanders, "Load-Line Regulation With Estimated Load-Current Feedforward: Application to Microprocessor Voltage Regulators," in *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1704-1717, Nov. 2006.

Layout Effort/Area Consumption



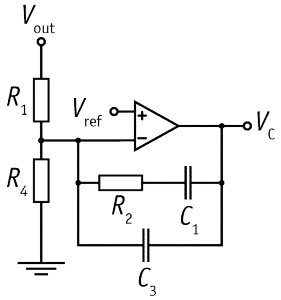
$V_1I_L + I_o$ Control Scheme Implementation

Implemented Control Scheme



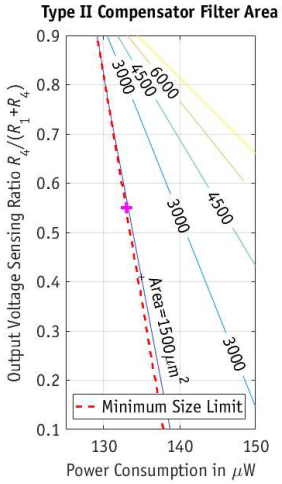
Type II Error Compensator

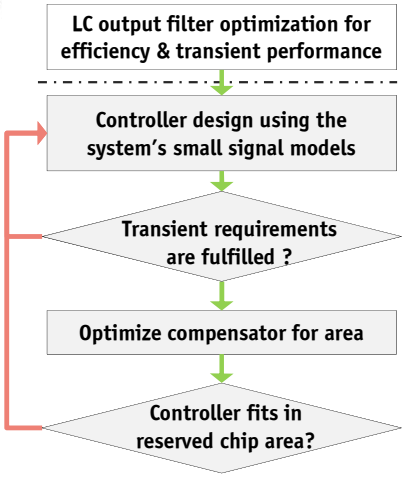
Transfer Function: $H(s) = \frac{V_C(s)}{V_{out}(s)} = \frac{1+sR_2C_1}{sR_1(C_1+C_3)+s^2R_1R_2C_1C_3}$



Parameter	Value
$BW_{ClosedLoop}$	9.67 MHz
Phase margin	100°
R_1	49 kΩ
R_2	31 kΩ
R_4	60 kΩ
C_1	5.3 pF
C_3	53 fF
Area	1300 µm²

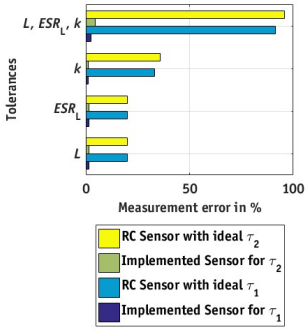
Compensator Design Flow

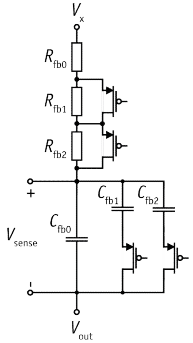




Adjustable Lossless Current Sensor

L, *ESR*, and coupling factor *k* of inductors are subject to ±20 % tolerances. The lossless current sensor can be configured to adapt to these tolerances, so that a considerable reduction of measurement error can be achieved.





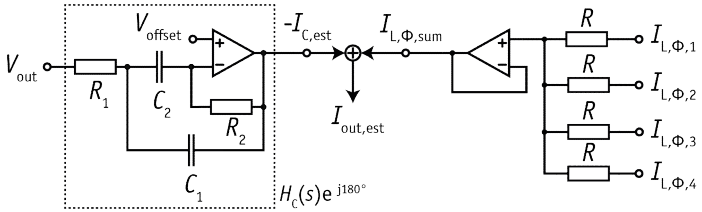
H. P. Forghani-zadeh and G. A. Rincon-Mora, "An Accurate, Continuous, and Lossless Self-Learning CMOS Current-Sensing Scheme for Inductor-Based DC-DC Converters," in *IEEE Journal of Solid-State Circuits*, vol. 42, no. 3, pp. 665-679, March 2007

Output Current Estimation

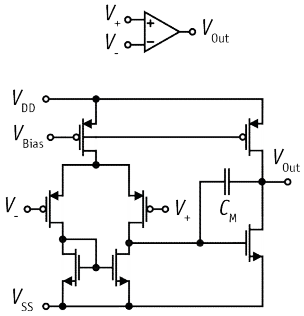
- $I_{out}(s) = \sum I_{phase}(s) - I_C(s) = \sum I_{phase}(s) - V_{out}(s) \cdot H_C(s)$
- Capacitor Current Transfer Function (2nd Order Bandpass):

$$H_C(s) = \frac{1}{Z_C(s)} = \frac{sC}{s^2 \cdot ESL_C \cdot C + s \cdot ESR_C \cdot C + 1}$$

- Implementation:



14nm EGFET OpAmp Design



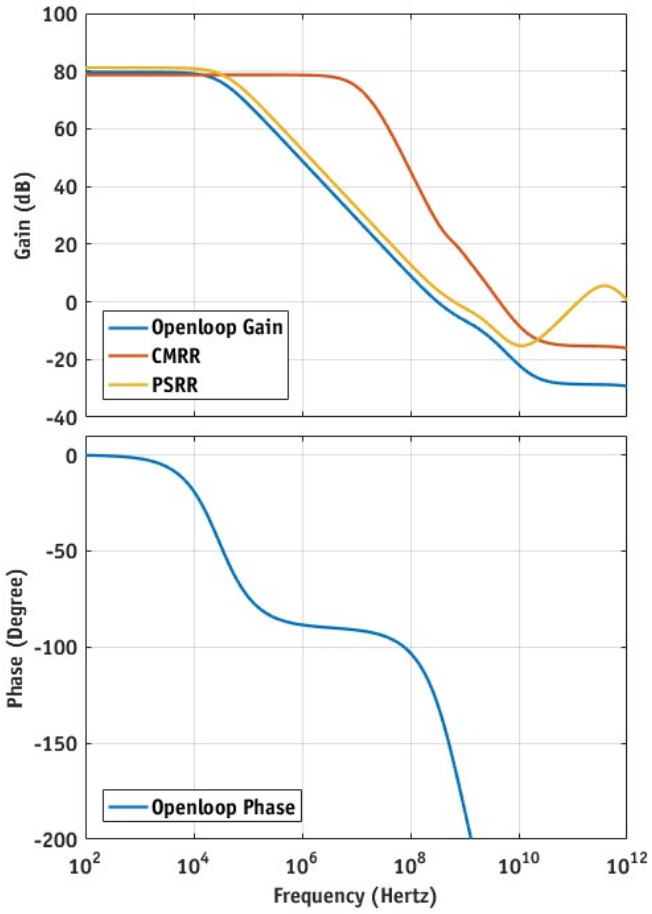
	Design 1	Design 2
A_{DC}	83 dB	
GBW	395 MHz	282 MHz
CMRR	69.6 dB	78.75 dB
PSRR	75 dB	104 dB
Devices	200 nm Gate EGFET	
Area	72 µm²	
Power	224 µW	128 µW

Tradeoff: Power Consumption ↔ Bandwidth

Both designs are used depending on the required bandwidth in each respective case.

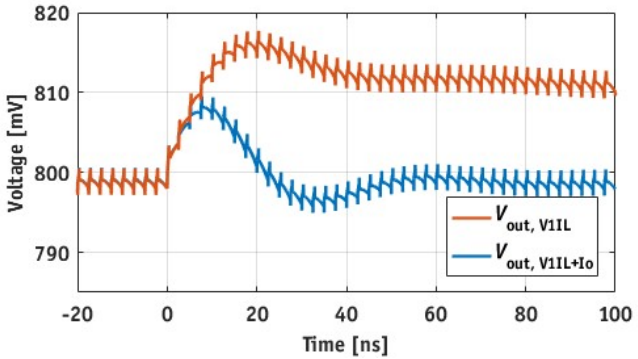
Simulation Results

OpAmp Characteristics



Small Load Current Transient

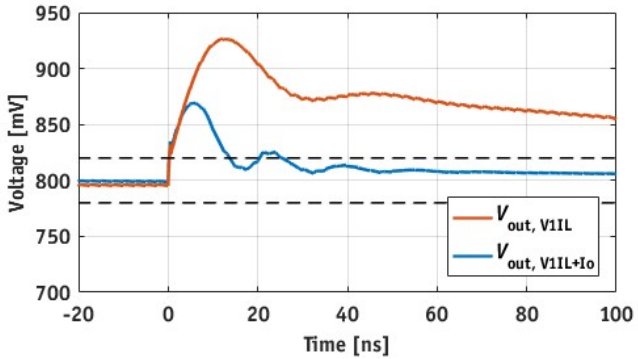
(62.5 mA/100 ps)



- Load current feedforward allows fast reaction

Large Load Current Transient

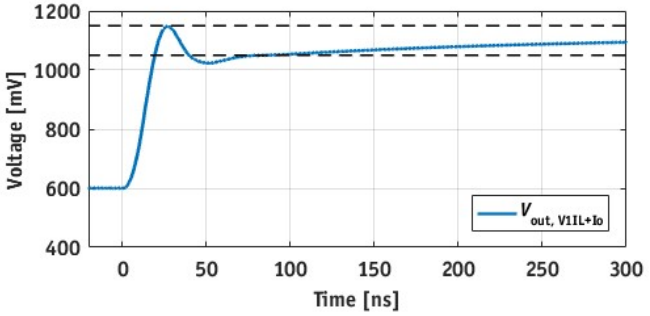
(625 mA/500 ps)



- Load step response meets requirements

Reference Voltage Transient

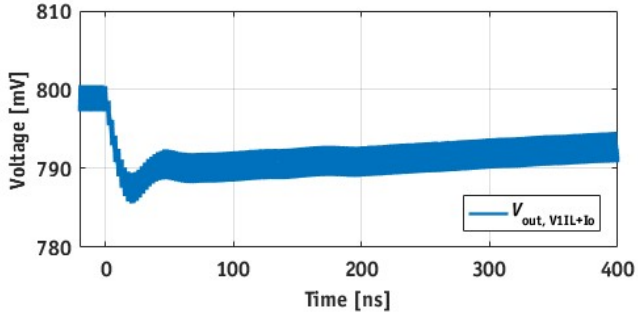
(500 mV)



- Meets transient performance requirements
- Possible improvement: (V_{ref} - V_{out}) feedforward

Input Voltage Transient

(200 mV)



- Possible improvements:
  (V_{ref} - V_{out}) or V_{in} or feedforward

Conclusions

Design	2012 [3]	2014 [2]	2016 [1]	This work
Process	45nm CMOS	22nm CMOS	65nm CMOS	14nm CMOS
Modulation	PWM	PWM	Hysteretic	PWM
f_{sw} / N_ϕ	80 MHz/4	140 MHz/360	200 MHz/4	100 MHz/4
L_ϕ	26 nH	unavailable	6.5 nH	15 nH
C_{out}	23 nF	4900 nF	3.77 nF	40 nF
V_{in}	1.8 V	1.7 V	1.2 V	1.6 V
V_{out}	0.7 V to 1.3 V	1.05 V to 1.7 V	0.6 V to 1.0 V	0.6 V to 1.1 V
$\Delta V_{out,pp}$	4 – 14 mV	3 mV	30 mV	1.2 mV
ΔV_{ref}	125 mV	unavailable	unavailable	500 mV
$t_{sett,ref}$	70 ns			80 ns
ΔI_{load}	600 mA/100 ps	8500 mA/1 ns	280 mA/120 ps	625 mA/0.5 ns
$t_{sett,load}$	26.66 ns	70 ns	14 ns	25 ns
$V_{droop,load}$	30 mV (with Loadline)	50 mV	78 mV	68 mV
Design	2012 [3]	2014 [2]	2016 [1]	This work

- **Design and implementation of $V_1 I_L + I_o$ in a mixed signal chip realized with 14nm technology**
- **Achievement of fast load current response of 25ns using a control bandwidth of 9.67 MHz**
- **Non-invasive output current estimation that can be used to achieve load-line regulation**
- **Technology related compensator optimization in terms of area and power consumption**
- **Design of an adjustable current sensor covering different inductors taking into account 20% manufacturing tolerance**

[1] M. K. Song, J. Sankman, J. Lee, and D. Ma, "A 200-mhz 4-phase fully integrated voltage regulator with local ground sensing dual loop zds hysteretic control using 6.5nh package bondwire inductors on 65nm bulk cmos," 21st Asia and South Pacific Design Automation Conference (ASP-DAC), pages 9–10, Jan 2016.

[2] E. A. Burton, G. Schrom, F. Paillet, J. Douglas, W. J. Lambert, K. Radhakrishnan, and M. J. Hill, "Fivr - fully integrated voltage regulators on 4th generation intel(r) core(tm) socs," IEEE Applied Power Electronics Conference and Exposition - APEC 2014, pages 432–439, March 2014.

[3] N. Sturcken, M. Petracca, S. Warren, P. Mantovani, L. P. Carloni, A. V. Peterchev, and K. L. Shepard, "A switched-inductor integrated voltage regulator with nonlinear feedback and network-on-chip load in 45 nm soi," IEEE Journal of Solid-State Circuits, vol. 47, no. 8, pp. 1935–1945, Aug. 2012.

Current Design Status and Outlook

Power Switches

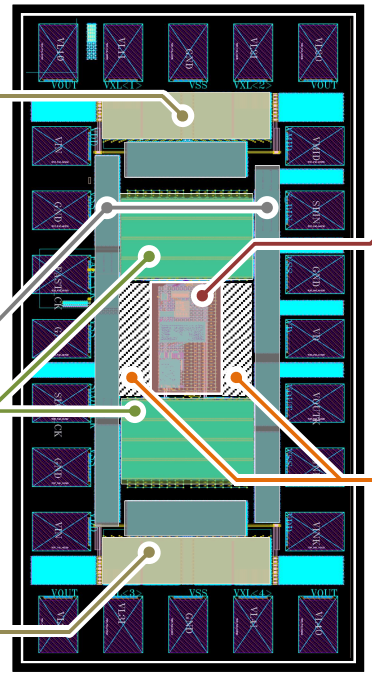
- Include gate drivers
- Build from 14nm FinFET devices
- Max. switching frequency: 250 MHz

Decoupling Capacitors

On-Chip Load

- Resistive Load
- Max. 2W Power

Power Switches



Open Loop Ctrl./Digital Block

- Serial bidirectional off-chip communication
- Registers
- Digital PWM
- Dead-time Control
- Load Control

Closed Loop Control (Planned)

- Voltage Mode Control
- Peak Current Mode Control + I_0 Feedforward
- Closed Loop/Open Loop interchangeable

1. Design

- Power Switch Testbench

Tape-out: February 2016

2. Design (Current)

- Better Power Switch Design
- Open Loop Control
- On-Chip Load

Tape-out: September 2016

3. Design (Planned)

- Closed Loop Analog Control

Tape-out: December 2016