Ferrochip Design Studio: A New Design Tool for Integrated Magnetics

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Introduction

One of the many benefits of integrated magnetics is the ability to optimise the component for a particular specification due to the many degrees of freedom. However, with this benefit comes increased complexity in design.

The Ferrochip Design Studio has been designed to be a user friendly software package to aid in the design, optimisation and fabrication of integrated magnetics.

It currently allows accurate modelling of magnetic components while also automatically generating Spice models and GDSII layout files.

The studio allows users to generate optimised designs with ease while also providing the detail required by experts.



An Intuitive User Interface

Ferrochip Design Studio												_	٥	×
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Design Builder	→ 4	Racetrack Inductor-SLM-	🖡 🗙 🛛 Design Resu	Its Comparison Geome	try									
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Sinusoidal Waveform		Parameter Value Min. Max. Unit Constraint	aja		Design: 1	Design: 2	Design: 5	esign. 4	*	*	-			



ferrochip



Currently Available Components

Magnetics	Circuits —
Solenoid Inductor	Buck Converter Single Phase
Rectangular Toroidal Inductor	Multiphase
Racetrack Inductor Single Layer Metal Double Layer Metal	Boost Converter Single Phase Multiphase
Coupled Solenoid Inductor	Buck-Boost Single Phase
Coupled Stripline Inductor Single Layer Metal Double Layer Metal	Sinusoidal Excitation
Racetrack Transformers Single Layer Metal Double Layer Metal	
Optimisati	ion Objectives
Maximise Full Load Efficiency	Maximise Inductance
Minimise DC Resistance	Minimise Footprint Area

Design Study - Coupled Cyclic Cascade Multiphase Inductors

The Design Studio is used to investigate the performance of two coupled structures for use in a multiphase buck converter which would be suitable for a microprocessor load. Two phase ripple current ratios($\Delta I_{p-p}/I_{dc}$) are investigated; 30% and 50%.

Circuit Specification

Frequency:100 MHzInput Voltage:1.8 VOutput Voltage:1 VDC Current:8 A

Coupled Inductors

Stripline - Single Layer Metal Solenoid - Interleaved



N-Phase cyclic cascade coupled Inductor

To enable a fair comparison of designs the stripline coupled inductor has a fixed winding thickness of 30 μ m and a single core lamination. For the solenoid type the winding thickness is set to 15 μ m (i.e. 30 μ m/2) and has two core laminations.





A number of design parameters are optimised for full load efficiency such as winding width, the number of phases, core aspect ratio and core layer thickness within a fixed area of 2 mm².

For this specification the optimum number of phases for all design cases is 5.

Ferrochip Design Studio										-	\circ >	ζ.
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Design Builder	- a	Stripline Coupled Inductor-SLM Cyclic Cascade 🔹 🖡 🗙	Des	on Results Comparis	on Ge	ometry	Characteri	sation				Ŧ
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4 🔁 Circuit Topology		Parameter Value Min. Max. Unit Constraint	l n	DC Winding Loss	w	0.379	0.597	0.247	0.388	1388		
Buck Converter		DC Winding Loss 0.247 W -		AC Winding Loss	w	0.0105	0.000748	0.0201	0.00133	1133		
Puck Converter		AC Winding Loss 0.0201 W -		Activition geoss	**	0.0103	0.000748	0.0201	0.00133			
Buck Multiphase Converter		Eddy Current Core Loss 0.0242 W -		Eddy Current Core Loss	vv	0.0666	0.107	0.0242	0.11			
Boost Converter		Hysteresis Core Loss 0.179 W -		Hysteresis Core Loss	w	0.163	0.0179	0.179	0.0222	222		
Boost Multiphase Converter		Total Loss 0.471 W -		Total Loss	W	0.619	0.723	0.471	0.521	521		
 Buck-Boost Converter 		Number Of Phases 5		Full Load Efficiency	%	92.8%	91.7%	94.4%	93.9%	3.9%		
🔺 🚝 Magnetic Component		Phase Angle 144		Number Of Phases	-	5	5	5	5	5		
Racetrack Inductor-SLM		Output Ripple Current 0.792 A _{p*p} -		Phase Angle	-	144	144	144	144	144		
Racetrack Inductor-DLM		Output Ripple Current/Idc 0.0989 Ap-p/Idc -		Output Ripple Current	A	0.669	0.642	0.792	0.745	.745		
Solenoid Inductor		Phase Ripple 0.8 Ap-p -		Output Ripple Current/I	A _e - _e /ldc	0.0836	0.0802	0.0989	0.0931	0931		
Rectangular Toroidal Inductor		Phase Ripple/Idc 0.5 Ap-p/Idc -		Phase Ripple	Ap-p	0.48	0.48	0.8	0.8	0.8		
Coupled Stripline Inductor-SLM		Peak 8-Field 0.325 T -		Dhase Disple/ids	An olide	0.3	0.3	0.5	0.5	20		
Coupled Stripline Inductor-DLM					Ap-p/loc	0.5	0.5	0.5	0.5	0.3		
Solenoid Coupled Interleaved Indi	luctor	Design Results		DC B-Field		0	U	0	0			
Racetrack Transformer-SLM	0000	Parameter Value Min. Max. Unit Constraint		Peak B-Field	T	0.198	0.244	0.325	0.308	308		
Received: Transformer-SLW		AC Self Phase inductance 4.662-09 12-06 22-06 H Range		AC Self Phase Inductant	н	8.51E-09	8.39E-09	4.66E-09	4.61E-09	E-09		
		Core Aspect Ratio 6.07 1 14 - Range		Device Area	m²	2E-06	2E-06	2E-06	2E-06	E-06		
Semiconductor Component		Core Laminations 1 Fixed		Core Aspect Ratio	-	8.48	6.53	6.07	2.27	2.27		
Capacitive Component		DC Phase Resistance 0.0193 Ω -		Core Laminations	-	1	2	1	2	2		
System		AC Phase Winding Resistar 0.0912 Ω -		DC Phase Resistance	Ω	0.0296	0.0467	0.0193	0.0303	3303		
Optimisation		Coupling Factor -0.416 Fixed			~	0.455	0.0515	0.0040	0.0000	1144		\sim
A Ittl Results		Core Width 0.000207 m Fixed	Loss	Breakdown × Loa	d Versus	Efficiency	Wa	veforms				Ŧ
Selected Design		Core Length 0.00125 m Fixed		0.8								
Characterisation		Device Height 6.25E-05 m Fixed		0.0						Eddy Current Cor	e Loss	
Waveforms		Device Width 0.00135 m Fixed								AC Winding Loss		
Efficiency Versus Load		Device Length 0.00148 m Fixed		0.6								
Loss Breakdown		Process Results										
Comparison		Parameter Value Min. Max. Unit Constraint		N								
Geometry		Winding Spacing 1.5E-05 m Fixed		· 0.4								
		Winding Width 7.45E-05 2E-05 0.0002 m Range		-								
		Winding Thickness 3E-05 m Fixed										
		Core to Winding Spacing 2E-05 m Fixed		0.2								
		Core Overlap 2E-05 m Fixed										
		Core Separation 3E-05 m Fixed		0								
		Core Lever Thickness 1.232-06 SE-07 3E-06 M Range		0.		100	1		1	2 3 4		
		Top Insulator 1.5E-05 - m Fixed								_ Design		
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Loss Breakdown and Comparison

The results show that for both phase ripple ratios investigated the coupled stripline inductor offers the highest full load efficiency.

That is 92.8% and 94.4% for 30% and 50% phase ripple current ratios respectively.



Geometry, Waveforms and Load vs. Efficiency

For load currents below approximately 3 A, the solenoid coupled inductor has a higher efficiency due to lower AC losses. It is interesting to note that core layer thickness for the solenoid is greater than the skin depth (2 μ m) in order to reduce DC resistance. This results in a sharper inductance roll off compared to the stripline structure.





Optimum Designs for a 50% Phase Ripple Current Ratio



GDSII Layout Files

Layout files automatically generated for export to 3rd party layout tools



Spice Model Curve Fitting

Phase Magnetizing Inductance
 Spice Model
 Phase Resistance
 Spice Model
 Phase Leakage Inductance

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Parameter DC Winding Loss

AC Winding Loss

Total Loss

Phase Angle

Phase Ripple

DC B-Field

Peak B-Field

Design Results

AC Self Phase Ind

Core Aspect Ratio

Core Laminations

Coupling Factor

Phase Angle

Core Width

Core Length

Device Height

Device Width

Device Length

Process Results

DC Phase Resistance

AC Phase Winding Resista

2.27

0.0303

0.0382

-0.409

0.000316

0.000717

6.5E-05

0.00201

0.000995

1.5E-05

0.000131

1.5E-05

2E-05

1E-07

1.5E-05

Core Layer Thickness 2.47E-06 5E-07 3E-06

Internal Winding Separatic 2E-05

Core Insulator Thickness

Top Insulator

Value Min. Max.

2E-05 0.0002

144

16

Range

Fixed

Fixed

Fixed

m Fixed

m Fixed

m Fixed

m Fixed

m Fixed

Unit Constraint

m Fixed

m Range

m Fixed

m Fixed

m Fixed

m Range

m Fixed

m Fixed

Parameter

Device Area Number of Turns

Phase Ripple/Ido

Eddy Current Core Loss

Hysteresis Core Loss

Full Load Efficiency

Number Of Phases

Output Ripple Current

Output Ripple Current/Idc

Result Display 🛛 🗸 Optimum Only 🖌 Always Load Optimum 🗌 Show Magnetically Saturated



12 🔳 📙 Design Builder

- Overview
- Vaveform Excitation
- 🔺 🎀 Circuit Topology
- Buck Converter
- Buck Multiphase Converte
- Boost Converter
- Boost Multiphase Converter
- Buck-Boost Converter
- 🔺 🚅 Magnetic Component Racetrack Inductor-SLM
- Racetrack Inductor-DLM
- Solenoid Inductor
- Rectangular Toroidal Inducto Coupled Stripline Inductor-SLM
- Coupled Stripline Inductor-DLM
- Solenoid Coupled Interleaved Inductor
- Racetrack Transformer-SLM
- Racetrack Transformer-DLM
- Semiconductor Component
- Capacitive Component
- 🏚 System
- 😑 Optimisa
- A III Results
- Selected Design Characterisation
- Waveforms
- Efficiency Versus Load Loss Breakdown
- Compariso
- Geometry







Frequency independent Spice model automatically curve fitted.







Conclusions

A brief outline of a new Design Studio for the optimisation of integrated magnetics is presented. It has been used to optimise a 1.8 V to 1 V multiphase buck converter using coupled inductors arranged in a cyclic cascade configuration.

The results of this study show that for high load currents, coupled stripline inductors offers the highest full load efficiencies compared to coupled interleaved solenoid inductors due their lower DC resistance for a fixed phase ripple current ratio.

The number of degrees of freedom allowed in the design of integrated magnetics mean that the component can be optimised for particular load conditions to achieve maximum performance.

Future Work

It is envisaged that the Design Studio will eventually provide a complete platform for the optimisation and validation of integrated systems incorporating magnetics.

Links to 3rd party software packages is seen as a key piece of future work and plans are in place to incorporate semiconductor and capacitor models into the Design Studio. This coupled with a scripting interface will allow smooth integration into already established design flows.

Ferrochip Design Studio - Beta

A 1-month trial version with limited models is now available to users. Please contact us for more information.

Contact

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