Deep Trench Capacitor Based On-Chip Switched Capacitor Voltage Regulators for Microprocessor Power Delivery

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Microprocessor power delivery – Typical
Microprocessor power delivery – Target

- On-chip switched capacitor voltage regulator (SCVR)

VRM efficiency
Improves 3–4%

C4 current
Reduces 2x

IR drops
Reduces 2x

Ldi/dt
Reduces 2x

12V VRM 1.8V

≈1.8V

Multicore microprocessor die

SCVR 0 0.7–1.1V core 0

SCVR 1 0.7–1.1V core 1

SCVR 2 0.7–1.1V core 2

SCVR 3 0.7–1.1V core 3

Voltage granularity
Improves efficiency up to 21%
(workload dependent [1])

How to achieve…?

- More than 85% efficiency
- More than 1W/mm²
- Faster than 1ns
- Deliver more than 1W

Simultaneously!
…with a little help from a friend!

- **The deep trench capacitor**
  - High capacitance density
  - Low bottom plate losses

- **Fast transistors in 32nm**
  - Good $R_{on}$ and $Q_g$ FOM

F. Roozeboom et al., PwrSoC 2008, Cork, Ireland

Wang et al., EIDM 2009
First chip – 2:1 SC converter

- A “learning vehicle”
  - 32nm SOI CMOS
  - 4.6W/mm² power density
  - 86% efficiency

Measured efficiency and power density

T. Andersen et al. “A 4.6W/mm² power density 86% efficiency on-chip switched capacitor DC-DC converter in 32nm SOI CMOS,” APEC, 2013
Summary: First chip

- More than 85% efficiency ✓ 86%
- More than 1W/mm² ✓ 4.6W/mm² but excl. $C_{out}$
- Faster than 1ns X Open loop
- Deliver more than 1W X 16mW
Second chip: a complete SCVR system

T. Andersen et al. “A sub-ns response on-chip switched capacitor DC-DC voltage regulator delivering 3.7W/mm² at 90% efficiency using deep-trench capacitors in 32nm SOI CMOS,” ISSCC, 2013
SC converter power stage

Interleaving

- Interleaving reduces:
  - output voltage ripple
  - input current ripple

- No dedicated output decoupling capacitance for $N \gg 1$
Feedback regulation: frequency control
Controller implementation

Single-bound hysteretic regulation

$V_{ref}$

$V_{out}$

$V_{ripple}$

clk$_{cc}$

clk$_{trig}$

Clocked comparator

Digital clock interleaver

$V_{out}$

$V_{ref}$

clk$_{cc}$

clk$_{trig}$

clk$_{MSB}$

clk$_{0}$

clk$_{1}$

clk$_{2}$

clk$_{3}$

$cl$k$_{cc} = 4$GHz
Chip photo

Test chip in 32nm SOI CMOS

On-chip load 258μm

Digital controller

582μm

33μm

Deep Trench (~1nF)

M_{1-9}(s)

Gate driver

Power grid

Deep Trench (~1nF)
Measured efficiency and power density – $V_{\text{in}} = 1.8\text{V}$
Measured transient response

Note! $V_{in}$ collapse is causing the output voltage droop
Summary: Second chip

- More than 85% efficiency ✔️ 90%
- More than 1W/mm² ✔️ 3.7W/mm²
- Faster than 1ns ✔️ <1ns but with droop
- Deliver more than 1W ✗ 840mW
Slides intentionally left out...
Summary: on-chip switched capacitor voltage regulators

- More than 85% efficiency  ✔️  85%
- More than 1W/mm²  ✔️  3.1W/mm²
- Faster than 1ns  ✔️  <1ns
- Deliver more than 1W  ✔️  10W