Scalable series-stacked power delivery architectures for improved efficiency and reduced supply current

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PwrSoC 2014
October 8, 2014
Outline

- Background and motivation
- Series-stacked architecture
  - Previous work
  - Advantages and challenges
- Top down:
  - General purpose computing units
  - Extreme efficiency data center power delivery
  - Scalability, experimental results
- Bottom up:
  - Specialized compute cores
  - Power converter and load integration
  - New switched-capacitor architectures
- Conclusion
Today’s Challenge – The Looming “Power Delivery Wall”

- Continued voltage reduction
- CPU power has remained fairly constant
CPU Current Trends

![Graph showing CPU Current Consumption over years with different Intel processors highlighted.]

- Intel Core i7
- Intel Xeon E7
- Intel Xeon
- Intel 386 SX
- Intel Pentium
VRM limitations

- Large current on I/O pins
- Difficult to realize large step-down voltage conversion on-chip
- Efficiency is limited by power converter efficiency

Can we leverage the increased core count for power delivery purposes?
Multi-core trends
Other Applications – Low Voltage Sources

- **Solar**
  - 0.5 V cells
  - 30 V modules
  - 600 V strings

- **Battery systems**
  - 3-12 V cells
  - Up to 400 V DC bus

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Series-stacking is widely used in low voltage DC sources
- Stack $N$ cores to match input voltage
- Inherent voltage step-down
- Greatly reduced I/O current
- No power conversion losses!
Series-stacked Architecture - Challenges

- Voltage regulation
- Grounding
- Communication across voltage domains
Prior Work

- We are looking at massively scaled architectures for future multi-core architectures
- Rely on high efficiency power electronics

Data Center Architectures

- **Before:**
  - Single computer
  - Single processor
  - Single core
  - Stacking not beneficial

- **Today:**
  - Warehouses of computers
  - Multi-processor servers
  - Multi-core CPUs
  - Stacking helpful, across the full system

Blue Waters @ Illinois
Data center application

- Motivation here is conversion efficiency
- Shares many constraints with stacked cores
- Proof-of-concept demonstration
- Voltage regulation
- Grounding
  - Design change
- Communication across voltage domains
  - Ethernet 1500 V isolation
  - Fiber-optic
- Hot-swapping, reliability
Proposed Solution – Differential Power Processing

✓ Voltage regulation by injecting or rejecting current from nodes.
✓ Bidirectional DPP converters process only the **difference** in power.
✓ Bulk power is delivered to the series-stacked servers without being processed.

Differential Power Processing – Low Voltage Ratings

- Non-isolated
- Inefficient power transfer
- Order-dependent

- Isolated converters
- Minimum power transfer
- Order independent

McClurg ECCE 2014

Candan INTELEC 2014
Four prototype DAB converter are designed as DPP converters.
Simple phase shift modulation is used.
Symmetrical design at both sides of the transformer.

**DAB Converter Specifications and Key Components**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Power</td>
<td>120 W</td>
</tr>
<tr>
<td>Peak Efficiency</td>
<td>95%</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>175 kHz</td>
</tr>
<tr>
<td>Modulation Technique</td>
<td>Simple phase shift</td>
</tr>
<tr>
<td>Control Mode</td>
<td>Bidirectional Hysteresis</td>
</tr>
<tr>
<td>Switch</td>
<td>DrMOS - Vishay SiC780ACD</td>
</tr>
<tr>
<td>Digital Isolator</td>
<td>TI - ISO7241C</td>
</tr>
<tr>
<td>Microcontroller</td>
<td>TI - C2000 Piccolo</td>
</tr>
</tbody>
</table>

*BoM is around $30*
Control Objectives:
- Server voltage regulation.
- Virtual Bus voltage regulation.
- Voltage sampling only.
- No communication between converters.
- Highest possible light-load efficiency

Bi-directional Hysteresis Control

Experimental Setup and Tests

Simultaneous measurements at 5kS/s with NI DAQ

- Input power: Bus voltage and current
- Output power: Server voltages and currents
- Virtual bus voltage

Web traffic test:
- 700 requests per second → 4 servers

Computation test:
- Linux 'stress' utility [*] on individual servers

The Dell Optiplex SX775 Core 2 Duo Motherboard Input: 12V

DPP converter

Agilent 6674A

Dell Optiplex SX775
Core 2 Duo
Motherboard Input: 12V

- Input: 12V DPP converter

### Experimental Setup – Conventional Architecture

- A best-in-class PSU with 96% peak efficiency.
- Identical web traffic and computational tests.
- The same measurement unit.

*SynQor PQ60120QEx25 - $200*
Experimental Results – Computation Test

Typical waveforms

Average Input and Output Powers During Computation Test

\[
< P_{\text{in}} > = V_{\text{Bus}} \times I_{\text{Bus}} \quad 426.60 \text{ W}
\]

\[
< P_{\text{out}} > = \sum_{i=1}^{4} V_{s,i} \times I_{s,i} \quad 426.11 \text{ W}
\]

Efficiency \quad 99.89 \%
Comparison

Comparison of Proposed Architecture with Conventional Architecture

<table>
<thead>
<tr>
<th></th>
<th>Web Traffic Test</th>
<th></th>
<th>Computation Test</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Proposed</td>
<td>Conventional</td>
<td>Proposed</td>
<td>Conventional</td>
</tr>
<tr>
<td>(&lt; P_{in} &gt;) [W]</td>
<td>241.09</td>
<td>252.87</td>
<td>426.60</td>
<td>447.59</td>
</tr>
<tr>
<td>(&lt; P_{out} &gt;) [W]</td>
<td>237.98</td>
<td>238.58</td>
<td>426.11</td>
<td>426.51</td>
</tr>
<tr>
<td>(&lt; P_{loss} &gt;) [W]</td>
<td>3.11</td>
<td>14.29</td>
<td>0.49</td>
<td>21.08</td>
</tr>
<tr>
<td>Efficiency [%]</td>
<td>98.71</td>
<td>94.35</td>
<td>99.89</td>
<td>95.29</td>
</tr>
</tbody>
</table>

With server to virtual bus DPP:

- 4.6 times reduction in average power loss for web traffic
- 40 times reduction in average power loss for computation

Note that the standard power supply for this system has 80-90% efficiency
Ongoing work

- Core-level emulation
  - 1GHz ARM Cortex-A8
- 5V, 1A Power requirements
- On-board PMU
- Resonant SC DPP converters

- Load balancing strategies
  - Modified Hadoop scheduler

Working with software and CPU architecture partners (you all should)
Bottom Up – Stackable Cores

Today:
- Tight voltage regulation
  - Transient conditions
- Error-free computing
- Digital logic has priority

Tomorrow?
- Deeply scaled CMOS (post-CMOS)
  - Increased variations
- Embrace errors?
  - Communication-inspired computing
- Power delivery and computing equal partners

Systems On Nanoscale Information fabriCs Center (SONIC)
Zhang et al.: A 0.79 pJ/k-gate, 83% efficient unified core and voltage regulator architecture, JSSC 2014

2x2mm, IBM 130 nm CMOS
Embrace the ripple
Conclusion

- Demonstrated a scalable series-stacked computer architecture
  - 12 V servers
  - Differential power processing
  - 40x loss reduction compared to state-of-the-art
- Outlined design challenges and opportunities for core-level work
- Requires careful cooperation/co-design of power electronics, CPU, and software
- Emerging compute units compatible with series-stacking may be best way forward

*Post-CMOS devices may be the ultimate driver for this technology*
Acknowledgments

- Texas Instruments
  - Pradeep Shenoy

- Google
  - Google Faculty Research Award

- UIUC Strategic Research Initiative
  - Profs. Phil Krein, Naresh Shanbhag, Yi Lu

Questions?