Resonant Switched Capacitor Converters for High-Density Power Delivery

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Motivation

- Applications that demand: high density + efficiency

**Application**

- Mobile Devices & Communication
- Performance Computing
- Renewable Energy, Automotive

**Trends**

- Pressure on battery life, size, cost, # converters
- # cores, density, integration, parasitics
- Extreme cost pressure, reliability
Switched Capacitor Converters

- Growing interest as candidate for monolithic DC-DC
- High energy density of Si-integrated capacitors (compared to inductors)
- Higher device utilization FOM* compared to traditional DC-DC converter topologies
- Deep-trench capacitors & scalable CMOS processes
- No Inductors

*M. D. Seeman et. al, *IEEE TPEL*, 2008
Resonant Switched Capacitor Converters

Similarities to SC Converters:
- Similar architectures (Ladder, Dickson, Series-Parallel, etc)
- Favorable device utilization FOMs
- Leverage high-density capacitors

Potential Advantages:
- Small magnetic component (few nH) resonates out reactive impedance (better capacitance utilization + soft switching)
- Improved trade-offs between switching (+bottom plate) loss and conduction loss

Kesarwani et. al., ISSCC, 2014
Resonant Operation

Nominal 2:1 Converter

Averaged Steady State Conditions:

\[ R_{EFF} \cong \frac{\pi^2}{8} R_{esr} \]
Effective Resistance

- $R_{\text{EFF}}$ models the effective output impedance of the converter
- SC in FSL: energy transfer is limited by ESR
- ReSC: Comparable minimum $R_{\text{EFF}}$, but at lower frequency
- Sub-harmonic operation for light load
- Burst mode even better\(^{[1]}\)

\[\begin{align*}
V_{\text{DD}} & \quad \rightarrow \quad R_{\text{EFF}} \quad \rightarrow \quad V_{\text{out}} \\
\rightarrow & \quad \text{Transformer Model} \\
N:1 & \quad \text{I}_{\text{DC}}
\end{align*}\]

\[\frac{R_{\text{EFF}}}{R_{\text{ESR}}} \begin{cases} \text{ReSC} & \text{SSL} \quad \text{FSL} \\
\text{SC} & \text{DOTM} \quad \text{ReSC Limit} \\
\text{SC Limit} & \text{DOTM} \quad \text{ReSC Limit}
\end{cases}\]

\[\text{R}_{\text{ESR}} \pi^2/8\]

\[\text{1/4f}_{\text{sw}} C\]

\[\text{Normalized Switching Frequency}\]

\[\begin{align*}
10^2 & \quad \rightarrow \quad 10^{-1} \\
10^{-1} & \quad \rightarrow \quad 10^0 \\
10^0 & \quad \rightarrow \quad 10^1
\end{align*}\]

\[\text{[1] Kesarwani & Stauth, ISSCC '14} \]

“Dynamic Off-Time Modulation (DOTM)”
Interleaving in ReSC

- Odd-order interleaving is better
- 3-phase $\rightarrow$ multiple order of magnitude improvement compared to 1-phase

When total die area is constrained:
- More bypass $\rightarrow$ lower ripple
- With interleaving can allocate more to CX $\rightarrow$ Major improvements
Limitations and Disadvantages

Summary (limitations)

- Need magnetic component(s)
  (Design goal is low ESR in resonant loop)

- Need ‘some’ explicit bypass capacitance

- Practical limitations on interleaving
  (Inductor scaling considerations)
Limitations and Disadvantages

Nonetheless:
- Favorable operation with *very small* inductors
- Lower $f_{SW} \rightarrow$ can **reduce** ESR in capacitors and interconnect (parasitics we often don’t talk about!)

**Graph:**
- $R_{ESR} = 8X \,(Q=1.25)$
- $R_{ESR} = 4X \,(Q=2.5)$
- $R_{ESR} = 2X \,(Q=5)$
- $R_{ESR} = 1X \,(Q=10)$
- SC: $R_{ESR} = 1X$

**Legend:**
- $R_{EFF}$
- Normalized Switching Frequency

**Analysis:**
Full analysis, optimization, and comparison is complicated:
- *Kesarwani & Stauth, COMPEL 2013*
- *Kesarwani & Stauth, TPEL 2015 (coming)*
Major Opportunity & Potential Advantage: Efficient & Granular Variable Conversion Ratios
Example – Step Up/Down

"boost" mode

"buck" mode
Challenges & Benefits

• Requires hard switching on one transition
  – Possible diode conduction
  – Need fast control

Advantages:

• Potential for high efficiency above/below nominal operating point
• Feedback control & regulation
• Can be used to compensate the load line!
Other ReSC Topologies: Direct vs Indirect

2:1 ReSC (Indirect Topology)

Identical to 2:1 SC but with resonant flying impedance

2:1 ReSC (Direct Topology)

Similar to 3-level buck converter*; but operates in resonant mode

*I/O perspective:
Identical Operation

Only major difference is current waveform in inductor

*G.V. Pique, PESC ’08
Direct/Indirect Comparison

Typical Inductor Characteristics
(Air-Core Solenoid 5.5nH)

Indirect Topology
- ~100% power at $f_0$

Direct Toplogy
- ~80% of power at DC

→ Lower conduction loss in inductor!
  (ballpark → ~ 3-4x lower)
Other Topologies (Higher Conversion Ratios): Ladder Architecture

N:1 SC Ladder Converter

N:1 ReSC Ladder Converter

Requires N-1 magnetic components

Simplest Abstraction: Resonate each flying capacitor in the circuit
Example: Photovoltaic Application

Example 1:
- Many Modules in Series
- ‘Submodule Converter’ (~10 V each; stack up to 500V)
- $\eta_{EFF}>99\%$
- insertion loss < 0.1 \%

Stauth et al, ISSCC ’12, TPEL ’13

Example 2:
- IC-Based conv.
- 4-6 cell strings
- < 1 cm²
- < 2mm height
- $\eta_{EFF}>95$-98\%

Sangwan et al, ECCE ‘14

PV Module
String 1
String 2
String 3
Resonant Switched-Capacitor Converter

To V1 of next panel
To V2 of next panel

VS4
VS3
VS2
VS1
V1
V2
V3
V4
Zx3
Zx2
Zx1
Lx
Cx
Lx
Cx
# Other Topologies: e.g. Series-Parallel, Dickson

## N:1 Series-Parallel ReSC

- Devices rated for ~ full stack voltage
- Different resonant frequency, each phase

## 4:1 Dickson ReSC*

- Efficient utilization of power devices
- Some charge sharing on phase transitions*

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*Lei, Pilawa, and May: COMPEL 2013*
High-Density Power Delivery:
1st Gen mm-Scale Prototype

- Technology: 0.18 μm CMOS
- Topology: 2-phase ReSC
- Conv Ratio: 2:1
- Vin: ~4.5-6 V
- Vout: ~2-3 V
- Frequency: ~35 MHz
- Cx: 9 nF/phase
- Cbp: 11 nF x 2
- Capacitor: MIM: 6.6 fF/um²

Dynamic Off-time Modulation (DOTM or Burst Mode) for light load & regulation

Die-attached air-core solenoid inductors (gold stud, solder reflow process)
Efficiency Measurements

Efficiency of 85.0 % @ 0.60 W/mm²
Comparison to Prior Work
(ISSCC Tech Trends 2014)

- 3-Φ ReSC 0.18, all-NMOS + var conversion ratios
- 2-Φ ReSC 0.18 um Bulk CMOS
- PCB-integrated Magnetics

G. Villar-Pique et al, TPEL 2013
Efficiency vs Peak Power

- **ISSCC 2014**
- **This Work (.18µm bulk, MIM)**
- 5.5nH discrete
- 1.9nH discrete
- 1.1nH PCB integrated

- **SC**
- **Inductive**
Future Prospects

Si-Microfabricated, High-frequency Magnetic Components

e.g. V-groove, Racetrack, Toroidal Inductor (Sullivan et al.)

Future Goal: Leverage both high-density (trench) caps, and high-frequency microfabricated magnetics

ReSC improves significantly with higher Cap Density and Low ESR Inductors!
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