Distributed Power Conversion - An answer to Power Delivery Challenges in SoCs?

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Outline

Motivation for fully integrated VRs

Capability of Switched Capacitor Voltage Regulator (SCVR)

DVFS enabler with minimum area-power overhead

Co-design with load

Summary and Conclusion
Motivation for fully integrated voltage regulators

The Platform Perspective

Current 15" MacBook Pro w/ CRW
HSW VR solution: CPU 3 phases; PCH 1 phase

Courtesy: S. Soman, A. Uan-zo-li; Intel
Motivation for fully integrated voltage regulators

The Platform Perspective

SoCs inherently require several voltage rails

Possible solution w/o FIVR: CPU ~11 phases; PCH 1 phase

Input rail consolidation simplifies power delivery significantly
Motivation for fully integrated voltage regulators

The Die Side of the Story

- Faster state transitions by 25%, higher performance per watt
- Overall idle power slashed by 20x, battery life improvement by > 50%
- Proliferation of Integrated voltage regulators in latest technology node

[Burton et.al APEC ’14]  [Kurd et.al ISSCC ’14]
Motivation for fully integrated voltage regulators

Finer Grain Voltage Domains

[Figure 6. (a) \( F_{MAX} \) recovery for different Adaptive Clock Distribution lengths. (b) Power vs. frequency for baseline design, baseline with adaptive clocking, and dual-Vcc design with adaptive clocking. (c) Energy efficiency vs. \( V_{CC} \).]

- Vmin reduction through many voltage domains
- Necessary level shifters incorporated here with 0 area penalty

[Tokunaga et. al ISSCC '14] Measured data

[PSoC 2014 Rinkle Jain]
Switched Capacitor Voltage Regulator Capability

Switched Capacitor VR with MIM

High density MIM

TEM [C.-H. Jan et al.; IEDM 2012]

<table>
<thead>
<tr>
<th>Technology</th>
<th>22nm Tri-gate CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passive Type</td>
<td>High Density MIM</td>
</tr>
<tr>
<td>MIM Area</td>
<td>99450 $\mu m^2$</td>
</tr>
<tr>
<td>Power Stage Area</td>
<td>3240 $\mu m^2$</td>
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<tr>
<td>Control Area</td>
<td>420 $\mu m^2$</td>
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<tr>
<td>Total Active Area</td>
<td>3660 $\mu m^2$</td>
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<tr>
<td>Total RF Area</td>
<td>101376 $\mu m^2$</td>
</tr>
<tr>
<td>Test Interface</td>
<td>Membrane probe</td>
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</tbody>
</table>

[R. Jain et al.; JSSC 2014]
Switched Capacitor Voltage Regulator Capability

Conversion Efficiency Measurements

- 84% peak and 63% minimum efficiency
- Lower peaks in other modes due to larger switch size
- Flat efficiency down to << 10% rated load with PFM

[R. Jain et al.; JSSC 2014]
Switched Capacitor Voltage Regulator Capability

Motivation for Conductance Modulation

\[ V_e = V_{in} \frac{n}{m} \]

\[ R_{out} = f(R_{fsl} \propto \frac{r_{dson}}{d}, R_{ssl} \propto \frac{1}{C_{fsw}}) \]

Averaged Model

Efficiency Contours

Limitations of simple frequency modulation

- Lower-than-optimal conversion efficiency at lower voltages
- Increased output ripple and associated power loss at light loads
- Input noise coupling. EMI/RFI due to impulsive current draw

Other knobs: \( 1/r_{dson} \) (conductance), \( C \) (fly capacitance), \( d \) (duty)
Switched Capacitor Voltage Regulator Capability

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Switched Capacitor Voltage Regulator Capability

Adaptive Widths Architecture

- Total transistor size implemented as 3 weighted banks (ratio 2:1:0.25)
- 8 way interleaving, 2GHz input clock; 2 bits for width selection

[R. Jain et al.; CICC 2014]
Switched Capacitor Voltage Regulator Capability

AW Measurements at Constant $V_{\text{ref}}$

- $f_{\text{sw}} < F_{\text{th}} W = \frac{bW'}{a}$ implies higher efficiency at $W'$ ($W'=W/n$)
- $f_{\text{sw}}$ is a good indicator of low voltage and light load conditions
Switched Capacitor Voltage Regulator Capability

**AW Measurements at different $V_{\text{ref}}$**

- Rout uniquely defines the optimal width
Switched Capacitor Voltage Regulator Capability

**AW control law: Measurements**

- \( F_{th} \) for each width computed from two open loop measurements
- Results show that proposed transition is effective
Switched Capacitor Voltage Regulator Capability

AW Conversion Efficiency Measurements

- All three major loss mechanisms scale with load (more than linearly)
- Nearly 15% improvement in 2:1 mode
Switched Capacitor Voltage Regulator Capability

**AW Conversion Efficiency Measurements**

- Constant resistance load
- All modes show optimal efficiency peaks
### Capability Summary

<table>
<thead>
<tr>
<th>Reference</th>
<th>2</th>
<th>3</th>
<th>5</th>
<th>This work</th>
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<tbody>
<tr>
<td>Process</td>
<td>45nm SOI</td>
<td>45nm</td>
<td>32nm SOI</td>
<td>22nm trigate</td>
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<td>Passives type</td>
<td>Deep trench</td>
<td>Gate Oxide SOI</td>
<td>Gate Oxide</td>
<td>MIM</td>
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<td>Maximum frequency</td>
<td>100MHz</td>
<td>30MHz</td>
<td>225MHz</td>
<td>250MHz</td>
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<tr>
<td>Input Voltage</td>
<td>2V</td>
<td>1.8V</td>
<td>2V</td>
<td>1.23V</td>
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<tr>
<td>Output</td>
<td>0.95V/2.7mA</td>
<td>0.8-1V/8mA</td>
<td>0.4-1.1V/0.28A</td>
<td>0.45-1V, 88mA</td>
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<tr>
<td>Power Efficiency %</td>
<td>90</td>
<td>69</td>
<td>81</td>
<td><a href="mailto:70@0.55V">70@0.55V</a>, <a href="mailto:84@1.1V">84@1.1V</a></td>
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<tr>
<td>Response time</td>
<td>Unregulated</td>
<td>120-200ns</td>
<td>Unregulated</td>
<td>3-5ns</td>
</tr>
<tr>
<td>Droop</td>
<td>-</td>
<td>250mV</td>
<td>-</td>
<td>≤25mV</td>
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<tr>
<td>Current density A/mm²</td>
<td>2.3</td>
<td>0.050</td>
<td>0.73</td>
<td>0.88</td>
</tr>
<tr>
<td>Area Overhead</td>
<td>13%</td>
<td>6x</td>
<td>41%</td>
<td>3.6%</td>
</tr>
</tbody>
</table>

- All-digital multi-mode SCVR in 22nm tri-gate CMOS using high-density MIM
- Wide voltage range, good conversion efficiency across load
- Low area overhead of 3.6%, comparison assumes 30mA, 0.1mm² load
- Fast < 5ns response times
- Max VR current density of 400(880) mA/mm² in 1:1(2:1) modes
Current capability

- At 1V, 2:1 mode: 1.2-1.6A/mm² (22nm)
- Atom at 2.5A/mm², Graphics at 1.25 A/mm²
- Worst case di/dt: atom at 2A/ns, Graphics at 150mA/ns
- Vin=Vccmax feasible, downconversion is not a must
- Reuse power gates, hybrid solution with LDO
- Minimum active power and area overhead
Distributed Implementation

Physical Design Constraints

Practical issues: Co-design with load

- Graphics: large area, lower power density
- Lots of signals traverse $x$ and $y$ and $x < y$
- Highly automated design, push button SoC Methodology (unlike core)
- Shared metal resources, IR drop on weak grids

Need for distribution

- One contiguous VR block $\Rightarrow$ large keep-out-regions in APR
- A stand-alone minimum-size VR tile desired, custom-laid out ok
- VR tile should be reuse-able across loads of any size, aspect ratio
Distributed Implementation

Active Ripple Control Enabling Distribution

**Proposed solution**

- Distributed standalone tiles
- Minimal interleaving
- Local current mode control
- Central PFM to drive all tiles
Distributed Implementation

Active Ripple Control Enabling Distribution

- VR Tile 1 $V_{out}$
- VR Tile 2 $V_{out}$
- Central feedback sense $V_{out}$
- $V_{ref}$
- Load step at Tile1

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Distributed Implementation

Active Ripple Control Enabling Distribution

VR Tile 1 Vout

VRTile 2 Vout

Central feedback sense Vout

Vref

load step at tile 1
Distributed Implementation

Active Ripple Mitigation Scheme (ARMS)

- Gate voltage of select transistors controlled using diff amplifier
- Ideally switch currents match load currents on a cycle by cycle basis

Objective: A frugal design that works across all conversion modes
Distributed Implementation

Active Ripple Mitigation Scheme (ARMS)

ARMS in 2:1 Operation

Low-Bound Hysteretic Control (LBHC)

Adaptive Gate Driver (AD)

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Load, $V_{out}$ independent ripple

Minimum size VR tile
Summary

- Point-of-load VR solution for fine grain domains enable power benefits
- Fast switched capacitor VRs with low area overhead demonstrated
- Capacitance density and ESR dict ate SCVR capability, less area with every node
- Hybrid DLDO-SCVR meets medium current density loads, no power penalty
- Control techniques ensure optimal efficiency and small VR tiles
- Distributed VRs desired for APR-friendly SoC integration for wide adoption
- High-current-density loads may have (i) few bumps or platform limitations. (ii) high di/dt, tighter impedance requirements ⇒ step down IVR

Higher current density VR solutions for small domains are needed!
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Thank you for your attention!