High Density Capacitor for Power Management Applications and its Integration in the SiP


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Outline

● High Density Capacitor
  ■ Capacitance density for various operating voltages
  ■ AC characteristics

● Capacitor die attachment techniques
  ■ Surface mount (on a substrate or another die)
  ■ Advanced wafer to wafer attachment techniques

● Summary and conclusions
Deep Trench Capacitor Structure
## Deep Trench Capacitor characteristics

<table>
<thead>
<tr>
<th>Density, nF/mm²</th>
<th>Breakdown Voltage, V</th>
<th>TDDB, V</th>
<th>Max Voltage rating, V</th>
</tr>
</thead>
<tbody>
<tr>
<td>180</td>
<td>16.1</td>
<td>7.0</td>
<td>4.5</td>
</tr>
<tr>
<td>250</td>
<td>14.3</td>
<td>6.8</td>
<td>4.2</td>
</tr>
<tr>
<td>500</td>
<td>6.5</td>
<td>4.5</td>
<td>3.2</td>
</tr>
<tr>
<td>600-700</td>
<td>4.0</td>
<td>3.8</td>
<td>2.5-1.2</td>
</tr>
</tbody>
</table>

### Graphs

- **VBD(I-V) vs Capacitance Density**
- **TDDB vs Capacitance Density**
DTC Capacitor Density v.s. Vcc, TDDB, VBD

V_{operate} vs Capacitance Density

- 180fF/um^2
- 250fF/um^2
- 500fF/um^2
Integrated capacitor Vcc and Tcc vs MLCC (~20nF device)

- TSMC DTC shows better VCC than MLCC
- TSMC DTC shows better TCC than MLCC
Our integrated device VCC is superior to that reported for the MLCC SMD0204
Integrated capacitor frequency response

- TSMC CIP2: Reduced ESR “hump” (low frequency to 10MHz)
- TSMC CIP1+2: Improve ESR to around 0.2ohm level

10nF T06-RF Pattern, capacitance density around 500nF/mm²

- 17.2nF, 500nF/mm² Original
- 19.7nF, 556nF/mm² CIP2
- 17.7nF, 500nF/mm² CIP1+CIP2
- MLCC 10nF(0603)
- MLCC 20nF(0603)
Equivalent Series Inductance

- $8.7\,\text{nF} @ 234\,\text{nF/mm}^2$ (N-type)
- $23.9\,\text{nF} @ 650\,\text{nF/mm}^2$ (square CONT)
- $17.1\,\text{nF} @ 500\,\text{nF/mm}^2$ (Salicide)
- $17.6\,\text{nF} @ 500\,\text{nF/mm}^2$, TV3, Salicide+Slot cont (TV2 style)
- $17.2\,\text{nF} @ 500\,\text{nF/mm}^2$ (N-type)
- $23.9\,\text{nF} @ 650\,\text{nF/mm}^2$ (street CONT)
- $19.7\,\text{nF} @ 556\,\text{nF/mm}^2$ (Salicide)
- $17.7\,\text{nF} @ 500\,\text{nF/mm}^2$, TV3, BGM2(0204)
- $10\,\text{nF}$ - MLCC
- $20\,\text{nF}$ - MLCC
Surface Mount Assembly
Approach #1 solder stenciled on soldering pads

IPD die

Substrate soldering pads

After reflow

Many voids trapped
## Approach#1 solder stenciled on soldering pads

<table>
<thead>
<tr>
<th>IPD device type</th>
<th>21</th>
<th>22</th>
<th>23</th>
<th>24</th>
<th>25</th>
<th>AVG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si THK(um)</td>
<td>78.9</td>
<td>79.8</td>
<td>78.4</td>
<td>76.1</td>
<td>77.5</td>
<td>78.1</td>
</tr>
<tr>
<td>Solder THK(um)</td>
<td>9</td>
<td>9.4</td>
<td>12.4</td>
<td>9.7</td>
<td>13.4</td>
<td></td>
</tr>
<tr>
<td>Total height(um)</td>
<td>100.8</td>
<td>98.5</td>
<td>102.7</td>
<td>95.7</td>
<td>100.8</td>
<td></td>
</tr>
</tbody>
</table>

![Images showing different approaches and measurements](image)
Approach#2 solder plated on IPD die

<table>
<thead>
<tr>
<th>Ti/Cu/Ni/Sn Ag</th>
<th>In-line measures</th>
<th>X-SEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si THK</td>
<td>Avg 71.4um (69~73um)</td>
<td>63.3um</td>
</tr>
<tr>
<td>Joint THK</td>
<td>N/A</td>
<td>9.6um</td>
</tr>
<tr>
<td>Total Height</td>
<td>N/A</td>
<td>75.4um</td>
</tr>
</tbody>
</table>
3D Structures (developed for BSI)

<table>
<thead>
<tr>
<th>Phase-1</th>
<th>Phase-1 plus</th>
<th>Phase-2</th>
<th>Phase-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Chip level)</td>
<td>(Column level)</td>
<td>(Column level)</td>
<td>(Pixel level)</td>
</tr>
<tr>
<td>u-PAD no. &lt; 100</td>
<td>u-PAD no. ~ row/column no. (k)</td>
<td>Inter-PAD no. ~ row/column no. (k)</td>
<td>Inter-PAD no. ~ pixel no. (M)</td>
</tr>
</tbody>
</table>

Fill factor ~ 85%
Wafer Level Bonding

- With the improved process control, the TVs fabrication problems could be solved.
TVs Electrical Characteristics

- TVs with a low resistance & tight distribution are achieved.
- Robust EM performance in the proposed TVs structure

Daisy chain Rc check

TOV Rc ~ 0.09 ohm/ea

Electro Migration Test
Summary and conclusions

- Deep trench capacitor with density up to 500nF/mm^2 was demonstrated
  - Capacitance density limit for 1.2V is expected to be in the 600-700nF/mm^2 range
  - ESR is comparable to commercially available caps, ESL, VCC, TCC are superior to commercially available discrete components
- Deep trench capacitors used for surface mount can achieve record thickness of ~70-100um
- TSMC developed wafer to wafer bonding processes can be used to assemble dice from different technologies (e.g., trench capacitor with the PMIC)