High Speed Lateral Power Devices

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Outline

• Integrated LDMOS
• Isolation Requirements
• Interconnect & Packaging
• Discrete lateral DMOS & Packaging
• Summary
High Frequency Switching

End solution size is the primary driver
Key Power Device Drivers

- **Rsp important ➔ Key Si cost driver**
  
  BUT

- **R x Qtot(Qgd) & Qrr ➔ Key performance drivers and system cost drivers**

  **ALSO NEED**

- **Reduced parasitics** (gate loop and power loop L, CSI)

**Integration and Integrated LDMOS**
LDMOS

NMOS

S

GATE

D

n+

p-region

n+

n+

p-body

n+ (low doped)

n-

n+

p or n-region

drain extension

low voltage

applied high voltage (Vds)

high voltage

E_h = E_cr

E_s < E_cr

electric field distribution

RESURF

deployment layer

thin 1d

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LDMOS Benefit

- Multi-voltage, Easy to Integrate
- Lowest Qg/Qtot for given Rdson – monolithically integrated
  - Low voltage integrated VDMOS not efficient due to significantly high Rsp

Synchronous Buck Converter – Monolithically Integrated
Vin=12V, Vout=1.5V, I=10A

Flip chip packaging (step gate)

Efficiency (%) vs. Switching Frequency (MHz)

- Int. LDMOS (msrd)
- Pseudo VDMOS (model)

Vin=12V, Vout=1.5V, I=10A

P-well
n-drift

Flip chip packaging (step gate)
Integrated Power Conversion

- Monolithic integration helps reduce both gate loop and power loop inductance

High speed Synchronous Buck Converter
Integrated FET Scaling – Drives Technology

- Integrated FET improvement at TI
  - about 25-30% node-on-node improvement

Timeline
- ~50V ldmos
- ~20V ldmos

Architectural Change
Outline

- Integrated LDMOS
- Isolation Requirements
  - Functionality
  - Efficiency
- Interconnect & Packaging
- Discrete lateral DMOS & Packaging
- Summary
Isolation - Functionality

- Protect circuitry from carrier injection
  - Diode recovery, Substrate bounce/noise
Isolation – Efficiency Improvement

- Integrated guard ring significantly reduces diode recovery loss → enables faster switching
Outline

• Integrated LDMOS
• Isolation Requirements
• Interconnect & Packaging
  – Electro migration
  – Parasitic inductance
  – Size and footprint
• Discrete lateral DMOS & Packaging
• Summary
Interconnect Optimization

- Thick Copper allows direct bonding on top of active device – delivers distributed current
- Enables flip chip package eliminating bondwires

Thick copper and bonding technology
HOTROD™ – Flip chip Package for Power

Flip-Chip Eliminates Wire Resistance & Wire Inductance

Package Bottom

Leadframe

Cu bumps on die

For Power Pins

For Signal Pins

Die

COA

Bump

Solder

Leadframe

HOTROD™

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Outline

• Integrated LDMOS
• Isolation Requirements
• Interconnect & Packaging

• Discrete lateral DMOS & Packaging
  – Path towards higher current
  – Reduced design cycle time
  – Product flexibility

• Summary
Discrete FET Technology

**NexFET™ LV Technology**
- LDMOS with Vertical Current Flow
- High density and low Rdson
- Low gate charge

**NexFET™ MV Technology**
- Planar gate for low gate charge
- SJ Trench for lower Rdson
- Low gate charge & fast switching
Power Loss vs. Frequency for Trench DMOS and NexFET

For same output inductor losses ($I^2R$): Inductor Volume $\alpha (1/F_{sw})$
40% System size reduction by using Lateral channel NeXFET
“Lateral” Discrete FET Flexibility

• Same architecture allows both “drain down” & “source down” structures
• Accomodates functional integration
  – Gate clamp, Gate segmentation, slew control
Stacked Die Packaging – Power Block

Stacked die reduces board space by more than 50%
Power Block – Efficiency Improvement

- About 20% reduction in losses with stacked die
- Similar die temperature/thermal performance
Summary

• Power conversion switching frequency increasing to enable footprint reduction
  – *Switching losses and diode losses more critical*

• Lateral power DMOS structure ideally suited
  – *Can be implemented as integrated or discrete*

• Lower gate and power loop as well as package inductances while maintaining high current interconnect
  – *Monolithic for low/mid current – flip chip*
  – *Stacked die for high current – Cu clip*
THANK YOU