Towards a PowerSoC Solution for Automotive Microcontroller Applications

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Outline

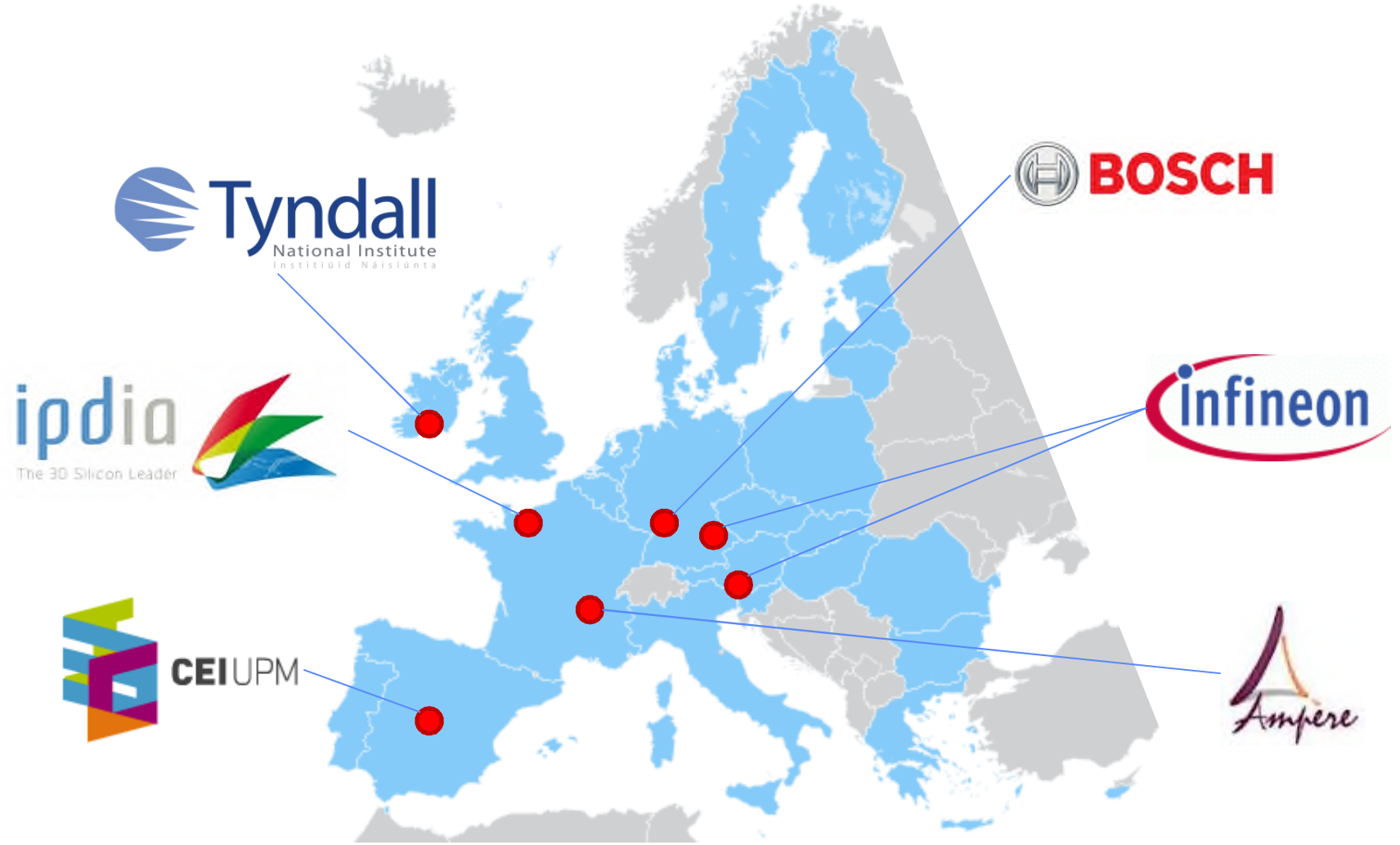
- Automotive uC Application
- Power Conversion Requirements
- Demonstrator System Architecture
  - High-Voltage (HV) DC-DC
  - Low-Voltage (LV) DC-DC
- Challenges:
  - Efficiency, packaging, ringing, EMI, cost
- Conclusions

Universal Power Management Specs

- **Take Up No Space**
- **Cost Nothing**
- **Last Forever**
- **Zero Power Loss**

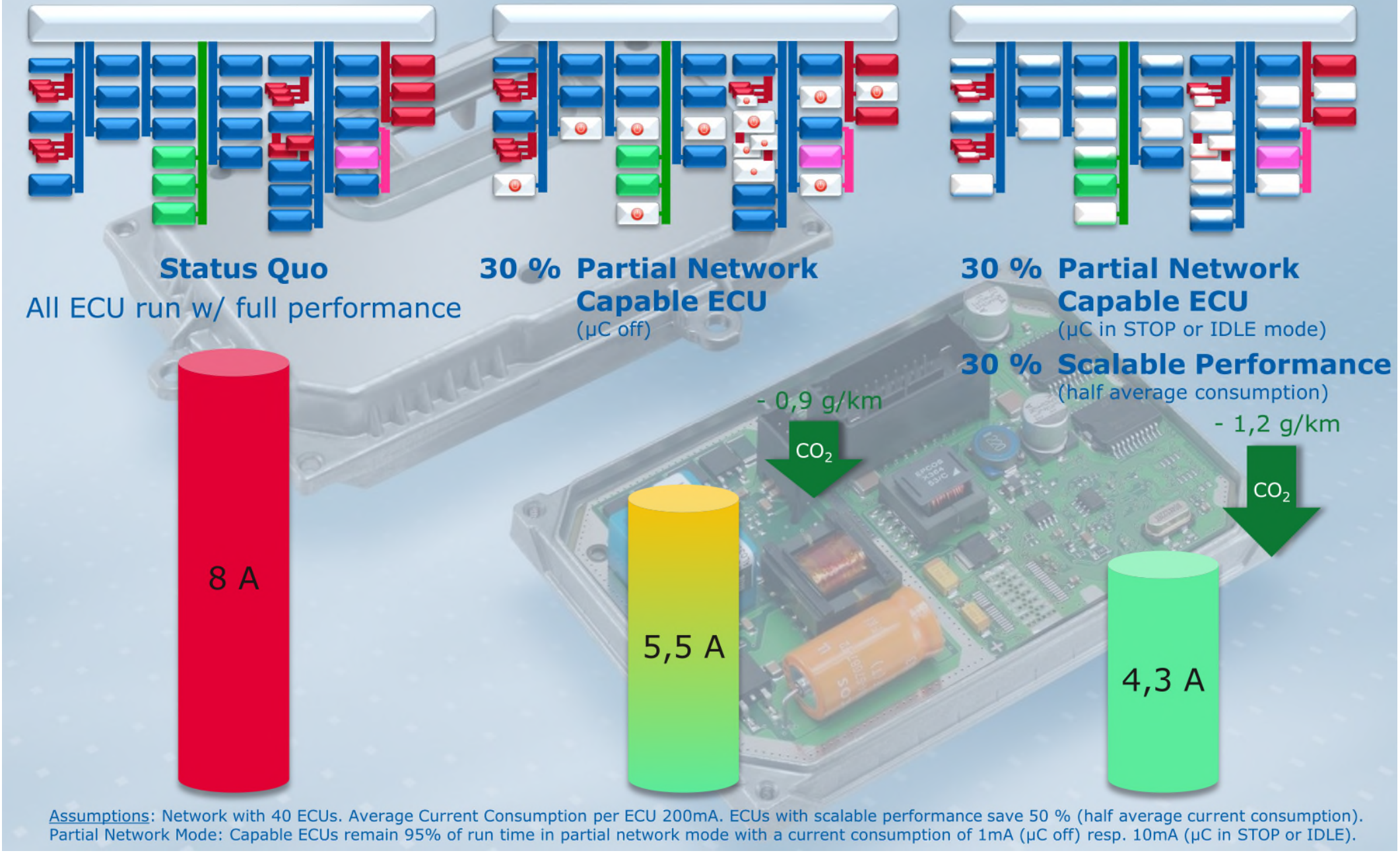
[Cian Ó Mathúna, Tyndall National Institute, Ireland]

PowerSwipe Project Partners

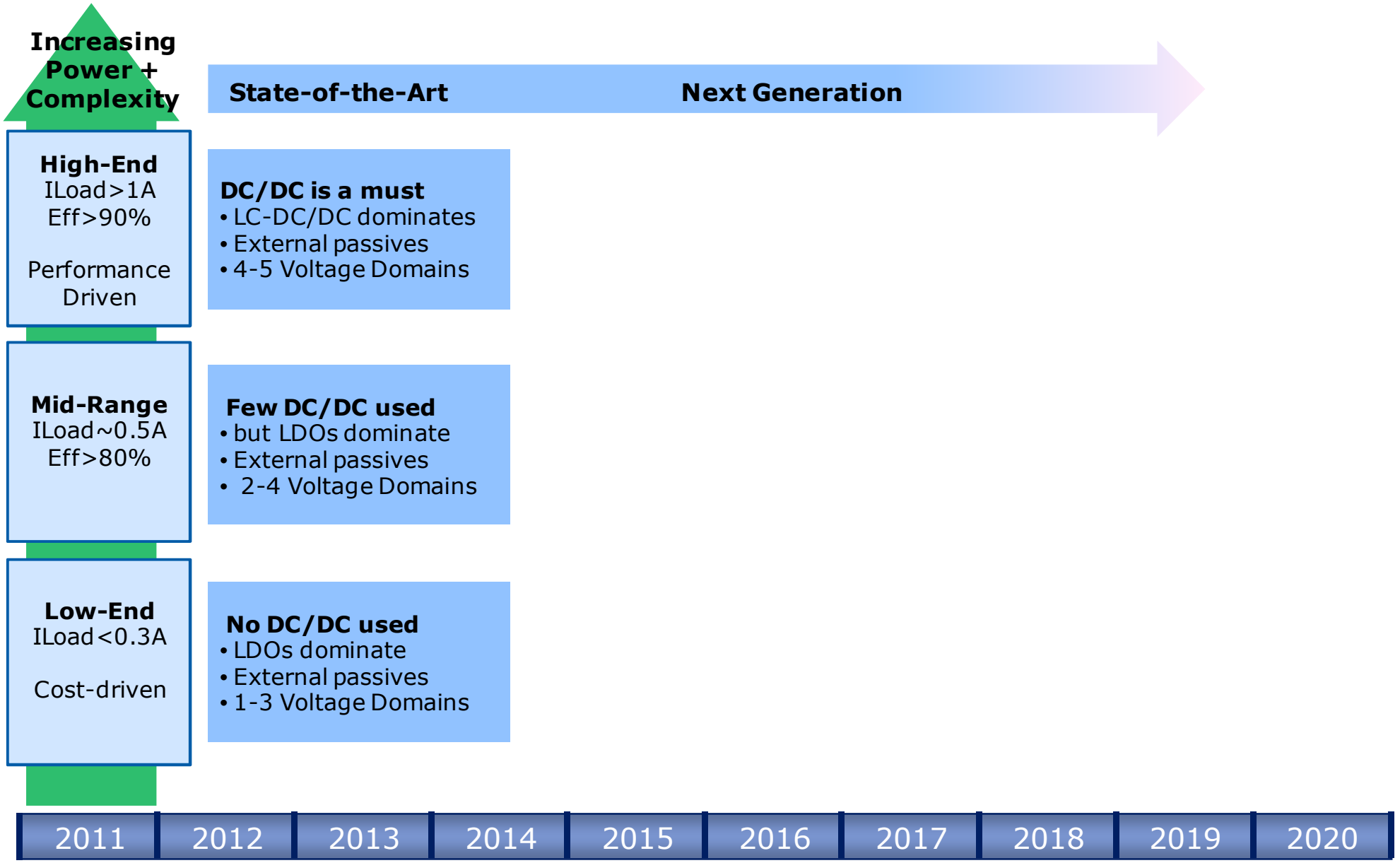


Motivation

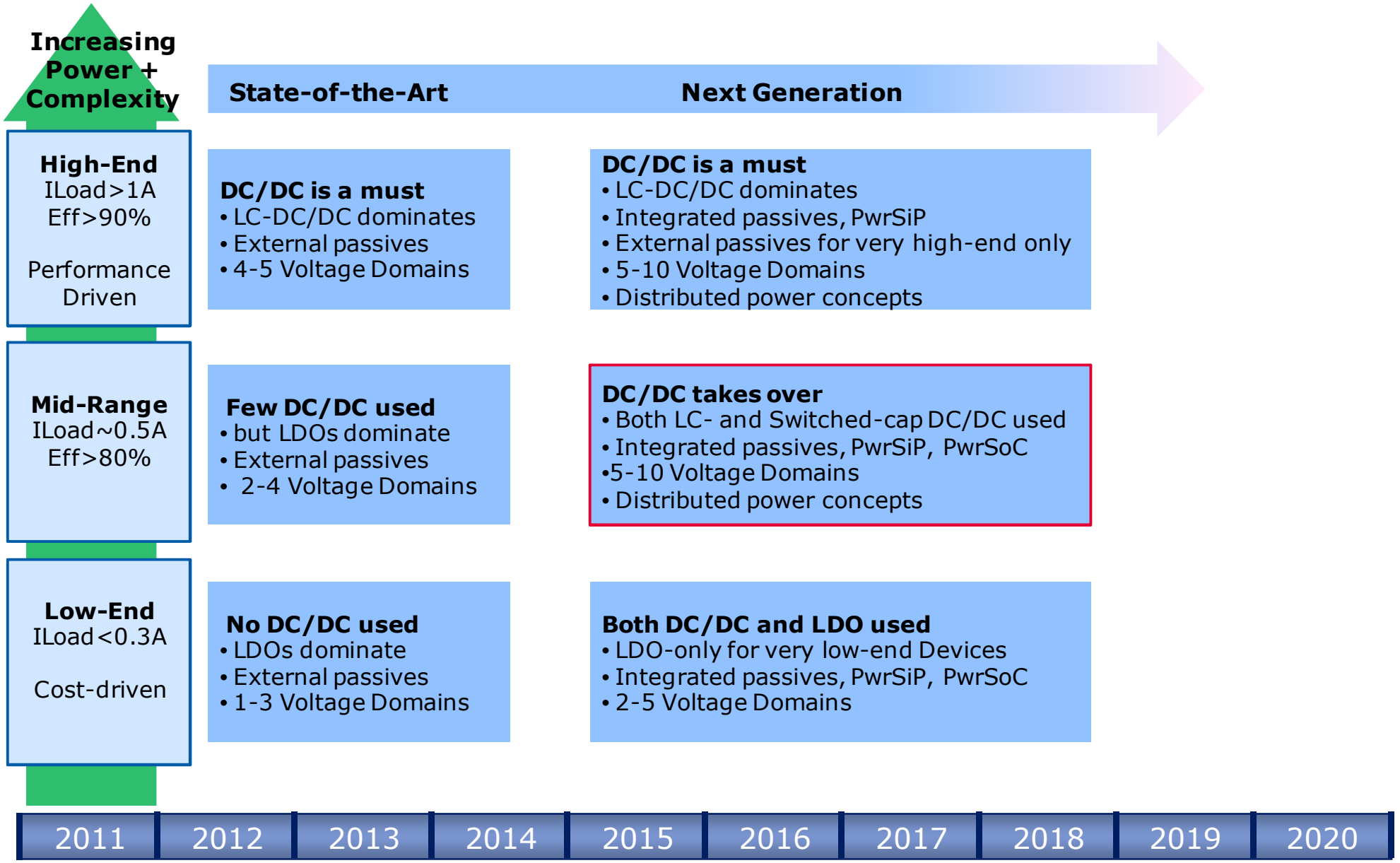
[L.S. Ming, “Architecture Trends Body Electronics”, 2010]



Automotive uC Application

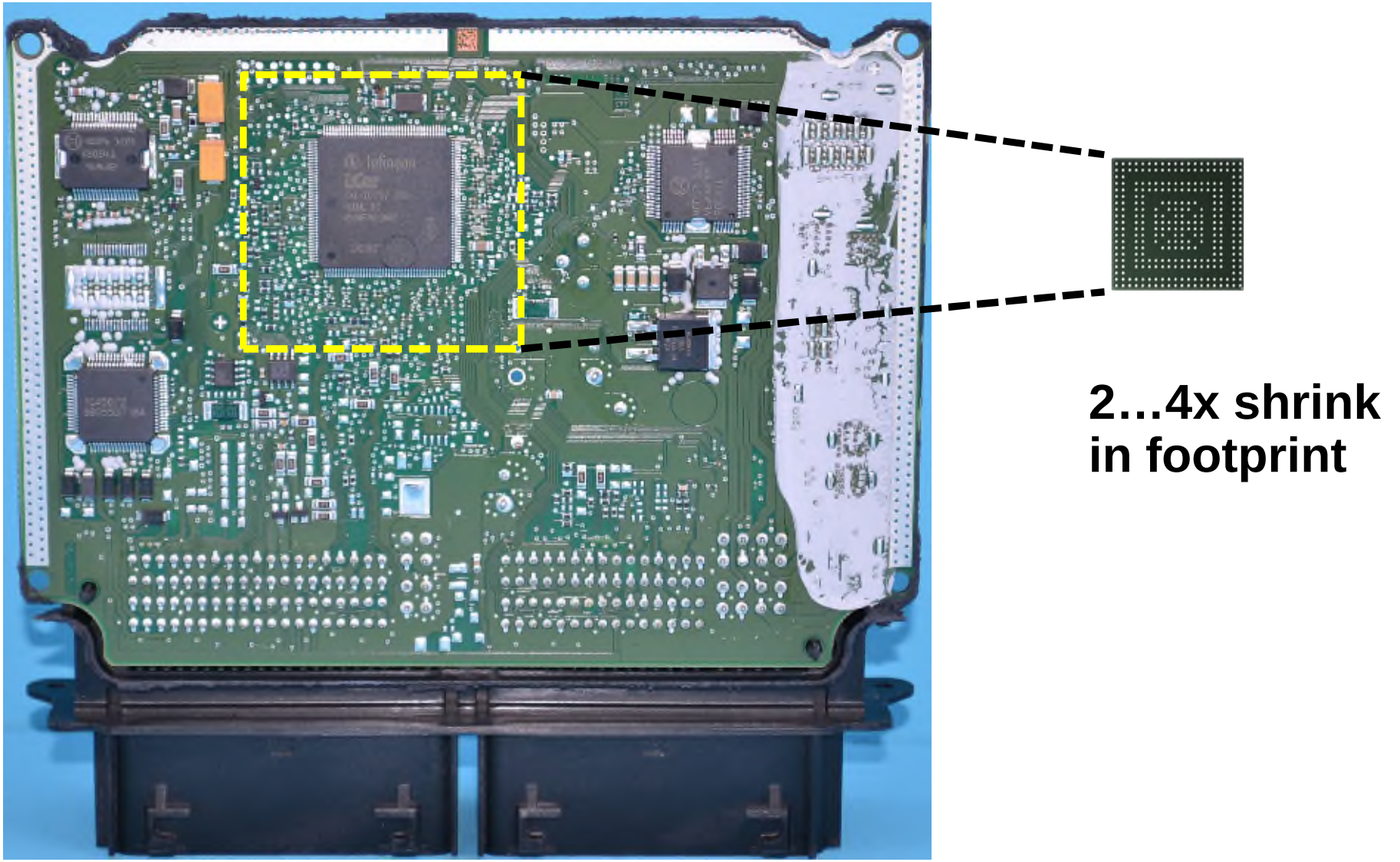


Automotive uC Application



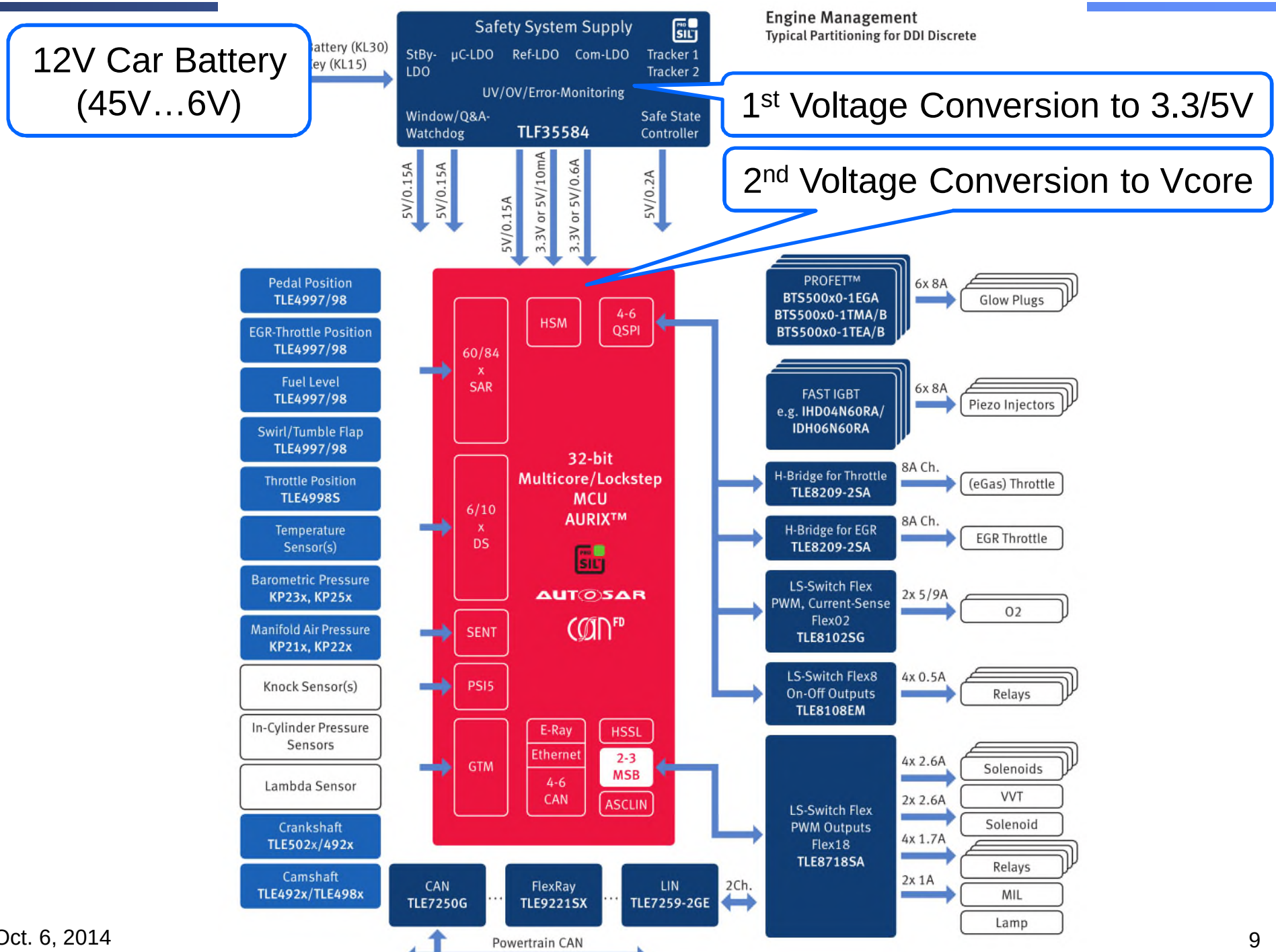
Automotive uC Application

Typical Engine Management Module:



2…4x shrink in footprint

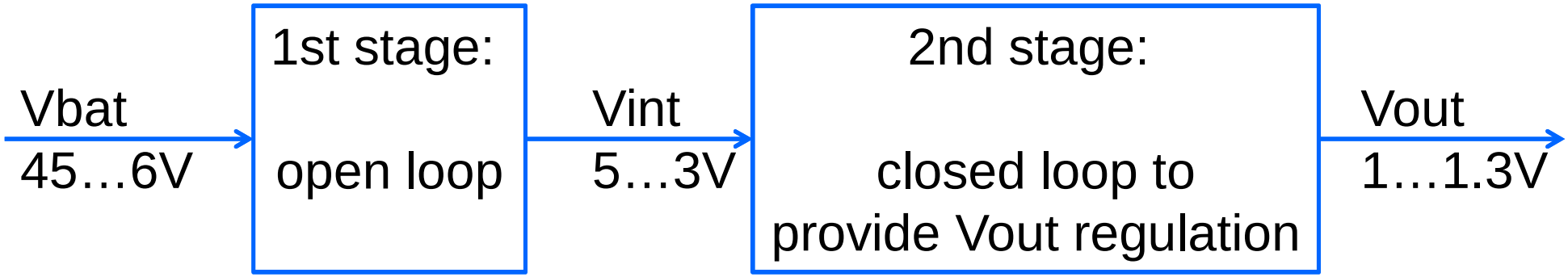
AURIX™ Engine Management System



VBAT Voltage Conversion

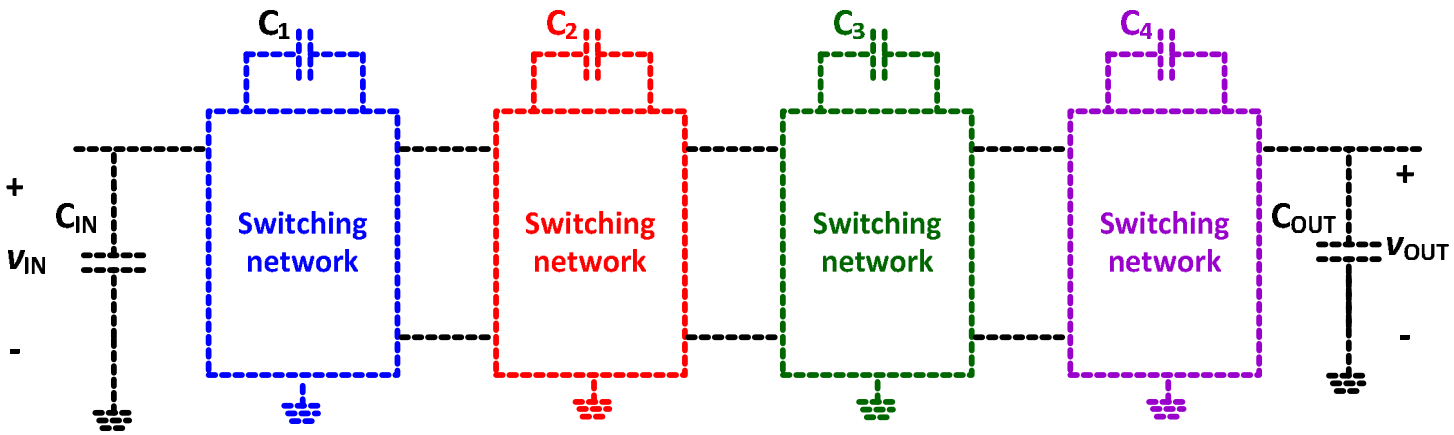
Alternatives to 2-step fixed Vint approach:

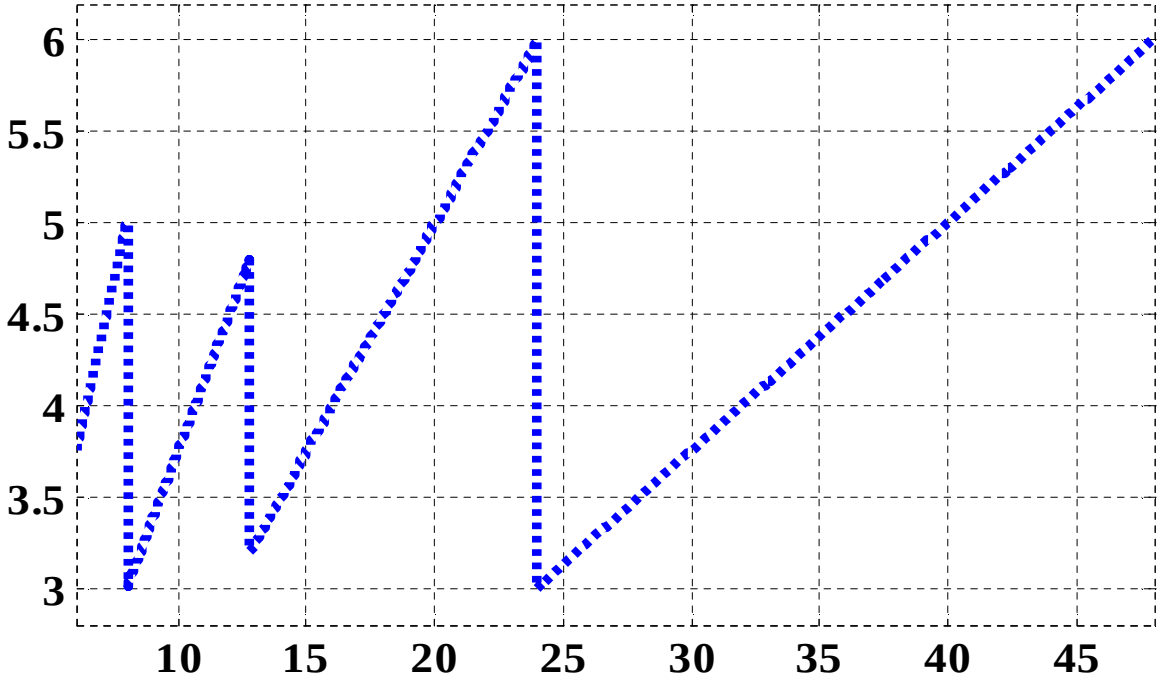
- **1-step**
  …not really…
- **2-step flex Vint:**



Fibonacci SC-DCDC as 1st Stage

[P. Alou, J. Oliver, UPM]

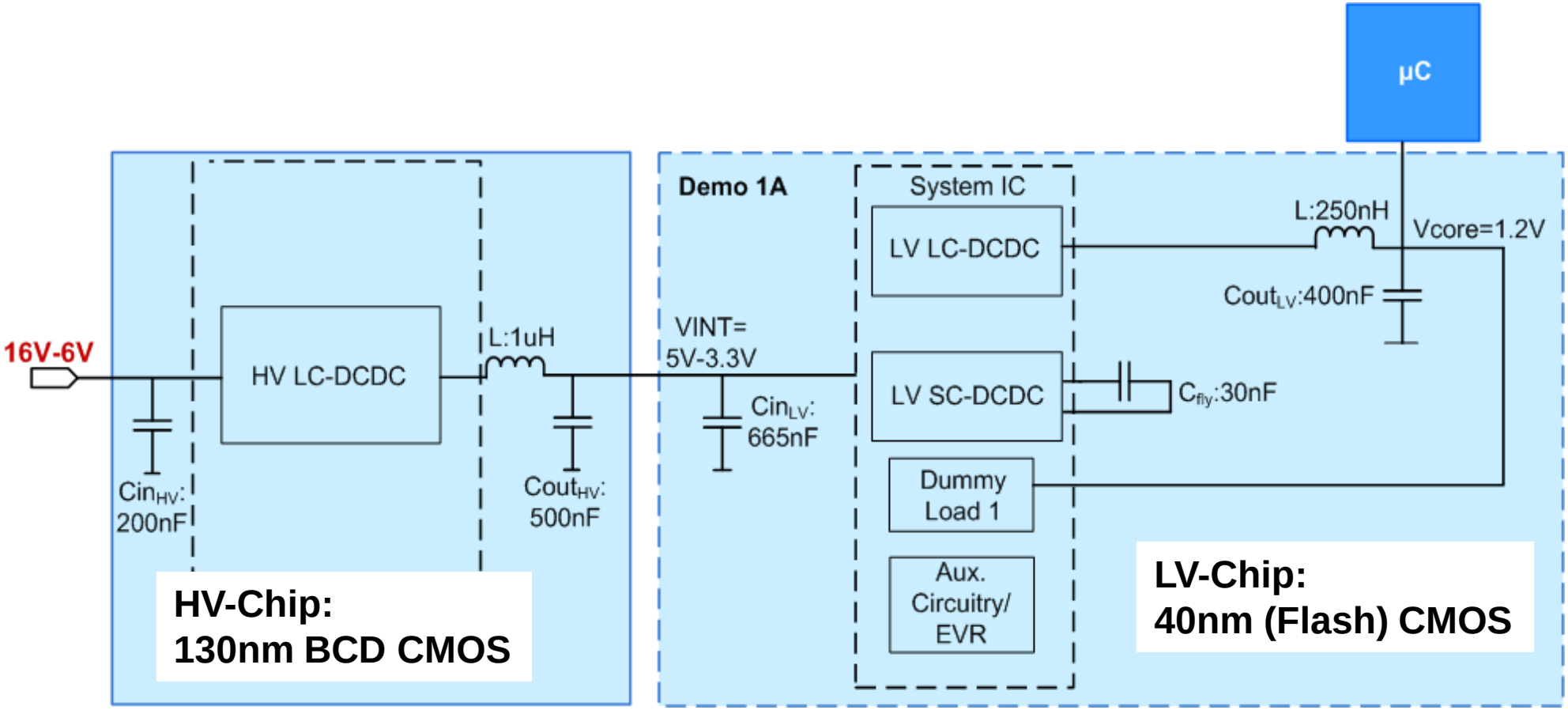




Gains:

5/8, 3/8, 2/8, 1/8

Sytem Overview Demonstrator



Specifications

- **High-Voltage (HV) Chip:**
  - Vin: 16V…6V
  - Vout: 5.0…3.3V
  - Iout_max: 500mA
  - η_peak: 80%
  - PFM, CCM, DCM
- **Low-Voltage (LV) Chip:**
  - Vin: 5V…3.3V
  - Vout: 1.0…1.3V
  - Iout1_max: 500mA
  - Iout2_max: 200mA
  - η_peak: 90%
  - PFM, CCM, DCM
  - (Embedded with uC)

- Technology: Automotive qualified
- Temp range junction: -40deg … +150deg

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- Challenges:
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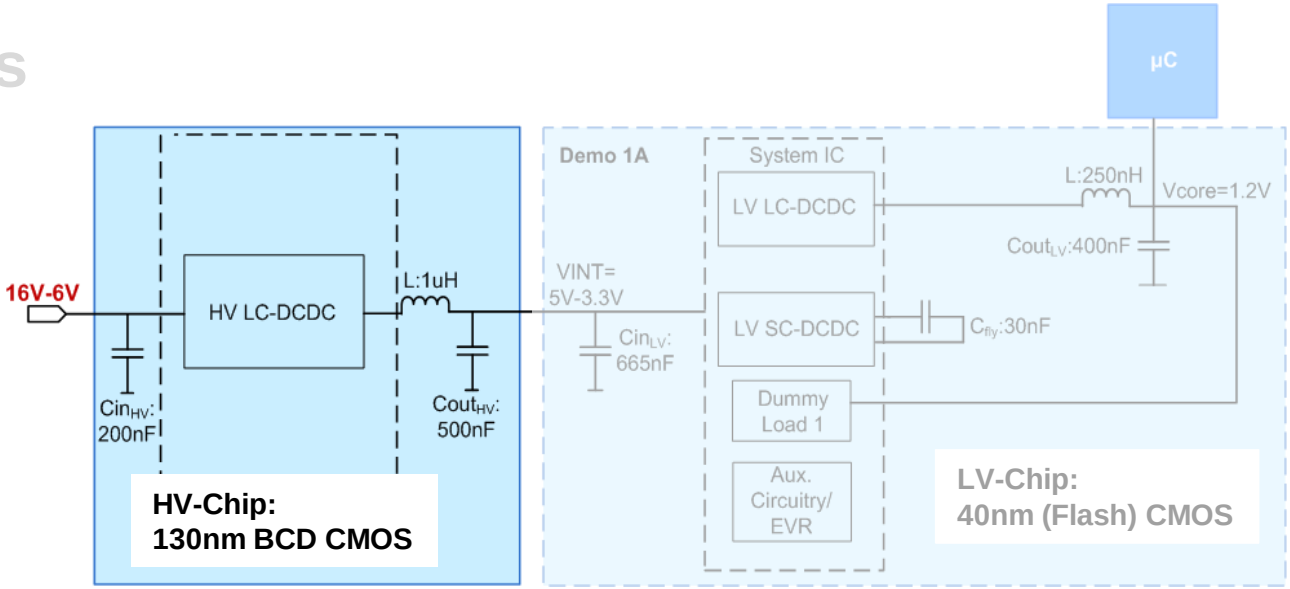
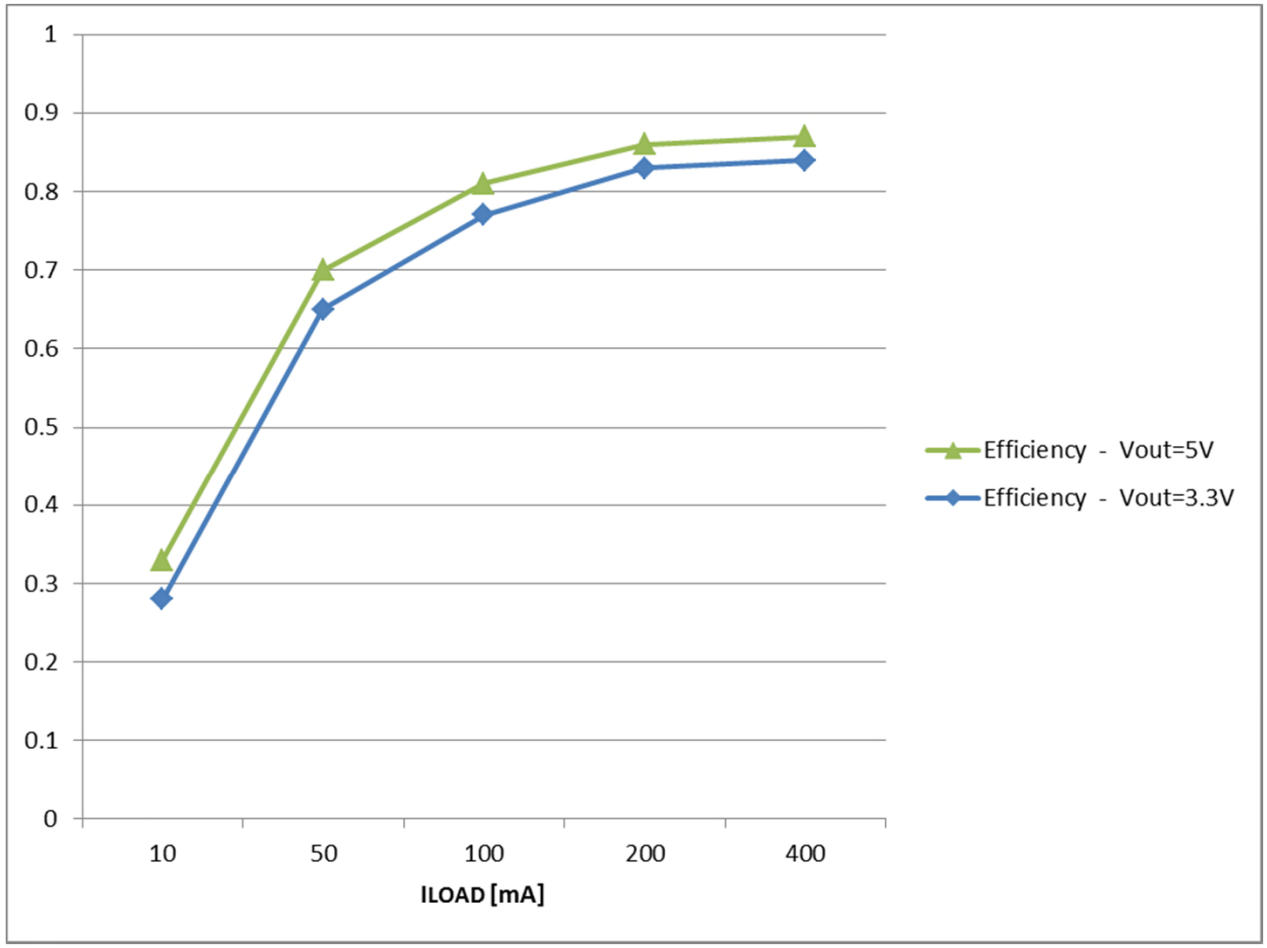


HV DC-DC – Simulated Efficiency

Vin=12V, fsw=10MHz, ESR_L=500mΩ, ESR_{COUT}=50mΩ, ESR_{CHS}=100mΩ, ESR_{CLS}=50mΩ



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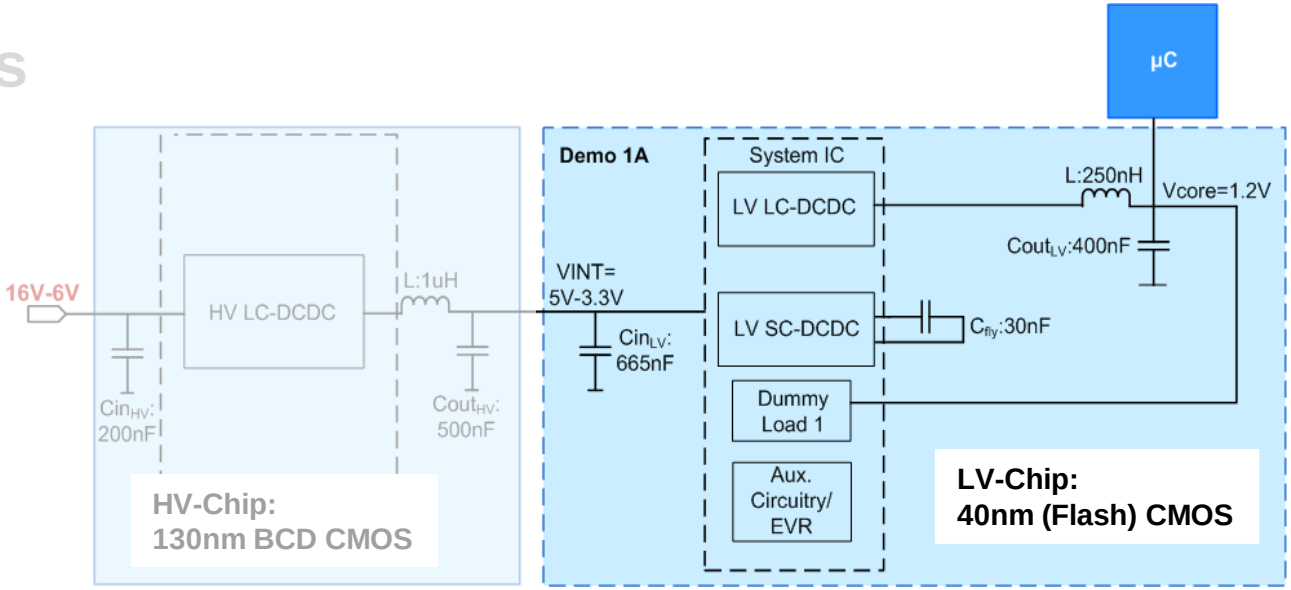
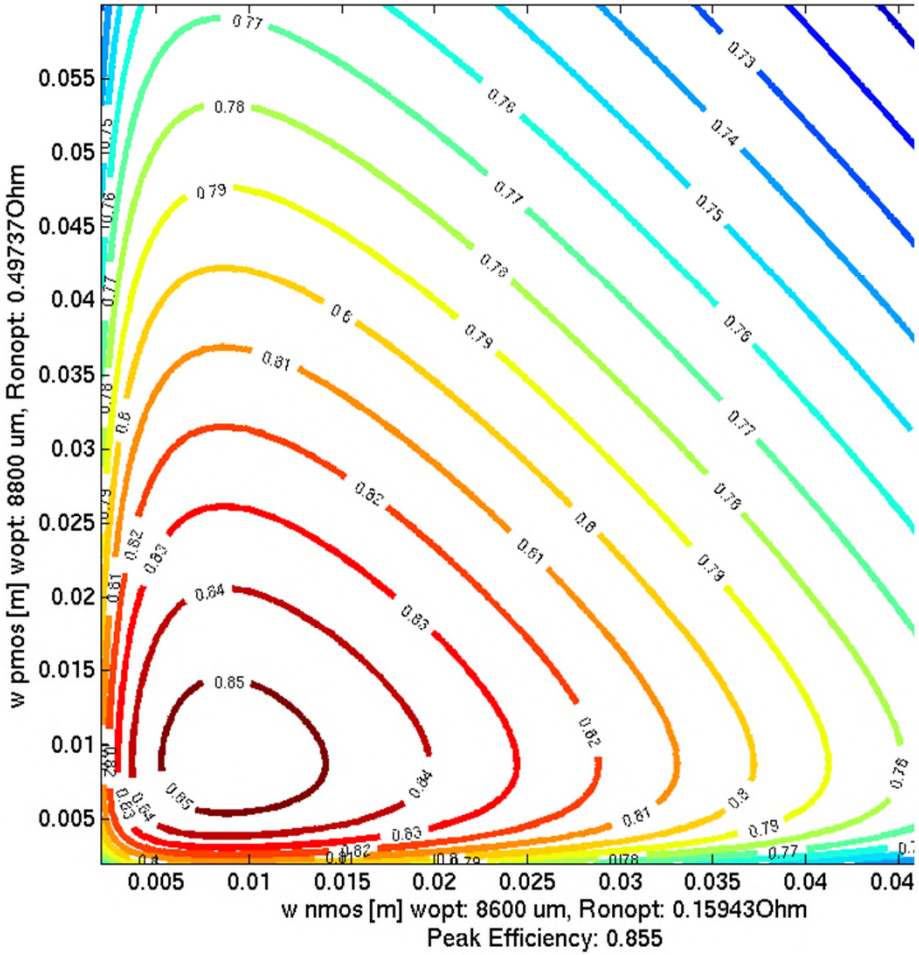
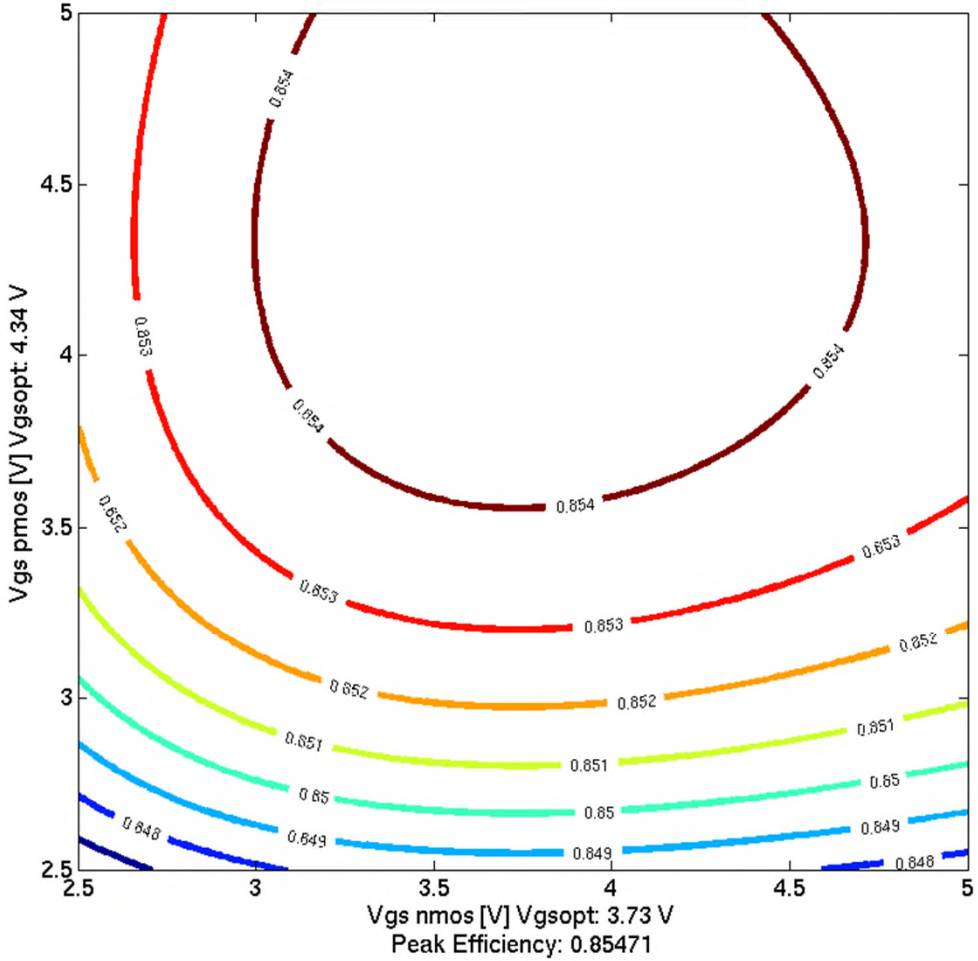


Efficiency Optimization: Device Dimensioning

NMOS vs. PMOS Width:

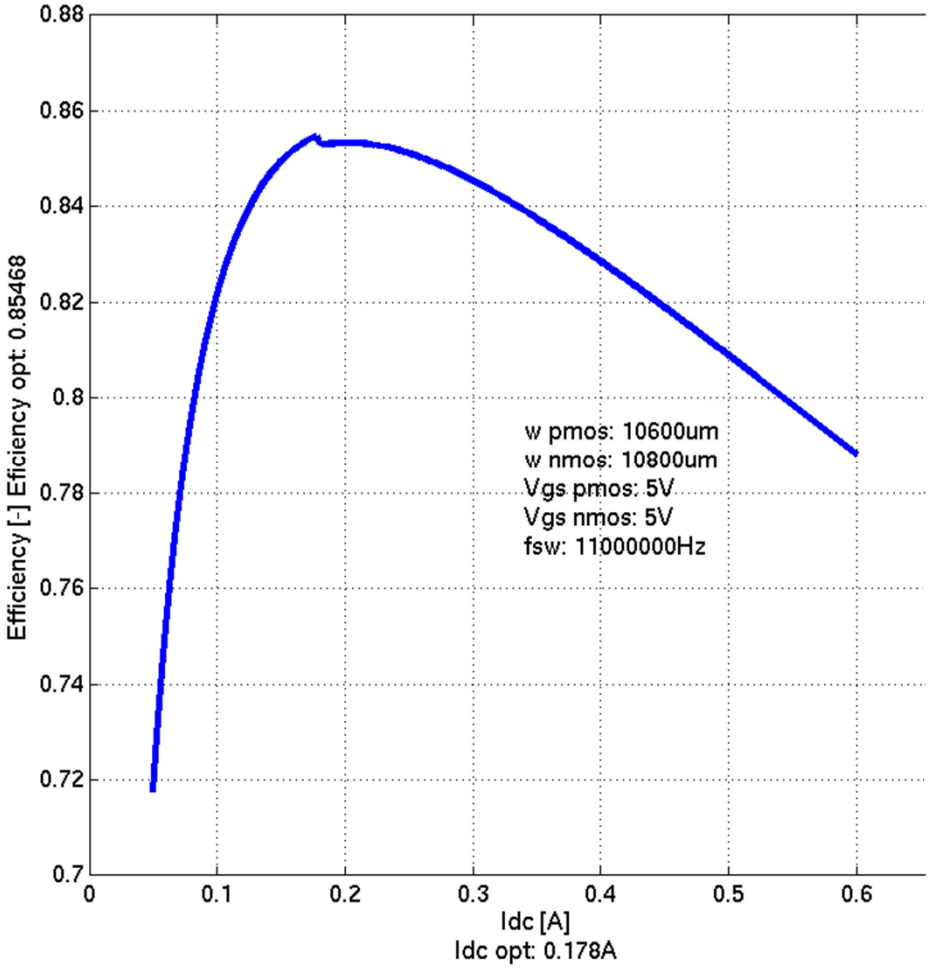


NMOS vs. PMOS Vgs:

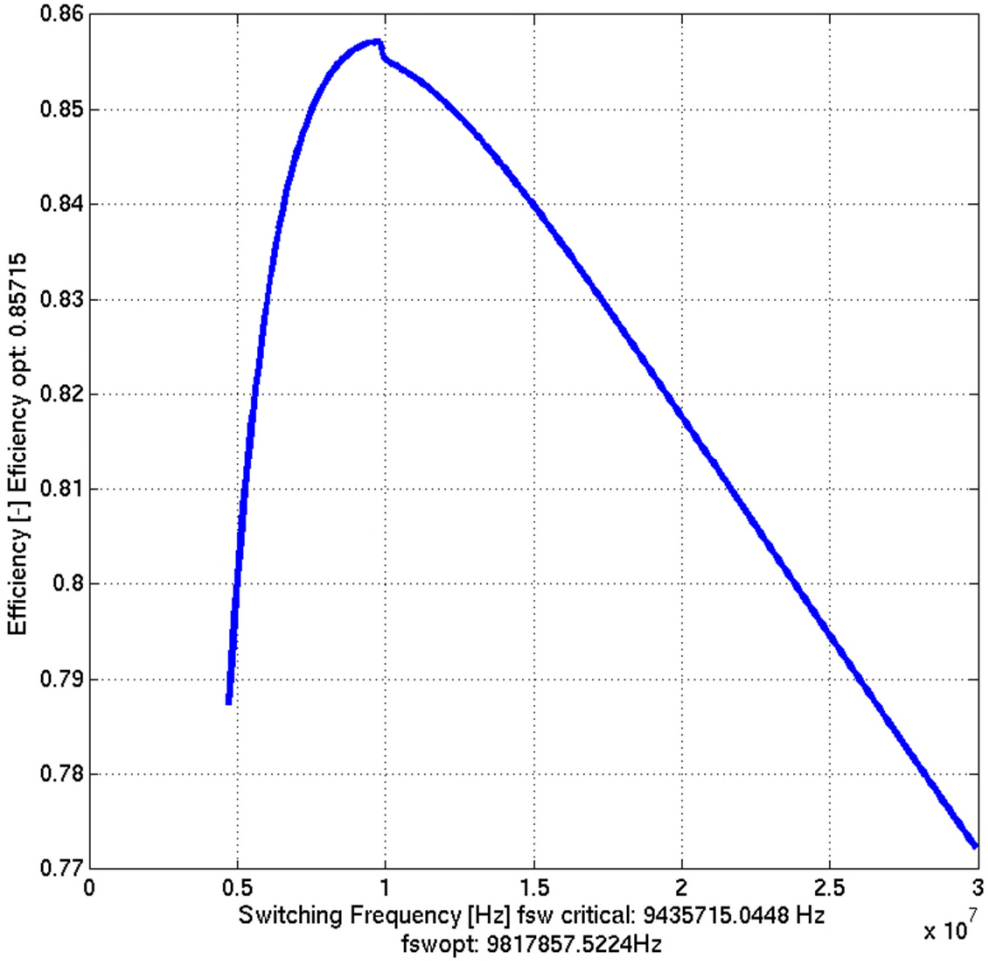


Efficiency Optimization (CCM)

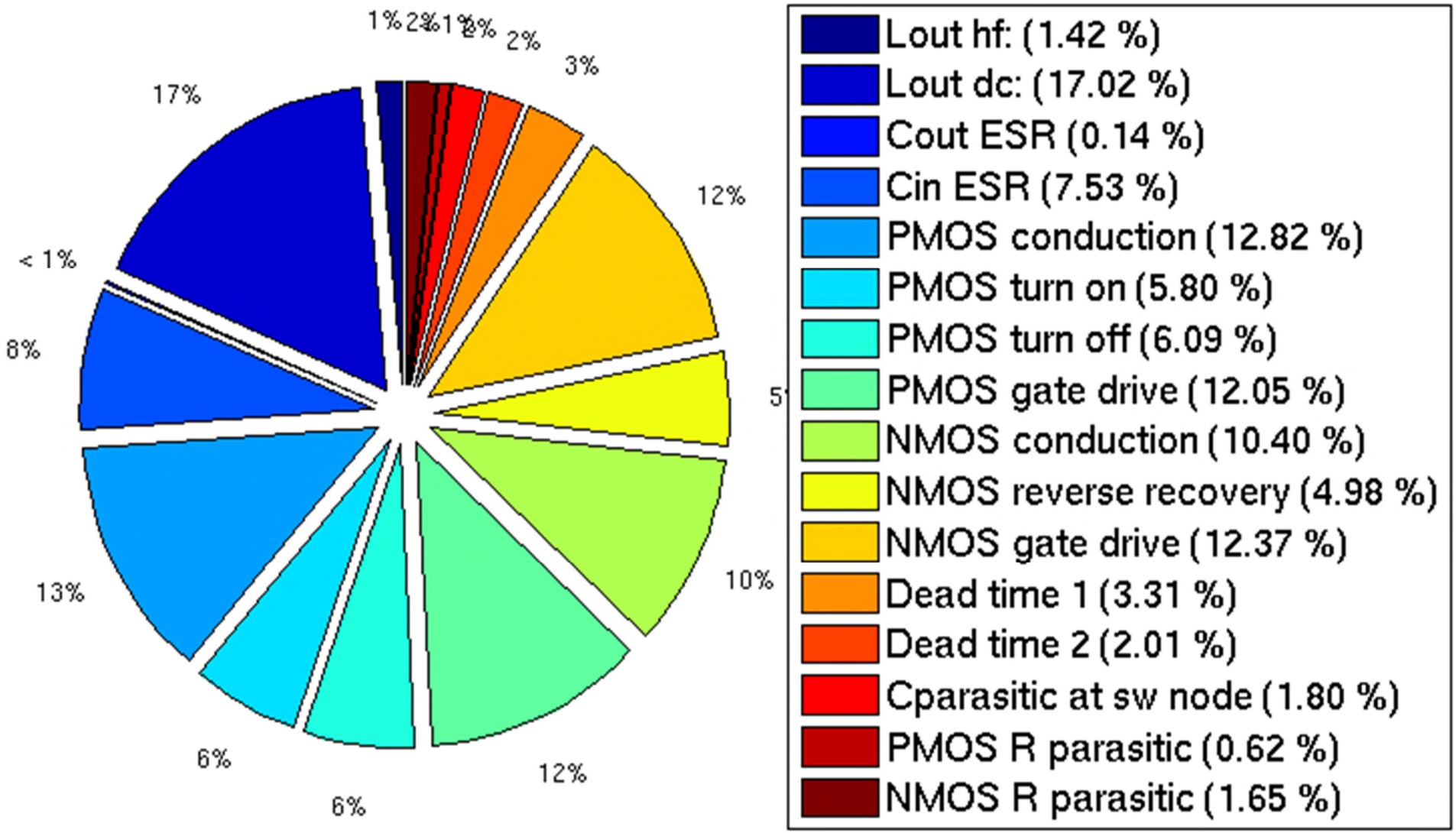
Efficency vs. Load:



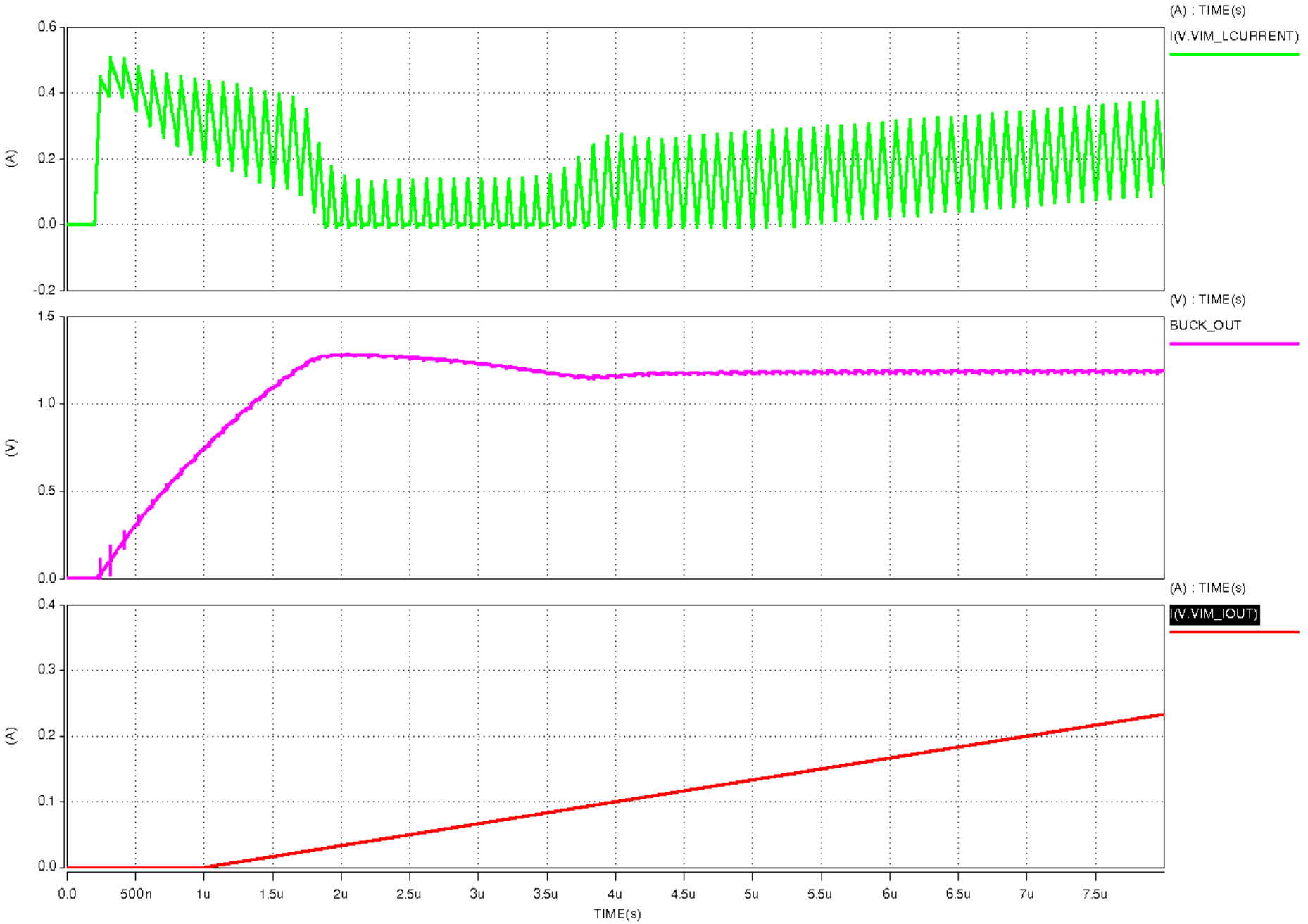
Efficiency vs. Switching Frequency:



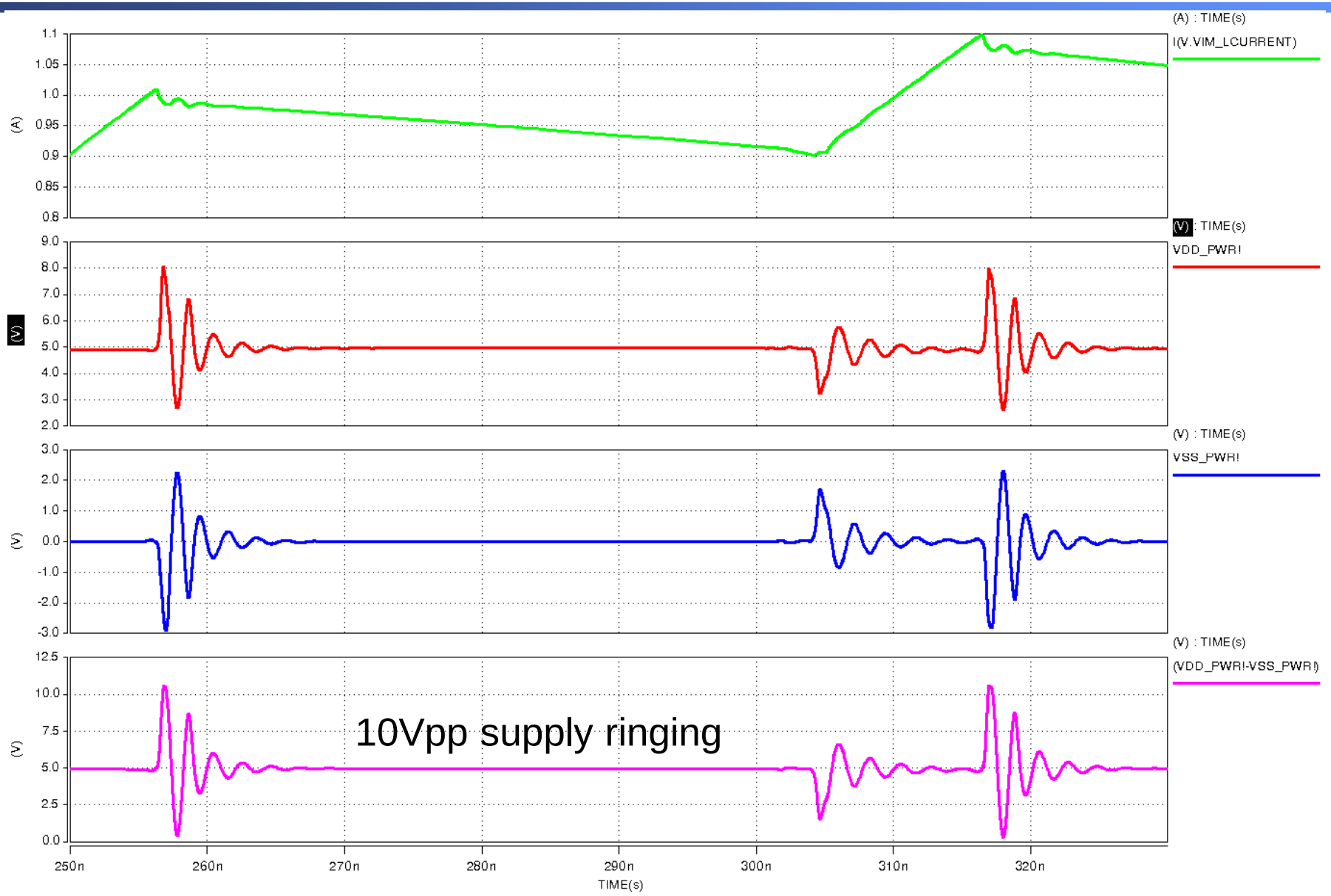
Efficiency Optimization



LV DCDC – CCM/DCM



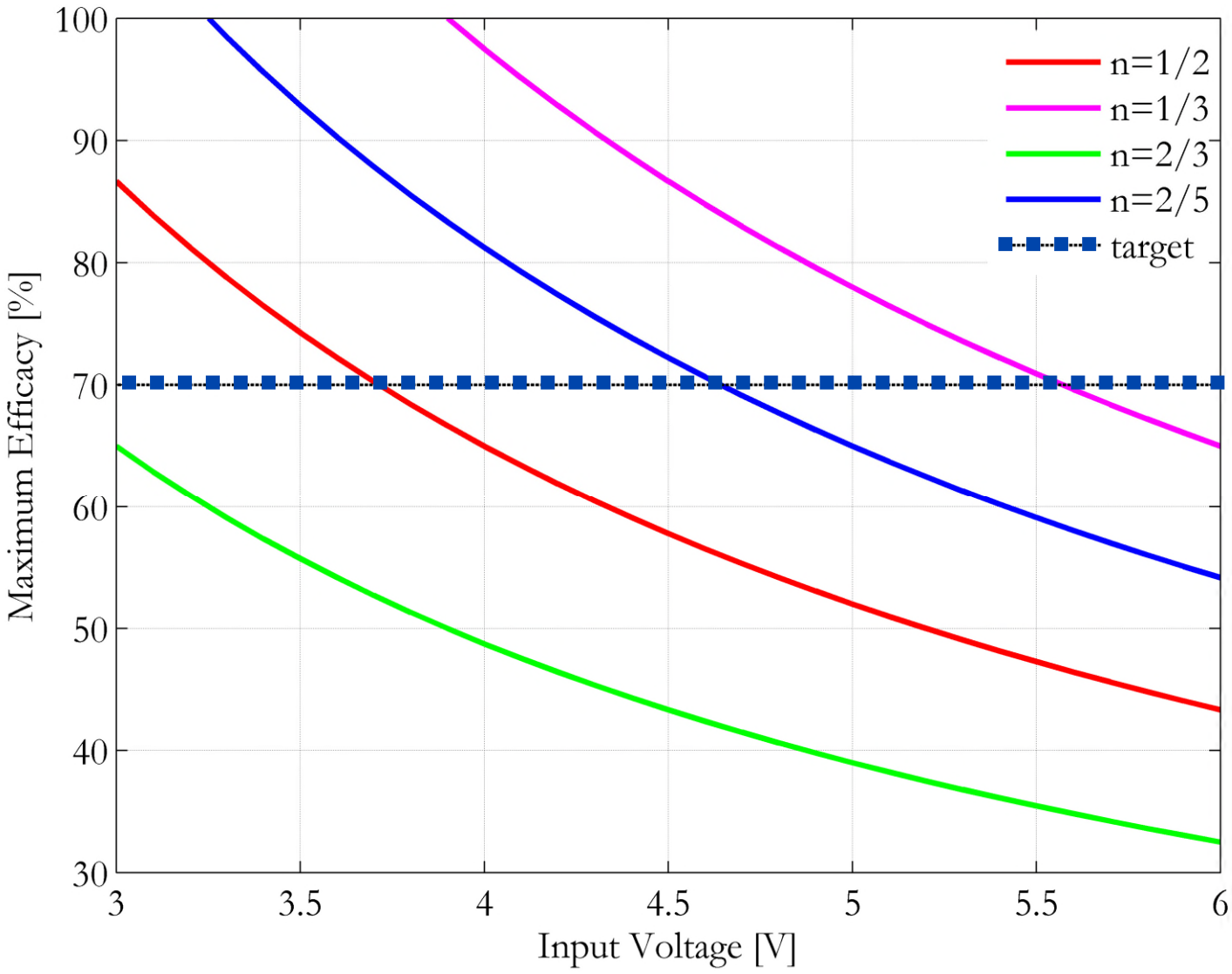
Package Parasitics: HF Issue



→ Without SiP integration such HF switching is not possible at all due to ringing!

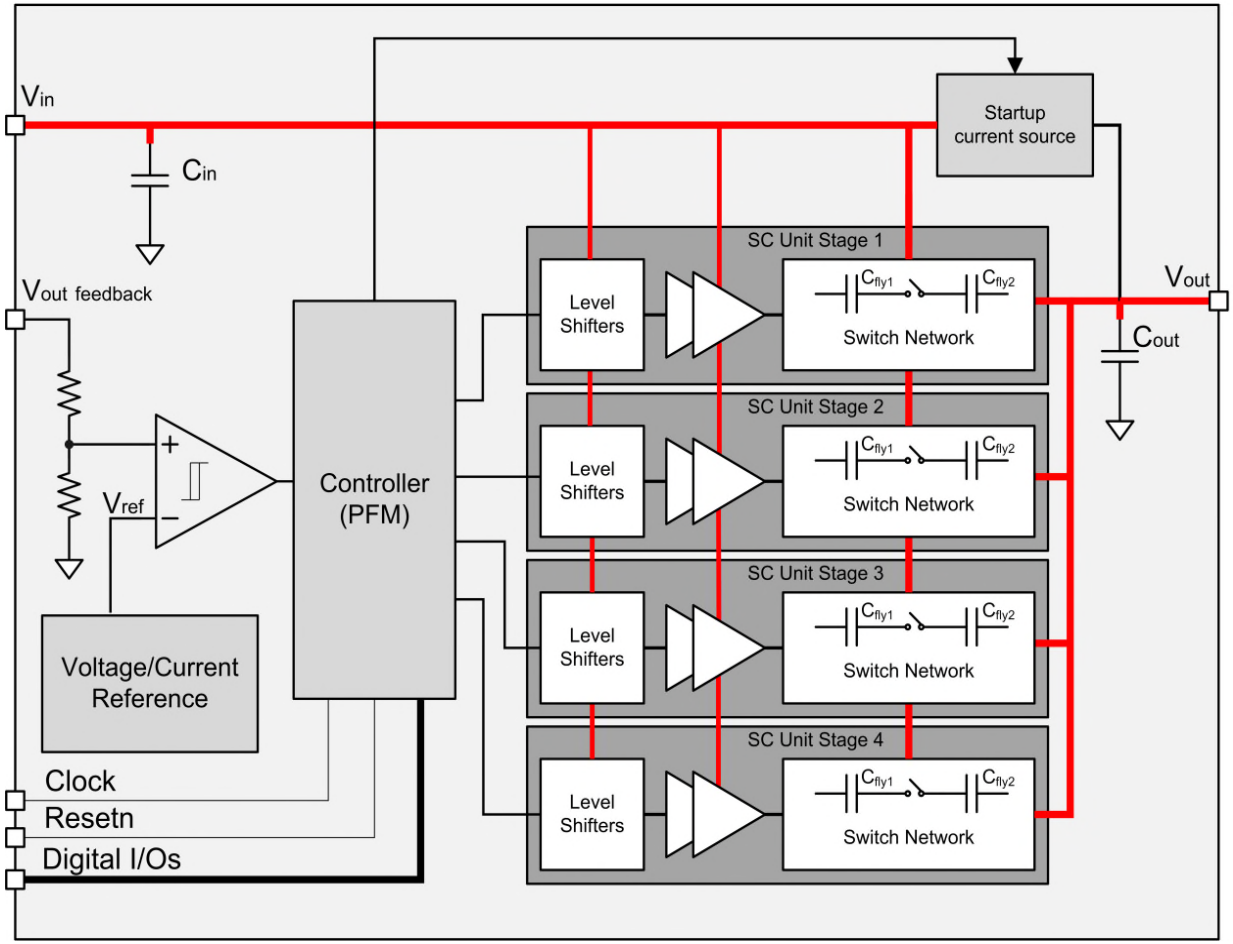
LV Switched-Capacitor DCDC

- **Theoretical Efficiency of an SC DCDC with Different Gain Modes (Vout=1.3V)**



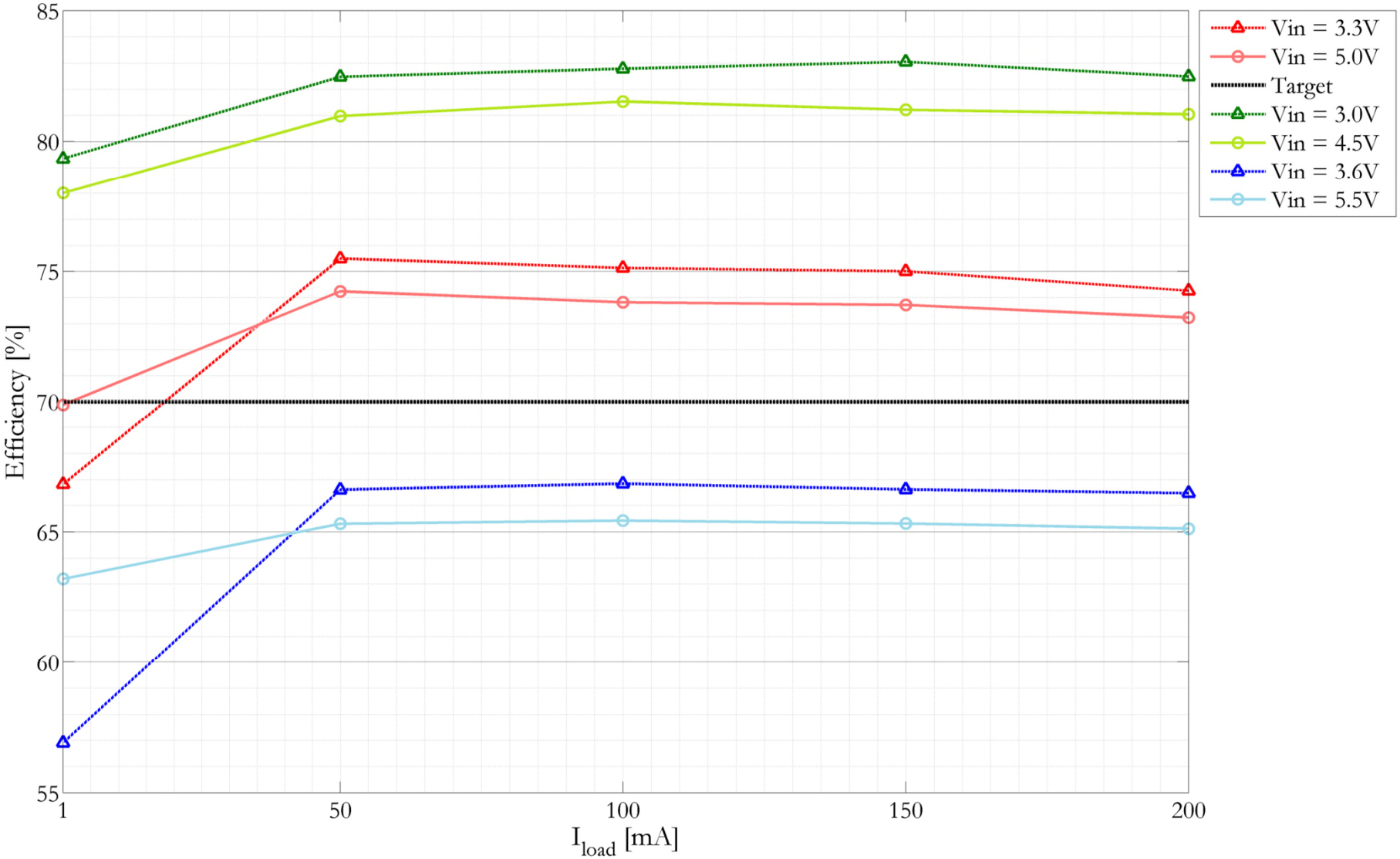
Switched-Cap DC-DC Converter

- **Topology:**
  - **Series-Parallel**
  - **Cfly: 8x 30nF**
  - **Cout: 260nF**
- **Gain modes:**
  - **1/2 (V_{dd}=3.3V)**
  - **1/3 (V_{dd}=5V)**
- **4 Interleaved Stages:**
  - **2 Cfly/stage**
  - **9 Switches/stage**
  - **fsw = 5 MHz max.**
- **Controller:**
  - **Pulse Frequency Modulation (PFM)**

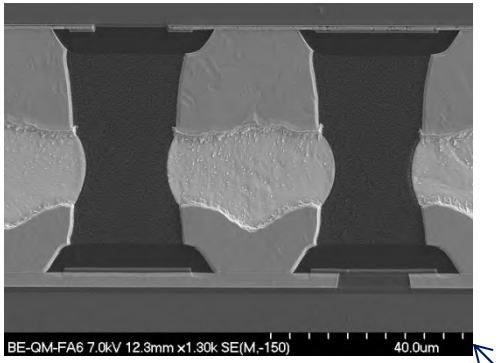


SC DC-DC Converter: Efficiency Simulation

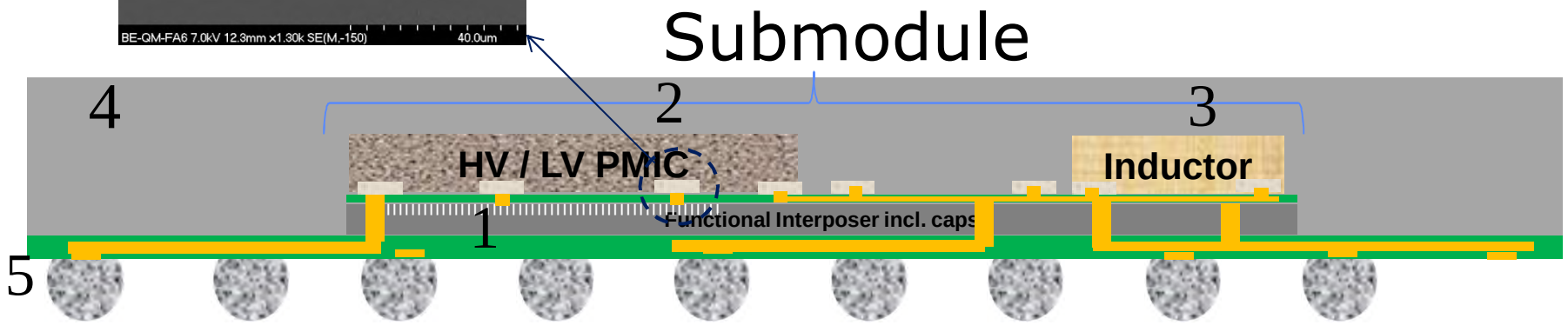
(Vin = 5V: Gain=1/3; Vin = 3.3V: Gain=1/2; Vout=1.3V)



eWLB Packaging



Face to face
with Cu-Pillar/
Sn-cap



1: „Functionalized“ Silicon interposer with integrated Caps and TSVs.
Routing plane on bottom side
2: Active die with Cu-pillar/Sn-cap die to interposer wafer bonded
3: Thinfilm inductor on Silicon die to wafer bonded
4: molded „artifcial wafer“
5: redistribution layer (RDL) and solder balls

Cost ???

Conclusions

- **Main threats towards a product:**
  - **Maintain the performance:**
    - **Concept: Chose optimum partitioning**
    - **Efficiency: Improve DCR of L, ESR of C, power switches**
    - **Ringing: Optimize loop inductances in chip/package**
    - **High energy density → thermal issues**
  - **COST, COST, COST … for high volume products**
    → Get rid of TSVs, reduce cost of inductor and capacitor topology

- **Main Potential:**
  - **Footprint and space constraint products**
  - **EMI critical products: EMI expected to improve due to much shorter current loops on both DCDC-Cin and uC decap**
  - **Exploit concepts with multiple passive components (SC-DCDC) – no pincount constraints**

Acknowledgements

- **PowerSwipe Partners:**
  - Tyndall National Institute / University College Cork, Ireland
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  - Infineon Technologies Austria AG, Austria
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