MicroSiP™ DC/DC Converters
Fully Integrated Power Solutions

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Outline

Illustrate TI’s recent developments in the MicroSiP™ packaging technology

• Overview
• Evolutions in the Subminiature SMPS Space
• MicroSiP™ Package Fabrication Flow
• Electrical Performance Aspect
• Conclusion
MicroSiP™: Overview

✓ Tiniest Solution Size
  • Passives integration ($C_{IN}$, $C_{OUT}$, L)
  • Substrate featuring embedded silicon
  • Small substrate layout

✓ Ease of Use
  • Real pick-and-place solution
  • No external passive components required
  • One-Stop-Shop, reduces HW design and layout efforts

✓ Performance
  • Passive components to match converter
  • Performance optimized layout

2.5W Fully Integrated Power Converter
2.5V to 5.5V$_{IN}$
MicroSiP™: When Solution Size Matters

**Solution size:** >45% smaller vs. discrete solution

**Profile:** <1mm height

**Power density:** ca. 6500W/inch³
Miniature Power Solutions Evolution

- **TPS6200x**
  - Form Factor: MSOP
  - Dimensions: 170mm²
  - Current Density: 4mA/mm²
  - Inductor: L = 10µH
  - Switching Frequency: fSW = 750kHz

- **TPS6226x**
  - Dimensions: 21.5mm²
  - Current Density: 28mA/mm²
  - Inductor: L = 2.2µH
  - Switching Frequency: fSW = 2.2MHz

- **TPS6223x**
  - Dimensions: 12mm²
  - Current Density: 42mA/mm²
  - Inductor: L = 1.0 to 2.2µH
  - Switching Frequency: fSW = 3MHz

- **TPS6262x**
  - Dimensions: 12mm²
  - Current Density: 50mA/mm²
  - Inductor: L = 0.47µH
  - Switching Frequency: fSW = 6MHz

- **TPS8267x**
  - Dimensions: 6.7mm²
  - Current Density: 90mA/mm²
  - Inductor: L = 1µH
  - Switching Frequency: fSW = 5.5MHz

- **TPS8268x**
  - Dimensions: 6.7mm²
  - Current Density: 230mA/mm²
  - Inductor: L = 0.47µH
  - Switching Frequency: fSW = 5.5MHz

Note: Output power level in the range of 1 to 2W
MicroSiP™: Production Flow

Silicon Fab → PicoStar Bump / Probe → PicoStar Back-End

Substrate Embedding

SMT of Passives → Solder Bump → Striptest

Singulation Tape & Reel
MicroSiP™: Assembly Flow

Wafer Fab

Thick Cu Process

Grind/Saw/T&R

Substrate Embedding

Subarray SMT/Singulate/Test/T&R

18x24” Panel
MicroSiP™: Embedding Process

- Thin Copper film adhered to carrier layer
- Pattern Cu film
- PicoStar™ Attach
- Print Adhesive
- Place PicoStar™
- Cure Adhesive
- Pattern Core Pre-preg, Apply Pre-Preg
- Laminate Top Metal Layer, Press/Cure
- Open μvias (laser)
- Drill Thru-Holes
- Cu Plating Via Fill Pattern/Etching
MicroSiP™: SMT Assembly

Solder Print → Reflow

Backside

Solder Print → Pick ‘n Place → Reflow

Frontside

Sub array

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TPS8267x
5.5MHz, 600mA Fully Integrated Step-Down DC/DC

Features
- Input voltage: 2.3V to 4.8V
- Output current: 600mA
- Total solution size: <7 mm²
- Fixed output voltage: 1.0V to 1.9V
  - +/-2% DC accuracy in PWM
- Over 90% efficiency at 5.5MHz Operation
- PWM switching frequency dithering
- Quiescent current: 17 µA
- Power Save Mode:
  - Auto PFM/PWM transition
  - PIN selectable: Auto mode / Forced PWM
- LGA package (2.3x2.9mm, 1mm height)

Benefits
- High switching frequency enables active and passive components integration (PMIC optimum fit).
- PMIC embedded substrate (3D assembly):
  < 7mm² total solution size, sub 1mm solution height
- PWM frequency dithering for improved RF spurious performance. Radiated noise reduction.
- Mode pin for highest efficiency or regulated frequency selection.
- Easy system level integration:
  reduces HW design workload, no more questionable layout.

TPS8267x SIP

![Diagram of TPS8267x SIP with components and connections.](image)

Texas Instruments
Fully Integrated Step-Down DC/DC
Benchmarking Integrated vs. Discrete Solution

DISCRETE SOLUTION

TPS62621

μDC/DC Solution

TPS82671SIP μDC/DC Converter
Efficiency Optimization
Time Controlled PFM Mode Architecture

State-of-the-art multilayer technology offers structures to realize non-linear inductances.

Gradual saturation inductor can help to maximize efficiency. Better tradeoff between Power FETs geometry and converter’s transient response.
Fully Integrated Step-Down DC/DC
AC Regulation Performance

\[ V_{IN} = 3.6\,\text{V}, \, V_{OUT} = 1.8\,\text{V} \]

PFM Mode Operation, \( I_{OUT} = 300\,\text{mA} \)

\[ V_{IN} = 3.6\,\text{V}, \, V_{OUT} = 1.8\,\text{V} \]

Load Transient 20mA to 800mA

\( t_{\text{rise}}, f_{\text{fall}} \sim 100\,\text{ns} \)
The spread spectrum architecture randomly varies the switching frequency by +/-5% to +/-20% of the nominal switching frequency thereby significantly reducing the peak radiated and conducting noise on both the input and output supplies.

The goal is to spread out the emitted RF energy over a larger frequency range so that the resulting EMI is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude.

- Easier to comply with EMI standards.
- Less filtering effort in RF apps, smaller solution size.

Spread bands of harmonics in modulated square signals

\[
B = 2 \cdot f_m \cdot (1 + m_f) = 2 \cdot (\Delta f_c + f_m)
\]
\[
B_h = 2 \cdot f_m \cdot (1 + m_f \cdot h)
\]

Modulation index is defined as: 
\[
m_f = \frac{\delta \cdot f_c}{f_m}
\]

- \(f_c\) is the carrier frequency
- \(f_m\) the modulating frequency
- \(\delta\) is the modulation ratio, 
\[
\delta = \frac{\Delta f_c}{f_c}
\]
TPS8267xSIP
PWM Operation – Conducted Output Noise Measurement

3.6V_{IN} 1.2V_{OUT} @ I_{OUT} = 100mA
No EMI filters

FREQUENCY DITHERING PARAMETERS
1- $\Delta f_c$ = c.a. 500kHz, $f_c$ = 6MHz, $\delta$ = 8.5%
2- $f_m$ = 120kHz, $m_f$ = 4.2
3- Triangular modulation
MicroSiP™: Better Co-Design Options to Reduce Parasitic

VHF Spurious Noise 400~800MHz Band

Fast $\frac{di}{dt} = 1A/400ps$
Switching Freq.: 6MHz

Parasitic ESL reduction is essential for electrical functional and RF performance
MicroSiP™: Improving Electrical, Thermal Performance

Min. Distance $C_f$-to-IC

PicoStar Face-Up

SON-like Thermal Pad
Enhanced $\theta_{JB}$

3600W/inch$^3$

1 mm max
MicroSiP™: Radiated EMI Spectrum

SMPS embedded face-down
SMPS embedded face-up
SMPS embedded face-down + x2 22nF embedded input decoupling
Noise floor

3.6V_{in}
1.8V_{out} @ I_{out} = 550mA
No EMI filters
SSFM enabled
MicroSiP™ DC/DC Converters

1. Smallest solution size: Innovative 3D integration
2. Every SiP is a custom design: Certain rationales need to be met
3. Early-phase co-design from the inside out (IC, passives, substrate)
4. Optimize electrical performance: Comparable efficiency, lower EMI
5. What helps electrically tends to benefit the SiP thermal management