High Frequency Switching Regulators for High Current Slew Rate Applications

Min Kyu Song, Joseph Sankman, and Dongsheng Brian Ma

Integrated System Design Laboratory
The University of Texas at Dallas
E-mail: d.ma@utdallas.edu
Outline

- Background and Challenges
- Integrated Design Solution
  - Near Zero Delay Response
  - \( f_{SW} \) Synchronization
  - Adaptive Voltage Tracking
  - High-Speed Current Sensing
- Design Examples
- Conclusions
Microprocessor Power Supply Trends

Recent Trends:
- Increasing clock frequency.
- Greater number of cores.
- Increasing power dissipation.

Fast Slew Rate: >1A/ns
Extremely High Magnitude

Presented by D. Brian Ma
2014 International Power Supply on Chip Workshop
Key Design Consideration: $f_{SW}$

- $f_{SW}$ Increase
  - To satisfy the **Trends**: $f_{SW} \approx 0.5\text{~to}1\text{GHz}$
  - Dramatic switching power loss increase.
  - Significant efficiency drop.

- Efficiency
- Power Level

Trends of Advanced
μProcessors in Mobile
Applications
Key Design Consideration: Control Scheme

- PWM Control
- Fixed \( f_{SW} \)
- Slow feedback loop – \( \Delta Q_{PWM} \)
- Larger \( V_O \) droop.

**Specifications:**
- \( C_O < 10 \mu F \)
- \( I_{L_RIPPLE} < 200mA \)
- \( I_O \approx 0 \sim 6A \)
- \( I_{O_{SR}} \approx 1A/1ns \)
Key Design Consideration: Control Scheme

- **Hysteretic Control**
- Fast response.
- Still, hysteresis delay. – $t_{DEL}$
- Varying $f_{SW}$. – $t_{SYNC}$
- Physical inductor current slew rate limitation. – $dI_L/dt$

---

Control Scheme → PWM Control (Slow) → Hysteretic Control (Fast)
**Key Design Consideration: Circuit Architecture**

- **Challenges**
  - Synchronization, current-sharing* along with *fast hysteretic control.*
  - Circuit implementation of current sensing at VHF levels.

Conventional Hysteretic Control

- **Fixed Hysteresis Window**
  - Finite hysteresis window size of $V_H - V_L$.
  - Hysteresis delay $\propto V_H - V_L$. 

Presented by D. Brian Ma

2014 International Power Supply on Chip Workshop
Zero Delay Response at $I_O$ Step-Up

- During $(1-D)T$, the control provides a zero hysteresis window, $V(I_L)-V_{HYS}=0$.
- When $I_O$ steps up during $(1-D)T$, $V_G$ turns on without delay since $I_L$ exits the (near-) zero hysteresis window instantly.
\( f_{SW} \) Synchronization

- At \( V_{CLK} \) pulse, \( V_{HYS} \) is reset to \( V_H \).
- \( V_G \) turns on instantly when \( V_{HYS} \) hits \( I_L \).
- \( V_G \) remains on until \( I_L \) reaches to \( V_{HYS} \).
- The leading edge of DT is synchronized to \( V_{CLK} \).
**Synchronization Recovery Scenario**

- At the next $V_{CLK}$ pulse, $V_{HYS}$ is reset to $V_H$, triggering $V_G$ on.
- Leading edge of $V_G$ is synchronized to $V_{CLK}$.
- $I_L$ is stabilized within a few cycles.
Adaptive Voltage Tracking

• As $V_{\text{REF}}$ increases, $V_{\text{ERR}}$ increases, causing the slope of $V_{\text{HYS}}$ to become shallower.

• Sensed $I_L$ takes longer to intersect $V_{\text{HYS}}$, causing an instantaneous duty ratio time change, $\Delta DT$. 

Presented by D. Brian Ma

2014 International Power Supply on Chip Workshop
**I_L-Sensing Limitations on VHF Operation**

**Transistor R_DS Sensing**

- $L_X$-spiking.
- Discontinuous.
- Wide-bandwidth amplifier required.

**Series R_SENS Sensing**

- Continuous.
- Power loss.
- Wide-bandwidth amplifier required.
**I_L-Sensing Limitations on VHF Operation**

**Pros:**
- Continuous $I_L$ sensing.
- No additional power loss from series R.

**Cons:**
- Small DCR.
- Insufficient current sense gain requires additional wide-bandwidth amplifier.

More power consumption as $f_{SW}$ increases!
Emulated AC+DC Current Sensor

- Split the AC (fast) and DC (slow) portion of $I_L$, amplify them separately, and combine them together.
- It eliminates the need for a power hungry wide-bandwidth amplifier in order to amplify the $V_{DCRs}$. 

Presented by D. Brian Ma

2014 International Power Supply on Chip Workshop
Example 1*: PMIC for High $I_0$ Slew Rate APs

- ZDS Hysteretic Control
- 4-phase synchronization
- Cycle-by-cycle current sharing.
- Adaptive transistor sizing with forced-CCM and $I_L$-sensed burst mode control


Presented by D. Brian Ma

2014 International Power Supply on Chip Workshop
**Results: Transient Response**

- 5A load step with >1A/1ns slew rate is tested with 2×470nF (10mΩ ESR) filtering output capacitor.
- Forced-CCM operation is temporarily active during the $I_o$ step down.
## Performance Comparison

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Control</strong></td>
<td>PWM</td>
<td>Hysteretic</td>
<td>Hysteretic</td>
<td>ZDS Hysteretic</td>
</tr>
<tr>
<td><strong>Current Sharing</strong></td>
<td>Master-Slave</td>
<td>Cycle-by-Cycle</td>
<td>None</td>
<td>Cycle-by-Cycle</td>
</tr>
<tr>
<td>$V_{IN \text{ (MAX)} \text{ (V)}}$</td>
<td>1.2</td>
<td>1.2</td>
<td>4.9</td>
<td>3.3</td>
</tr>
<tr>
<td>$V_{OUT \text{ (V)}}$</td>
<td>0.6-1.05</td>
<td>0.9</td>
<td>0.86-3.93</td>
<td>0.7-2.5</td>
</tr>
<tr>
<td>$f_{SW \text{ (MHz) (phases)}}$</td>
<td>100 ($\times$4)</td>
<td>233 ($\times$4)</td>
<td>32-35 ($\times$4)</td>
<td>40 ($\times$4)</td>
</tr>
<tr>
<td>$L \text{ (nH)}$</td>
<td>8</td>
<td>6.8</td>
<td>110</td>
<td>78</td>
</tr>
<tr>
<td>$C_{OUT \text{ (µF)}}$</td>
<td>0.00187</td>
<td>0.0025</td>
<td>0.2</td>
<td>0.94</td>
</tr>
<tr>
<td>$I_{MAX \text{ (A)}}$</td>
<td>1.2</td>
<td>0.3</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td><strong>Load Step (mA/µs)</strong></td>
<td>180 / 800</td>
<td>150 / 0.1</td>
<td>300 / 30</td>
<td>5000 / 5</td>
</tr>
<tr>
<td>1% $t_{settle \text{ (µs)}}$</td>
<td>$\sim$2000</td>
<td>$\sim$30</td>
<td>$\sim$350</td>
<td>230</td>
</tr>
<tr>
<td>$V_{OUT \text{ Droop (%)}}$</td>
<td>6.7%($V_{OUT}$=0.9V)</td>
<td>10%($V_{OUT}$=0.9V)</td>
<td>10%($V_{OUT}$=1.8V)</td>
<td>9.8%($V_{OUT}$=1.2V)</td>
</tr>
<tr>
<td><strong>Peak Efficiency (%)</strong></td>
<td>82.4</td>
<td>83.2</td>
<td>80</td>
<td>86.1</td>
</tr>
</tbody>
</table>
Example 2*: Envelope Modulator for LTE PAs

- Dual-phase **switching converter-only** topology.
- Adaptive Voltage Tracking (AVT) control.
  - Fast hysteretic response.
  - Clock sync. for predictable noise

Key Results

Specs:
- 2-W PA
- $V_{IN} = 3.3$ V
- 10-MHz LTE
- The dual-phase converter
- synchronized at 40MHz with 180° phase shift.

Proposed 2-Phase 40MHz DC-DC Converter (DC input reference)
Proposed Supply Modulator (Tracking 10MHz LTE envelope signal)
Conclusion

- Current SoCs face speed bottleneck imposed by slow and bulky power management solutions.
- Strong demands for “smart” power and performance control push the power management to be achieved on-chip.
- As high density, high frequency and high speed become necessary, they create unprecedented design challenges.
- Cross-layer design efforts are needed in order to achieve desired performance breakthroughs.
Acknowledgements

This work is in part supported by the U.S. National Science Foundation under the research contracts CCF-0844557 and DGE-1147385 and the Semiconductor Research Corporation under the research contract GRC 1836.139.