Integration of GaN Supply Modulators and RF Power Amplifiers

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\textsuperscript{1}CU-Boulder Colorado Power Electronics Center (CoPEC): drain supply modulators
\textsuperscript{2}CU-Boulder microwaves research group: RFPAs and transmitter systems
\textsuperscript{1,*}now with AMD
System: RF Transmitters

Each site has between 3 and 12 transmitters!
System Efficiency Improvement Objectives

- Higher reliability
- Lower system cost
- +In mobile platforms: battery life

Requires systems approach, co-design of architecture, baseband, RF, and power electronics
CoPEC

Supply Modulation Approach

Supply modulator performs a form of “envelope tracking” (ET) to achieve linearity and efficiency improvements.
System Operation\textsuperscript{[1]}

\begin{itemize}
  \item Digital
  \item Envelope Modulator
  \item Up Converter
  \item Analog
\end{itemize}

\textbf{20MHz 40W BTS ET Transmitter}

\textbf{Note: envelope BW can be substantially larger than baseband signal BW}

PwrSOC: ET Transmitter on a Chip

High-frequency (100MHz), wide-bandwidth (20MHz) switcher assisted by 500MHz cascode amplifier

Saturated, harmonically terminated, high-efficiency RFPA

5.4 x 3.8 mm in GaN-on-SiC RF process

Cascode ET amp, 500 MHz BW [5, 6]

100MHz switching ET amp, 20MHz BW [8, 9]

10W, X-Band RFPA [2, 3, 4]
D-mode GaN-on-SiC 0.15 μm RF process

- Intended for RF applications, e.g. RFPA’s, MMIC’s
- Depletion-mode, n-type only, threshold voltage $V_T \approx -3.5$ V
- Device size (gate periphery) $W = N \cdot W_g$
  - $N =$ number of gate fingers
  - $W_g =$ gate width

![GaN-on-SiC HEMT basic unit cell](image1)

![Simplified device layout with 4 parallel cells](image2)
RF PA MMIC Design Example[3]

- Two-stage X-band (10 GHz) power amplifier MMIC
- Class-E output stage: four 0.9 mm devices
- Gain: 20 dB, bandwidth: 1.6 GHz

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Circuit B - Drain Voltage Sweep

Power-added efficiency as a function of output RF output power at different drain supply voltages

<table>
<thead>
<tr>
<th>$V_d$ (V)</th>
<th>PAE (%)</th>
<th>$P_{out}$ (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20.0</td>
<td>59.9</td>
<td>25</td>
</tr>
<tr>
<td>17.5</td>
<td>60.0</td>
<td>30</td>
</tr>
<tr>
<td>15.0</td>
<td>55.0</td>
<td>35</td>
</tr>
<tr>
<td>12.5</td>
<td>50.0</td>
<td>40</td>
</tr>
<tr>
<td>10.0</td>
<td>45.0</td>
<td></td>
</tr>
<tr>
<td>7.5</td>
<td>40.0</td>
<td></td>
</tr>
<tr>
<td>5.0</td>
<td>35.0</td>
<td></td>
</tr>
</tbody>
</table>

Max PAE (%) | 59.9
Max $P_{out}$ (W) | 13.2
Gate size (mm) | 3.6
W/mm | 3.68

Very high frequency switching supply modulator

- Dynamic capabilities suitable for envelope tracking application
  - High bandwidth (20 MHz LTE envelope) and high efficiency (>80%) must be met simultaneously
- Possibilities for SOC integration in the same GaN-on-SiC RF process
# Device switch characteristics

<table>
<thead>
<tr>
<th></th>
<th>$R_{on,s}$</th>
<th>$C_{oss,s}$</th>
<th>$C_{iss,s}$</th>
<th>$Q_{g,s}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulated</td>
<td>2.1 $\Omega \cdot$ mm</td>
<td>0.4 pF/mm</td>
<td>1.5 pF/mm</td>
<td>8.8 pC/mm</td>
</tr>
</tbody>
</table>

### Comparison of 40V devices

<table>
<thead>
<tr>
<th>Device Type</th>
<th>FOM = $R_{on,s}Q_{g,s}$ [pVs]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon MOSFET (e.g. Si 2318)</td>
<td>148</td>
</tr>
<tr>
<td>GaN-on-Si (e.g. EPC 8008)</td>
<td>58</td>
</tr>
<tr>
<td>RF GaN-on-SiC process</td>
<td><strong>19</strong></td>
</tr>
</tbody>
</table>

- **Low device FOM**
- **Zero-voltage-switching (ZVS)**
- **Gate-drive integration**

High-efficiency at very high switching frequency
100 MHz Integrated GaN PWM Buck Converter

100 MHz PWM control signals

20 MHz tracking bandwidth
5-17 V, 10 W peak
100 MHz Integrated GaN PWM Buck Converter

Key challenge: level-shifting high-side gate driver to support very high frequency (100 MHz) PWM control
Standard active pull-up driver

Chip layout: 2.4 × 2.3 mm

Half-bridge power stage

\[ V_{dd} = V_{in} \]

High-side gate driver

Low-side gate driver

<table>
<thead>
<tr>
<th>( Q_{HS} ), ( Q_{LS} )</th>
<th>( D_{HS} ), ( D_{LS} )</th>
<th>( Q_1 ), ( Q_3 )</th>
<th>( Q_2 ), ( Q_4 )</th>
<th>( R_1 )</th>
<th>( R_2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>10x125( \mu m )</td>
<td>10x120( \mu m )</td>
<td>2x25( \mu m )</td>
<td>4x50( \mu m )</td>
<td>300 ( \Omega )</td>
<td>125 ( \Omega )</td>
</tr>
</tbody>
</table>
Active pull-up driver operation

\( Q_{HS} \text{ on, } Q_{LS} \text{ off} \)

\[ I_{Q3} = 13.2 \, mA \]

\( Q_{HS} \text{ off, } Q_{LS} \text{ on} \)

\[ I_{Q1} = 8.5 \, mA \]

\[ P_{d,conduction} = -DV_{ssLS}I_{Q3} + (1-D)(V_{in}-V_{ssHS})I_{Q1} \text{ HIGH} \]

\[ D=0.5, \, I_o=0.25 \, A \]
Modified active pull-up driver\textsuperscript{[8,9]}

Chip micro-photograph: 2.4 $\times$ 2.3 mm

<table>
<thead>
<tr>
<th>$Q_{HS}, Q_{LS}$</th>
<th>$D_{HS}, D_{LS}$</th>
<th>$Q_1, Q_3$</th>
<th>$Q_2, Q_4$</th>
<th>$R_1$</th>
<th>$R_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>20x200$\mu$m</td>
<td>20x100$\mu$m</td>
<td>4x25$\mu$m</td>
<td>4x50$\mu$m</td>
<td>100 $\Omega$</td>
<td>75 $\Omega$</td>
</tr>
</tbody>
</table>
Modified active pull-up driver operation

$Q_{HS}$ on, $Q_{LS}$ off
$I_{Q3} = 25.6 \text{ mA}$

$Q_{HS}$ off, $Q_{LS}$ on
$I_{Q1} = 23.3 \text{ mA}$

$P_{d,\text{conduction}} = -DV_{ssLS}I_{Q3} + (1-D)(-V_{ssHS})I_{Q1}$

$D=0.5$, $I_o=0.25 \text{ A}$

Low driver power loss, and no bootstrap capacitor required
Experimental prototype

- 10-200 MHz PWM switching, ZVS operation (QSW)
- Control: Altera Stratix IV FPGA, 125 ps resolution
- Chip package: 20-pin 4x4mm QFN package
- Filter components
  - Low-ESR capacitors
  - High-Q air-core inductor (47 nH)
Efficiency as a function of switching frequency

Peak efficiency

2.4 × 2.3mm integrated buck switching converter chip
Experimental results at 100 MHz switching frequency

- $P_{out}$ up to 7 W static
- $\sim$ 0.2 W driver loss
- 91% peak power-stage efficiency

![Graph showing efficiency vs. output power for different duty cycles D = 0.25, 0.5, 0.75.](image)

- $V_{out} = 14$ V, $P_{out} = 4.5$ W, $\eta = 91.0\%$
Application: envelope tracking supply for RFPAs

- Target signal: 20 MHz bandwidth LTE envelope
- 4th order filter, 25 MHz cut-off frequency
- 100 MHz switching frequency

\[
\begin{align*}
FPGA & \quad \text{Look-up Table} \\
\text{\(v_{\text{target}}\)} & \quad \text{\(v_{\text{HS}}\)} \\
\text{\(v_{\text{LS}}\)} & \quad \text{\(v_{\text{in}}\)} \\
\text{\(v_{\text{sw}}\)} & \quad \text{\(v_{\text{dd}}\)}
\end{align*}
\]

<table>
<thead>
<tr>
<th>(L_1)</th>
<th>(C_2)</th>
<th>(L_3)</th>
<th>(C_4)</th>
<th>(R_L)</th>
<th>(V_{\text{in}})</th>
<th>(P_{\text{out, pk}})</th>
</tr>
</thead>
<tbody>
<tr>
<td>28 nH</td>
<td>820 pF</td>
<td>307 nH</td>
<td>270 pF</td>
<td>30 Ω</td>
<td>20 V</td>
<td>10 W</td>
</tr>
</tbody>
</table>
Envelope tracking experimental results

- 20 MHz LTE envelope, 100 MHz switching frequency
- Power stage efficiency: 83.7%
- Total efficiency: 80.1% (including on-chip driver loss)
- Normalized RMS error: 5.4%
Path to very high bandwidth (500MHz) tracking

Multi-phase switcher [10]

AC-coupled wide-bandwidth linear amplifier [5, 6]
Two-phase buck converter chip

2.6 x 2.7 mm
Two-phase switching ET amplifier

- 50MHz per-phase switching frequency
- 25MHz tracking bandwidth
- 3.4% RMSE tracking
- 93.2% peak, 85% total efficiency
ET Transmitter System Test Results

18MHz LTE
PAR=7.1dB

VeSP = signal split + DPD

Composite power-added efficiency: 53.6%
ACPR: -28 dB
Conclusions

• Integrated switching converters in GaN-on-SiC process

• 20 V, 10 W peak, >90% peak efficiency, 100 MHz switching

• Accurate tracking of 20 MHz LTE envelope, 85% overall efficiency

• Path to ET RF transmitter SOC integration with up to 500 MHz envelope bandwidth capability in GaN-on-SiC process

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• DARPA MPC program
Selected References


