EFFICIENT MULTILEVEL VOLTAGE REGULATION FOR MICROPROCESSOR CORES STACKED IN VERTICAL VOLTAGE DOMAINS

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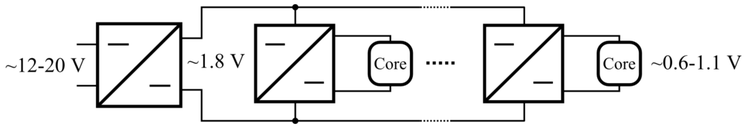
Abstract

Supply voltages for digital circuits have fallen considerably in the past decade, especially for mobile applications supply voltages are projected to reach 0.4 V by 2026. At the same time the level of parallelism in performance and mobile microprocessors is expected to increase substantially posing significant challenges for traditional power supply architectures. In this work we present a power conversion topology to provide independent multi-core regulation in the 0.8-1.4 V range from a 12 V DC bus. The topology uses a multi-stage, hierarchical ladder converter to manage power delivery to performance digital circuits stacked in vertical voltage domains. Measurement results of a discrete prototype verify the control scheme and demonstrate the potential advantages in system efficiency.

Traditional Multi-Core DVFS

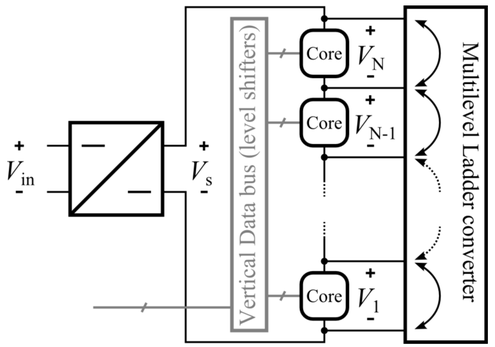
- Supply voltages for digital circuits are projected to fall to 0.4V by 2026 [1]
- Number of parallel cores is increased to scale throughput
- Dynamic voltage and freqency scaling (DVFS) is commonly used to reduce power consumption of cores with low computational load [2]
- DVFS requires independent voltage regulation for each core



- Tradtional solution involve two conversion stages
- First stage requires very low conversion ratio e.g. 19V to 1.8V (laptop)

Stacked Core DVFS

- Series-stacking of cores has been proposed to address some of the shortcomings of traditional solutions [3-5]
- A system dc-dc converter supplies the stack
- Independent core voltage regulation (DVFS) is provided by a parallel power converter
- The partial-power-processing converter provides a parallel path for current to flow around cores with lower supply current



Advantages

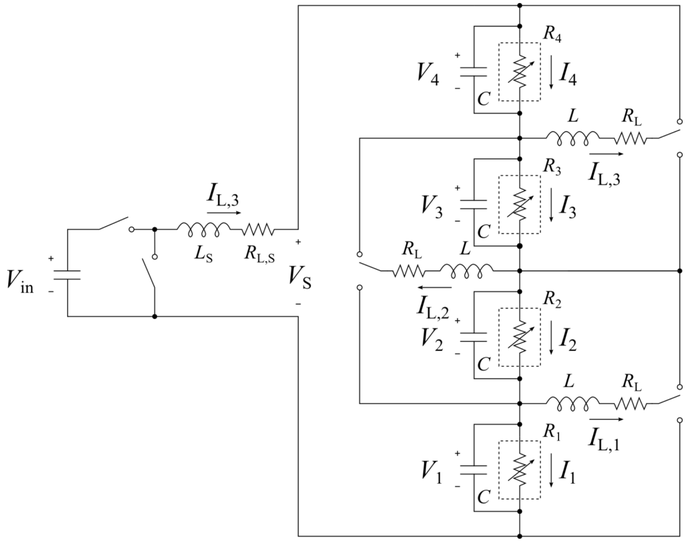
- Moderate conversion ratio in the system dc-dc converter
  -> higher efficiency
- Lower supply current
  -> fewer I/Os
- Most of the power is only processed by one stage
  -> higher efficiency

Challenges

- Communication between cores requires level-shifting
- Parallel converter is required to regulate core-voltages

System Architecture

- The proposed power supply architecture employs a buck converter which supplies and regulated the core stack
- A inductive ladder converter is used to provide independent core voltage regulation



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[6] A. V Peterchev and S. R. Sanders, "Load-Line Regulation With Estimated Load-Current Feedforward: Application to Microprocessor Voltage Regulators," IEEE Trans. Power Electron., vol. 21, no. 6, pp. 1704–1717, Nov. 2006.

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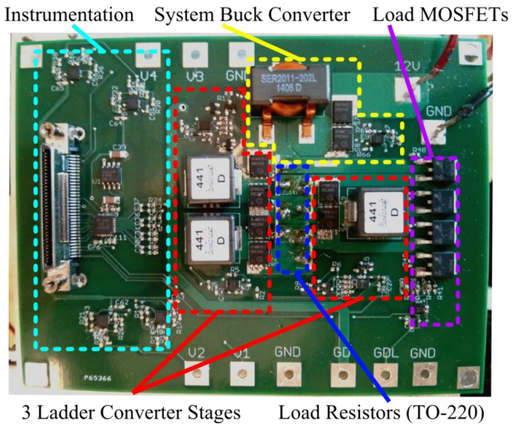
Hardware Implementation

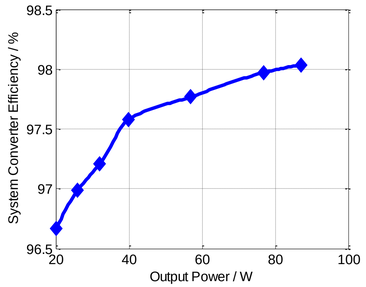
- A full system prototype was implemented on a 4 layer SMT PCB
- Can supply 4 cores with 0.8V-1.4V and up to 90W
- Each core is represented by a 100 mΩ load resistor and a parallel load MOSFET to simulate transient events
- System buck and 3-stage ladder converter use 30V nMOS devices switched at 500 kHz

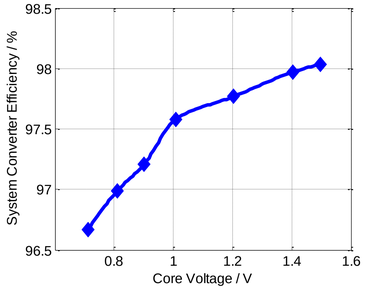


Description	Component	Value
Input voltage	V_{in}	12 V
Load (Core) voltages	V_1-V_4	0.8 V - 1.4 V
Ceramic bypass capacitors (per stage)	6 x 47 µF	~250 µF
Load resistor	PWR220T-35	100 mΩ
Ladder converter inductor	SLC1480	440 nH
System buck converter inductor	SER2011	2 µH

Efficiency

- Up to 98% efficiency were achieved for an ideal scenario with all cores operating with the same supply current and voltage
- >95% efficiency could be maintained even for scenarios with one core consuming more the 50% of the total power





	Scenario 1	Scenario 2	Scenario 3	Scenario 4
Core 4	20 W / 1.4 V	20 W / 1.4 V	20 W / 1.4 V	20 W / 1.4 V
Core 3	20 W / 1.4 V	20 W / 1.4 V	10 W / 1.0 V	6 W / 0.8 V
Core 2	20 W / 1.4 V	6 W / 0.8 V	10 W / 1.0 V	6 W / 0.8 V
Core 1	20 W / 1.4 V	6 W / 0.8 V	10 W / 1.0 V	6 W / 0.8 V
System efficiency	98.0 %	97.0 %	97.1 %	95.6 %

Control

- Independent regulation of all core voltages is challenging due to cross-coupling effects between converter stages

	I_1	I_2	I_3	I_4	V_1-V_4	$I_{L,s}$	$I_{L,1}$	$I_{L,2}$	$I_{L,3}$
Operating Point 1	4 A	4 A	4 A	4 A	1 V	4 A	0 A	0 A	0 A
Operating Point 2	8 A	4 A	4 A	4 A	1 V	5 A	6 A	4 A	2 A

- A feedback with parallel feedforward scheme based on estimated load currents [6] was developed to achieve high dc accuracy and fast response