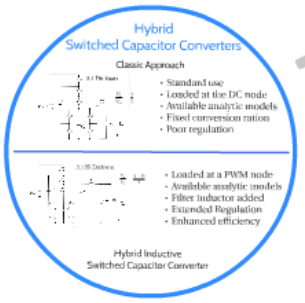
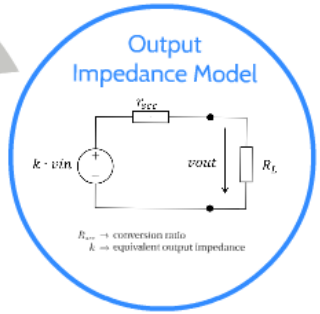
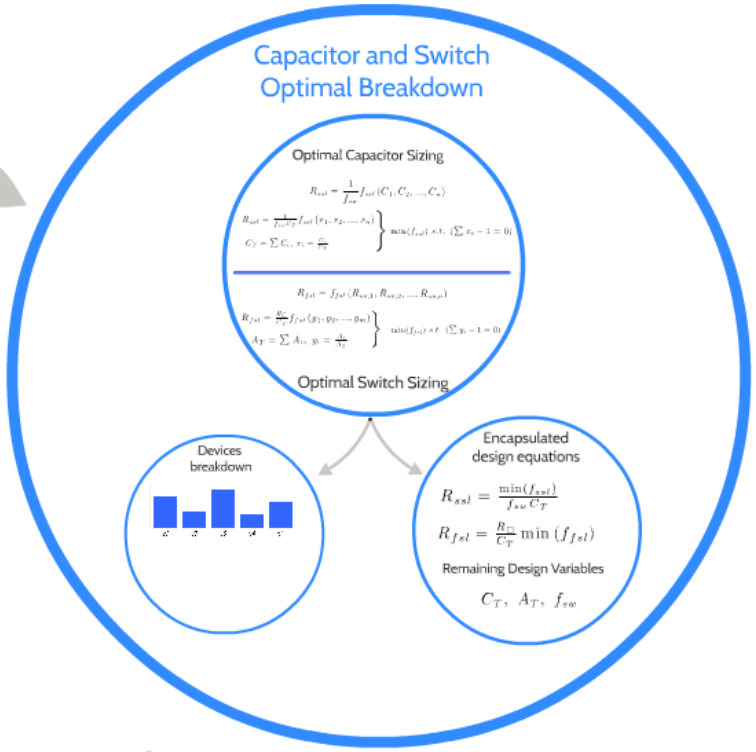
# Resource/performance optimization for Hybrid Inductive-Capacitive Converters

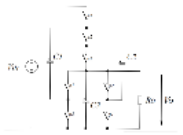


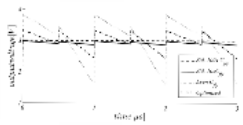

## Results

### 3:1 Dickson



Capacitor Breakdown Results for a 3:1 Dickson SCC loaded at the DC node operating with
$V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 50\%$, $R_{sw} = 1m\Omega$

| Design | $X_1$ [%] | $X_2$ [%] | $X_3$ [%] | $f_{ssl}$ [$m\Omega FHz$] | $C_T$ [$nF$] | $\Delta V_{o,pp}$ [$mV$] | $MIM^1$ [$mm^2$] | $IPDiA^2$ [$mm^2$] |
|---|---|---|---|---|---|---|---|---|
| Std. $100C_{fly}$ | 1 | 1 | 98 | 32460 | 39660 | 16 | 396.6 | 1.6 |
| Std. $10C_{fly}$ | 8 | 8 | 85 | 2430 | 3646 | 116 | 56.6 | 140E-3 |
| Even $C_{fly}$ | 33 | 33 | 33 | 375 | 563 | 895 | 3.6 | 22E-3 |
| Optimized | 43 | 43 | 14 | 238 | 357 | 2237 | 3.6 | 14E-3 |

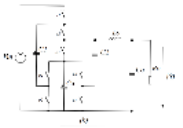


Switch Area Breakdown Results for the 3:1 Dickson SCC loaded at the dc node [1] and the 3:1 Dickson H-SCC[2] loaded at the 2ND *pwm* node

| Design | $X_1$ [%] | $X_2$ [%] | $X_3$ [%] | $X_4$ [%] | $X_5$ [%] | $X_6$ [%] | $X_7$ [%] | $f_{fsl}$ [$\Omega m^2$] |
|---|---|---|---|---|---|---|---|---|
| SCC Opt. | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 10.8 |
| H-SCC Even | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 31.3 |
| H-SCC Opt. | 23.1 | 13.4 | 16.5 | 3.8 | 6.6 | 13.4 | 23.1 | 25.4 |

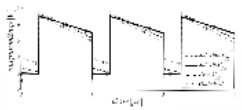
[1] Solution with $Duty = 50\%$
[2] Solution with $Duty = 25\%$

### 3:1 Hybrid-Dickson



Capacitor Breakdown Results for a 3:1 H-Dickson SCC loaded at the 2ND *pwm* node operating with
$V_{in} = 10V$, $F_{sw} = 1MHz$, $\eta = 90\%$, $I_o = 5mA$, $Duty = 25\%$, $R_{sw} = 1m\Omega$

| Design | $X_1$ [%] | $X_2$ [%] | $X_3$ [%] | $f_{ssl}$ [$m\Omega FHz$] | $C_T$ [$nF$] | $\Delta V_{o,pp}$ [$V$] | $MIM^1$ [$mm^2$] | $IPDiA^2$ [$mm^2$] |
|---|---|---|---|---|---|---|---|---|
| Std. $100C_{fly}$ | 1 | 1 | 98 | 23124 | 19820 | 3.73 | 198.2 | 792E-3 |
| Std. $10C_{fly}$ | 8 | 8 | 83 | 2651 | 2272 | 3.78 | 27.7 | 110E-3 |
| Even $C_{fly}$ | 33 | 33 | 33 | 594 | 508 | 4.07 | 5.1 | 20E-3 |
| Optimized | 58 | 21 | 1 | 409 | 350 | 4.45 | 3.5 | 14E-3 |



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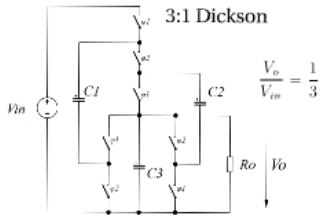
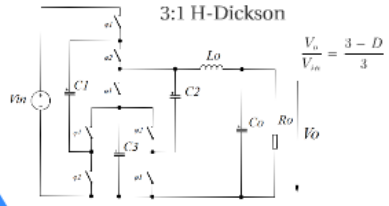
# Hybrid Switched Capacitor Converters

## Classic Approach



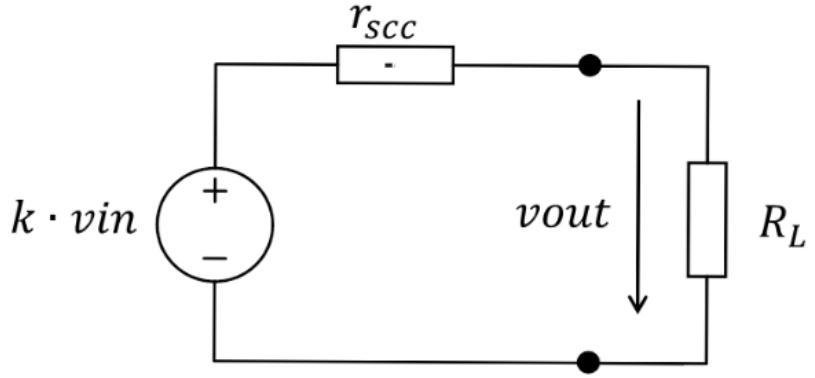

- Standard use
- Loaded at the DC node
- Available analytic models
- Fixed conversion ration
- Poor regulation




- Loaded at a PWM node
- Available analytic models
- Filter inductor added
- Extended Regulation
- Enhanced efficiency

## Hybrid Inductive Switched Capacitor Converter

# Output Impedance Model




$R_{scc} \rightarrow$ conversion ratio

$k \rightarrow$ equivalent output impedance

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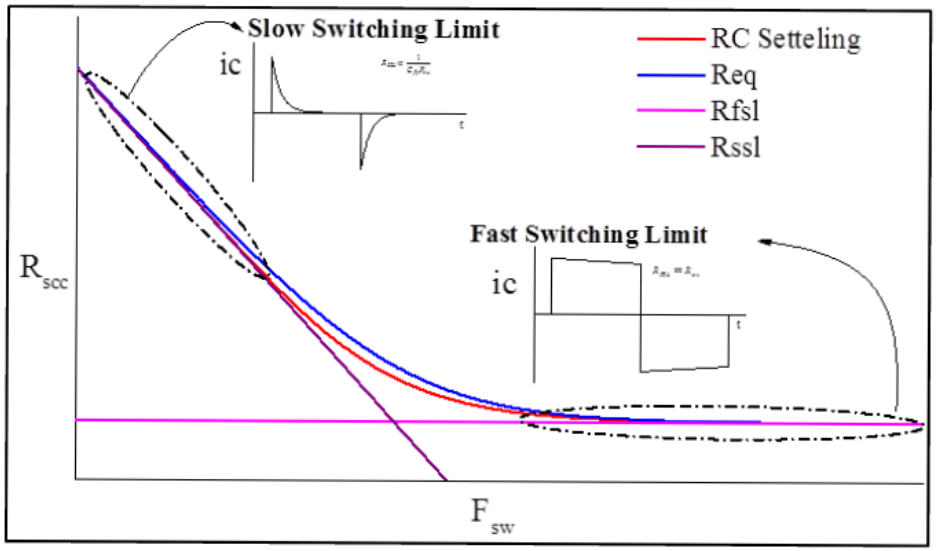
# Output resistance characteristics




Two regions of operation

Slow Switching Limit (SSL)
Charge Transfer Dominate Losses

$$R_{ssl} = \frac{1}{f_{sw}} f_{ssl}\left(C_1, C_2, \ldots, C_n\right)$$

Fast Switching Limit (FSL)
Switch ON-channel Resistance Dominate Losses

$$R_{fsl} = f_{fsl}\left(R_{on,1}, R_{on,2}, \ldots, R_{on,n}\right)$$

# Capacitor and Switch Optimal Breakdown

## Optimal Capacitor Sizing

$$R_{ssl} = \frac{1}{f_{sw}} f_{ssl}\left(C_1, C_2, ..., C_n\right)$$

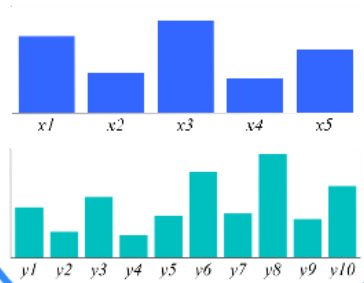
$$\left.\begin{aligned} R_{ssl} &= \tfrac{1}{f_{sw} C_T} f_{ssl}\left(x_1, x_2, ..., x_n\right) \\ C_T &= \textstyle\sum C_i,\ x_i = \tfrac{C_i}{C_T} \end{aligned}\right\} \min(f_{ssl})\ s.t.\ \left(\textstyle\sum x_i - 1 = 0\right)$$

## Optimal Switch Sizing

$$R_{fsl} = f_{fsl}\left(R_{on,1}, R_{on,2}, ..., R_{on,n}\right)$$

$$\left.\begin{aligned} R_{fsl} &= \tfrac{R_\square}{C_T} f_{fsl}\left(y_1, y_2, ..., y_m\right) \\ A_T &= \textstyle\sum A_i,\ y_i = \tfrac{A_i}{A_T} \end{aligned}\right\} \min(f_{fsl})\ s.t.\ \left(\textstyle\sum y_i - 1 = 0\right)$$

## Devices breakdown




## Encapsulated design equations

$$R_{ssl} = \frac{\min(f_{ssl})}{f_{sw} C_T}$$

$$R_{fsl} = \frac{R_\square}{C_T} \min\left(f_{fsl}\right)$$

Remaining Design Variables

$$C_T,\ A_T,\ f_{sw}$$

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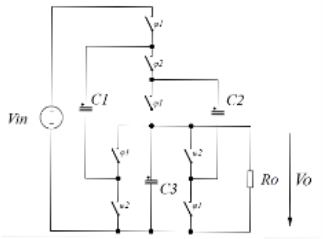
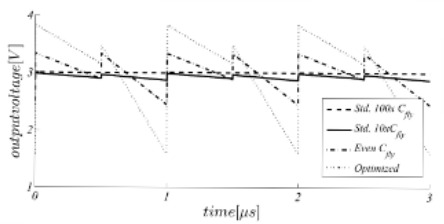
# Results

## 3:1 Dickson




CAPACITOR BREAKDOWN RESULTS FOR A 3:1 DICKSON SCC LOADED AT THE *DC* NODE OPERATING WITH
$V_{in} = 10V,\ F_{sw} = 1MHz,\ \eta = 90\%,\ I_o = 5mA,\ Duty = 50\%,\ R_{sw} = 1m\Omega$

| Design | $X_1$ [%] | $X_2$ [%] | $X_3$ [%] | $f_{ssl}$ $[m\Omega FHz]$ | $C_T$ $[nF]$ | $\Delta V_{o,pp}$ $[mV]$ | $MIM^1$ $[mm^2]$ | $IPDiA^2$ $[mm^2]$ |
|---|---|---|---|---|---|---|---|---|
| Std. $100C_{fly}$ | 1 | 1 | 98 | 22400 | 33660 | 10 | 336.6 | 1.4 |
| Std. $10C_{fly}$ | 8 | 8 | 83 | 2430 | 3640 | 116 | 36.6 | 140E-3 |
| Even $C_{fly}$ | 33 | 33 | 33 | 375 | 563 | 892 | 5.6 | 22E-3 |
| Optimized | 43 | 43 | 14 | 238 | 357 | 2237 | 3.6 | 14E-3 |

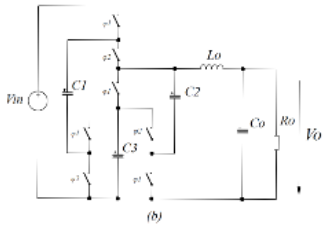



SWITCH AREA BREAKDOWN RESULTS FOR THE 3:1 DICKSON SCC LOADED AT THE *dc* NODE [1] AND THE 3:1 DICKSON H-SCC[2] LOADED AT THE 2ND *pwm* NODE

| Design | $X_1$ [%] | $X_2$ [%] | $X_3$ [%] | $X_4$ [%] | $X_5$ [%] | $X_6$ [%] | $X_7$ [%] | $f_{fsl}$ $[\Omega m^2]$ |
|---|---|---|---|---|---|---|---|---|
| SCC Opt. | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 10.8 |
| H-SCC Even | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 14.2 | 31.3 |
| H-SCC Opt. | 23.1 | 13.4 | 16.5 | 3.8 | 6.6 | 13.4 | 23.1 | 25.4 |

[1] Solution with $Duty = 50\%$
[2] Solution with $Duty = 25\%$

## 3:1 Hybrid-Dickson




CAPACITOR BREAKDOWN RESULTS FOR A 3:1 H-DICKSON SCC LOADED AT THE 2ND *pwm* NODE OPERATING WITH
$V_{in} = 10V,\ F_{sw} = 1MHz,\ \eta = 90\%,\ I_o = 5mA,\ Duty = 25\%,\ R_{sw} = 1m\Omega$

| Design | $X_1$ [%] | $X_2$ [%] | $X_3$ [%] | $f_{ssl}$ $[m\Omega FHz]$ | $C_T$ $[nF]$ | $\Delta V_{o,pp}$ $[V]$ | $MIM^1$ $[mm^2]$ | $IPDiA^2$ $[mm^2]$ |
|---|---|---|---|---|---|---|---|---|
| Std. $100C_{fly}$ | 1 | 1 | 98 | 23124 | 19820 | 3.73 | 198.2 | 792E-3 |
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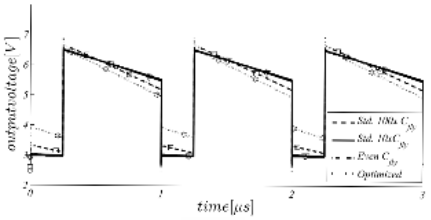


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