1 mΩ/[] Bond-Able Post-Passivation Interconnect for Power Management Technologies.

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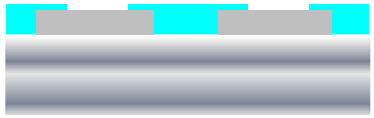
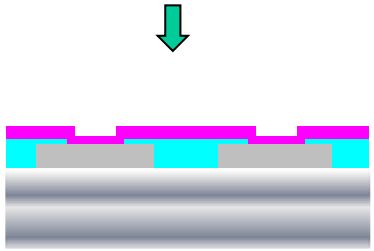
Outline

- Technology development
  - Planarized passivation
  - Test chip description
  - Passivation and thick Cu effects on device parameters
- Assembly issues
- Reliability qualification tests
- Summary and conclusions

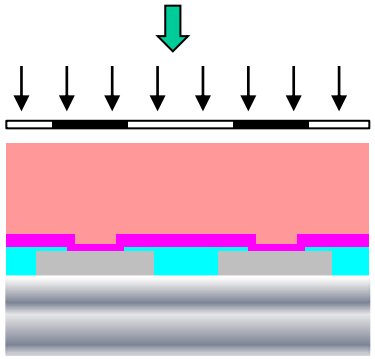
Simplified process flow



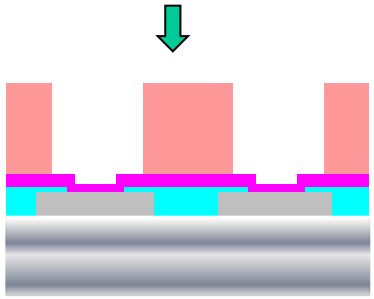
- *Incoming Wafer*



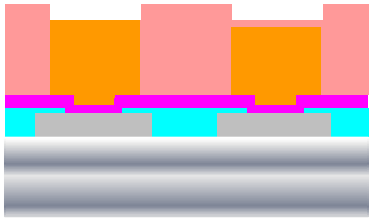
- *UBM sputter*



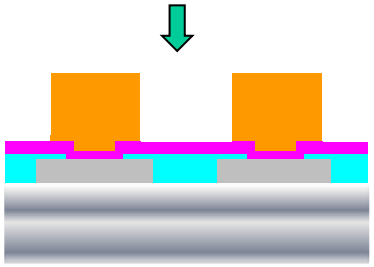
- *PR coating & PR exposure*



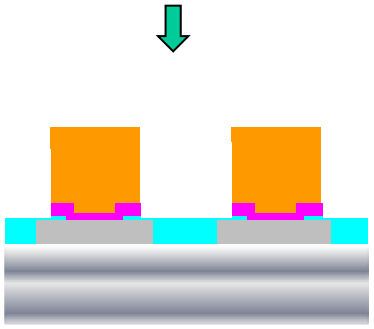
- *PR develop*



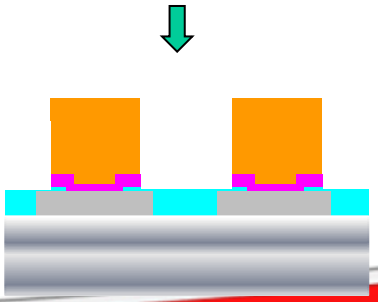
- *Cu/Ni/Au plating*



- *PR strip*



- *UBM Etch*



- *FQM/FQI/OQC*

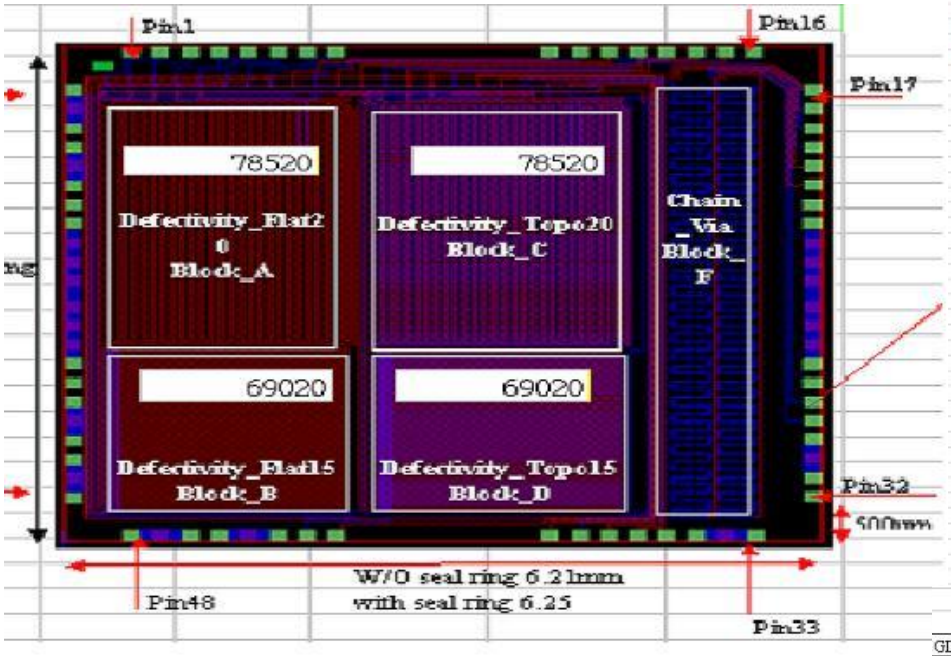
Wafer Fab process flow

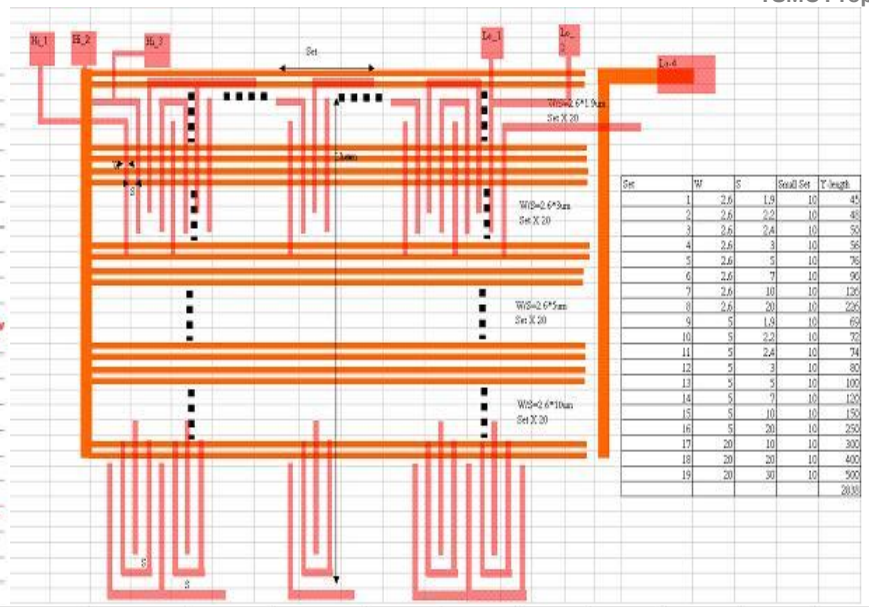
- Planarized passivation (oxide/nitride)
  - Developed for two top Al film thickness values
    - 3.0μm thick Al
    - 0.8μm thick Al
- Pad opening photo/etch process
  - 5X5 μm minimum pad opening for Cu to Al interconnect
    - 3x3mm sub-minimum size pad opening (process marginality check)
- UBM, photo, plating and UBM removal process at vendor's
  - 20μm Cu/ 2μm Ni/ ~0.4μm Au

Test Chip description

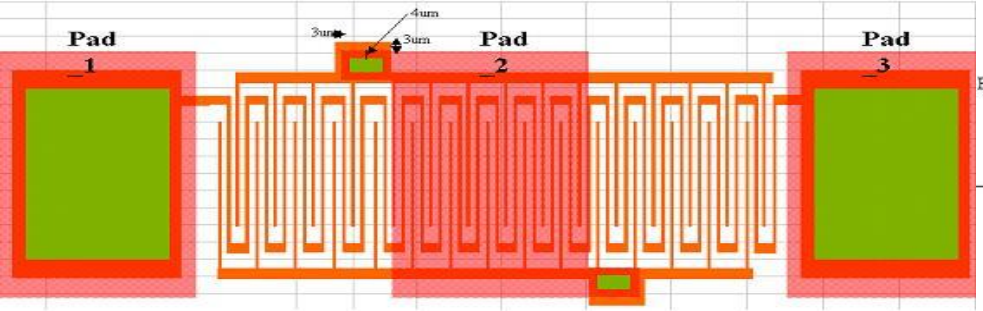
- 6 test chips, 6.25X6.25mm each
- Main test structures
  - 20μm line/ 20μ space serp-comb (~15cm periphery)
  - 15μm line/ 15μ space serp-comb (~15cm periphery)
  - Structures placed over flat Si and over Al topography
  - Serp-comb under the bonding pad
  - Via chains and Kelvin via structures
  - Variable length/width strips of Cu to check for Cu de-lamination

Test Chip description

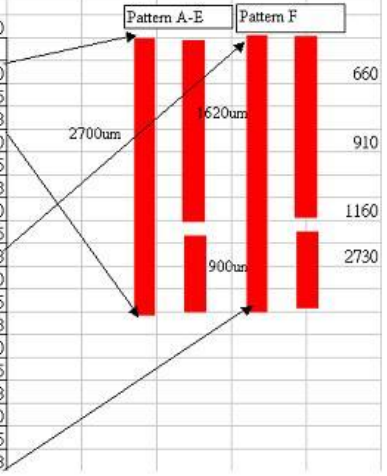




Set	W	S	Small Set	Y length
1	2.6	1.9	10	45
2	2.6	2.2	10	48
3	2.6	2.4	10	50
4	2.6	3	10	56
5	2.6	5	10	76
6	2.6	7	10	90
7	2.6	10	10	120
8	2.6	20	10	220
9	5	1.9	10	69
10	5	2.2	10	72
11	5	2.4	10	74
12	5	3	10	80
13	5	5	10	100
14	5	7	10	120
15	5	10	10	150
16	5	20	10	250
17	20	10	10	300
18	20	20	10	400
19	20	30	10	500



GDS name		Length (L)	Width (W)	Pattern	SET
Bonding_A~E	a	5400	250	A	30
	b	2700	250	A	15
	c	1440	250	A	8
	d	5400	375	A	30
	e	2700	375	A	15
	f	1440	375	A	8
	g	5400	500	A	30
	h	2700	500	A	15
	i	1440	500	A	8
Bonding_F	a	5400	250	A	30
	b	2700	250	A	15
	c	1440	250	A	8
	d	5400	375	A	30
	e	2700	375	A	15
	f	1440	375	A	8
	g	5400	500	A	30
	h	2700	500	A	15
	i	1440	500	A	8



PPI plating vendors

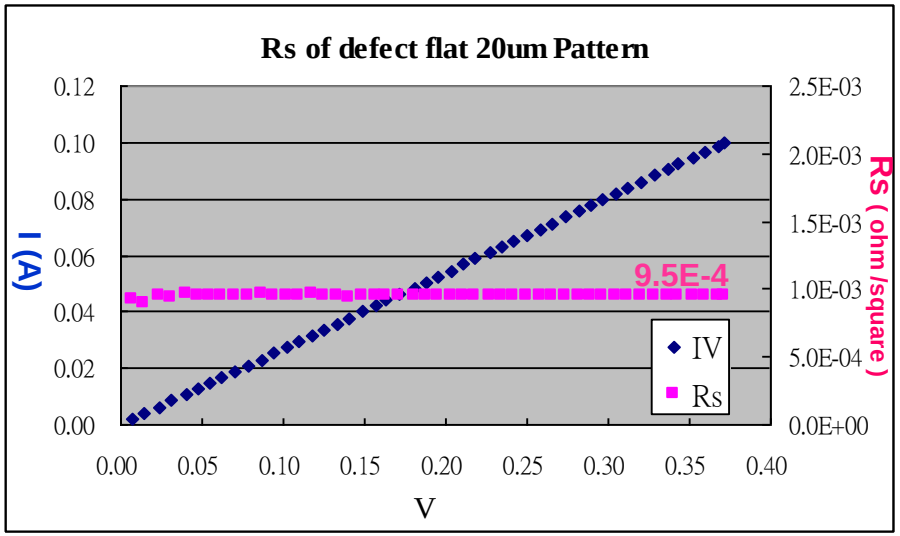
- Vendor A: completed pre-qualification
- Vendor B: could not meet specifications
- Vendor C: currently in pre-qualification
- “Vendor A” results are presented in subsequent slides

"Vendor A" results, as deposited Cu

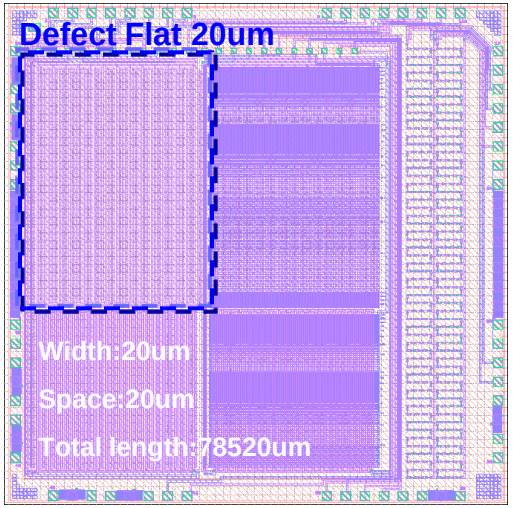
- 30kA Al and 8kA Al WAT show the following:
- thick Cu to underlying Al capacitance is very well controlled, indicating good thickness uniformity of the planarized passivation (C_Area=350000um2)
- Thick Cu to the underlying Al leakage measured at 80V is well under 1nA (defectivity structure)
- Thick Cu sheet resistance is below ~1.5 mOhm/[]
- Cu line to line leakage measured between the serpentine and the comb with the effective serp perimeter of ~15cm is < 10nA at 80V (or 0.1uA per cm2 of the serp sidewall area). Leakage yield loss is <1%
- 3X3 Via resistance (Kelvin method) is ~15mOhm

Rs of 20um Cu PPI Pattern

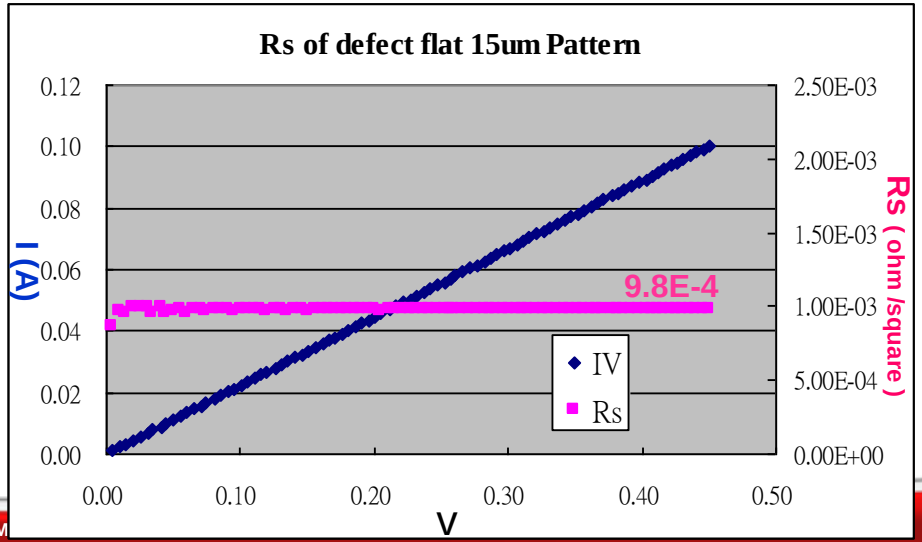
- Rs of PPI defect flat 20um Pattern ~9.5E-4 ohm/square
- Sample size: 1100



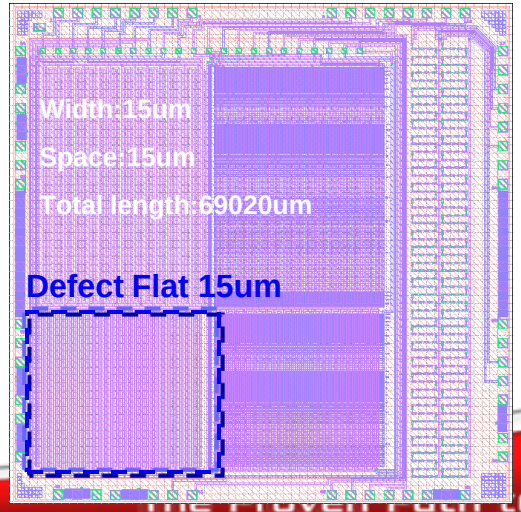
TMAQ32 CHIP1



- Rs of PPI defect flat 15um Pattern ~9.8E-4 ohm/square
- Sample size: 1100



TMAQ32 CHIP1

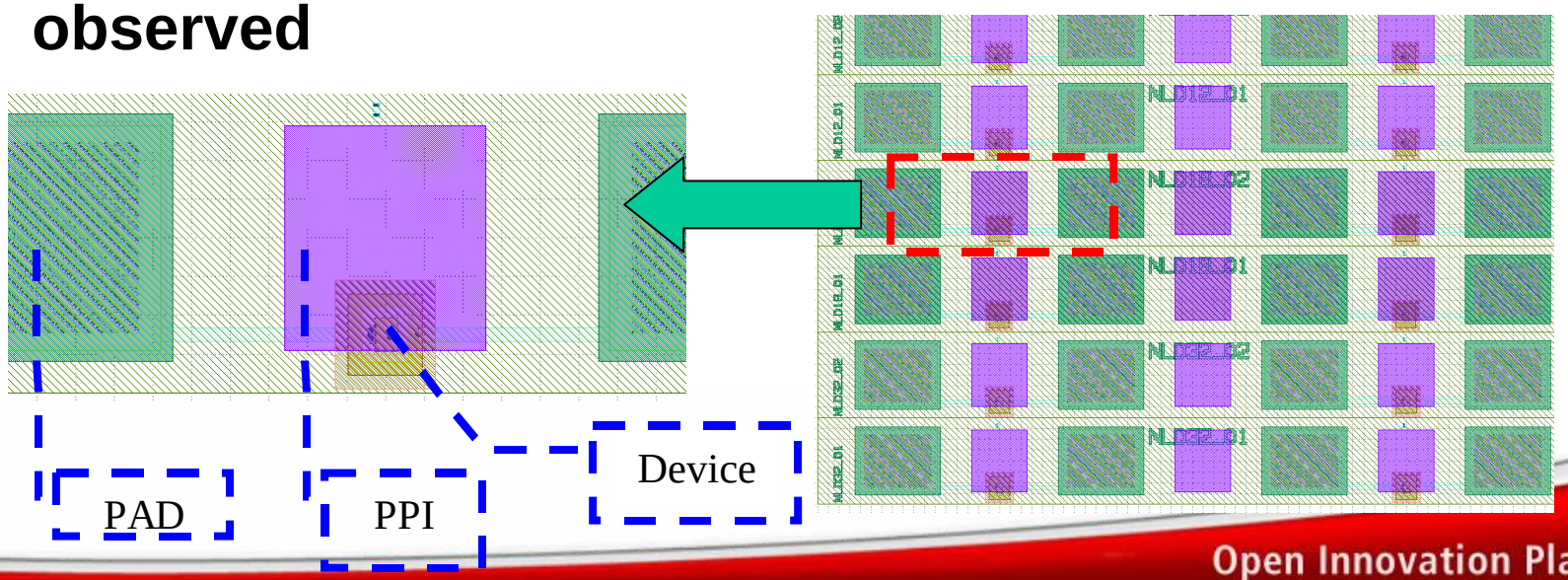


"Vendor A" results, wafer level stress

- Cu PPI exposed to ambient, clean required after the stress test prior to electrical testing.
- Temperature cycling, -65C to 150C, 1000 cycles
  - Passed with no changes in parametrics and no cracks
- High Temperature Storage, 150C in air
  - 5X5 via chains develop a higher R "tail". This is not observed on Kelvin vias or on packaged via chains
- Un-biased HAST, 130C, 85% relative humidity
  - 5X5 via chains develop a higher R "tail". This is not observed on Kelvin vias or on packaged via chains

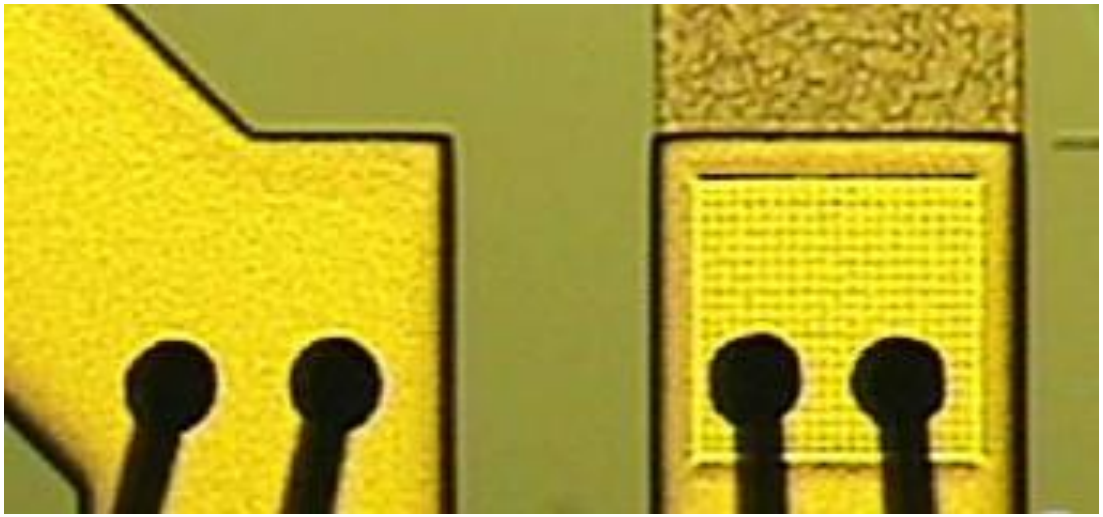
Planarization and PPI effect on devices

- Planarized passivation with and w/o the PPI was applied to 0.25μm (2.5V/5V) and 0.18μm (1.8V/5V) BCD processes.
- Used 30kA and 8kA top Al for both processes
- Each device is partially covered by the PPI
- Less than 3% differences in parameter values observed



Assembly issues

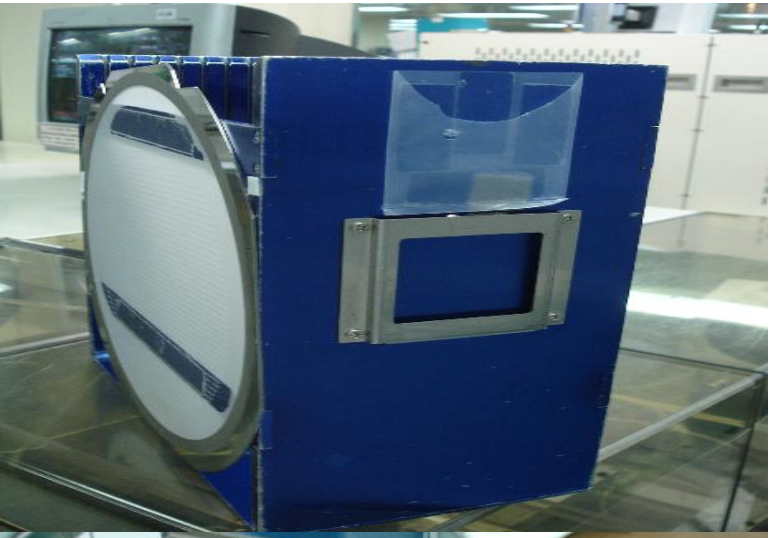
- Two assembly houses evaluated
  - QFN-88 package with 0.8 mil Cu wire
  - Both assembly houses demonstrated excellent bond-ability to Cu/Ni/Au both on flat features and over a “sea of vias” with specific design rules

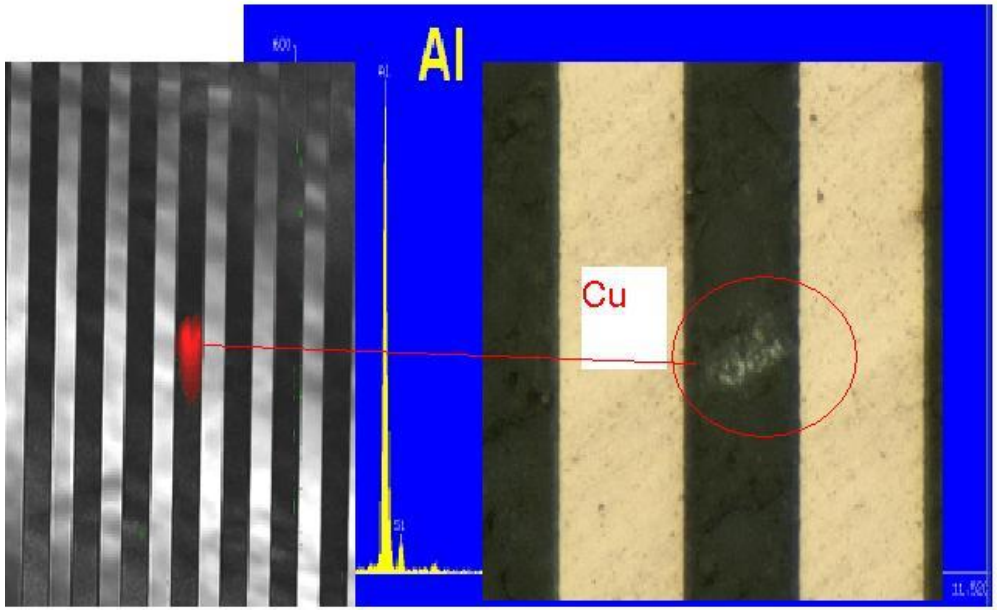


“Random” assembly defects

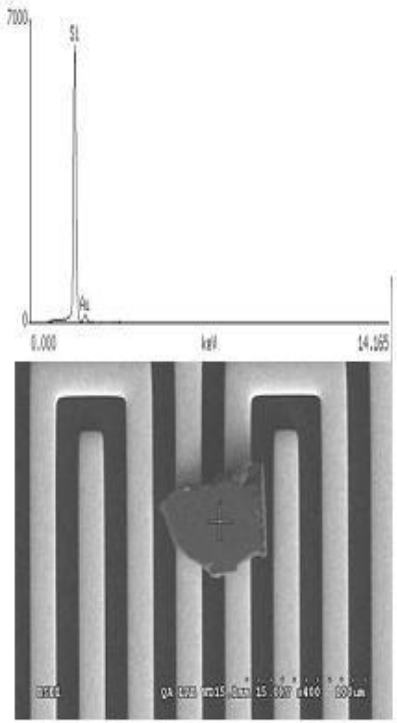
- Defective units (QFN-88 not meeting the line-line leakage specification) FA
  - Assembly house A
    - Al particles
    - Si particles (single occurrence)
    - Ag particle
  - Assembly houses A and B
    - Stainless steel particle
    - Cu particles
    - C particle

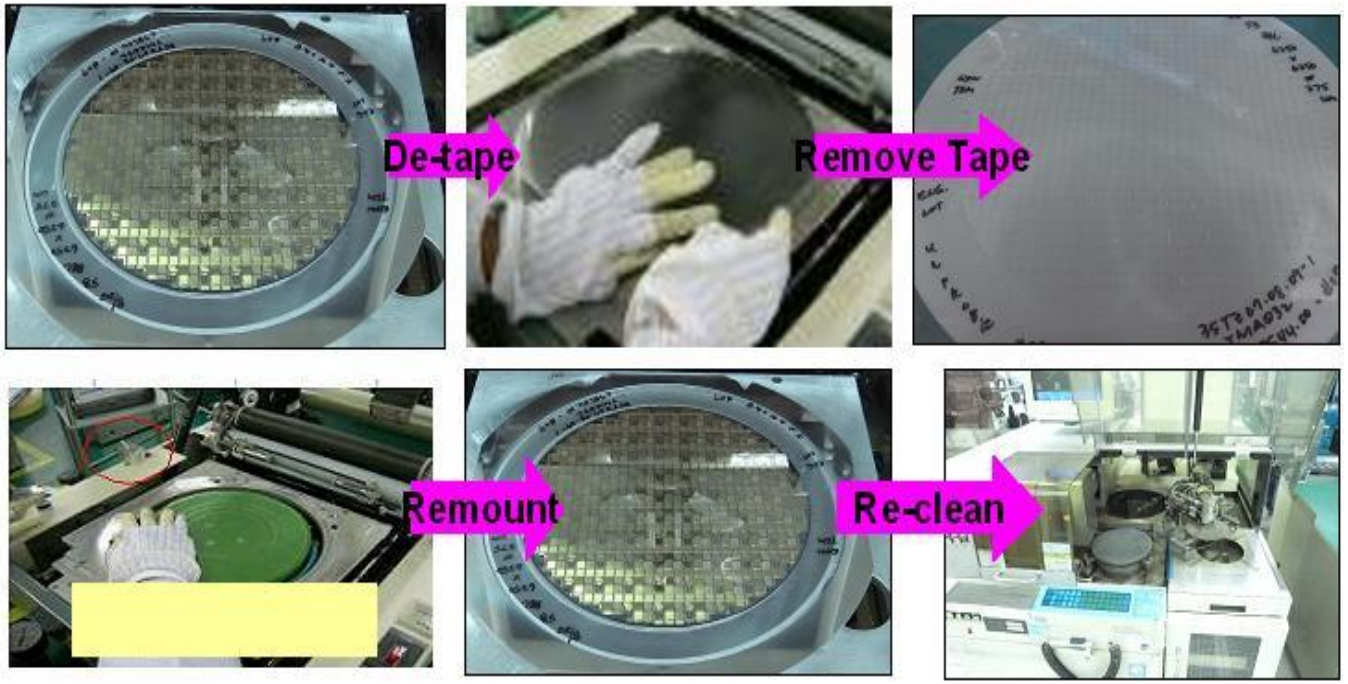
Al particle (Assembly A): poorly maintained strip magazines and wafer carriers





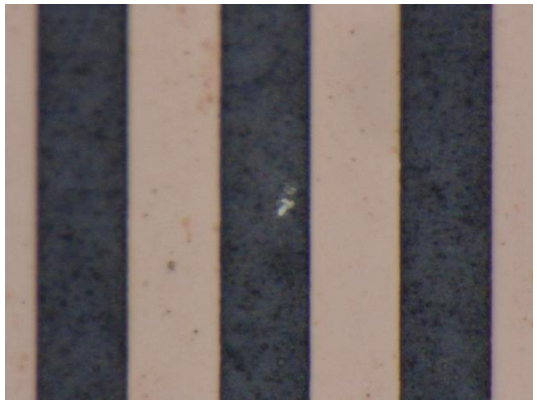
Si particle (Assembly A): one time occurrence



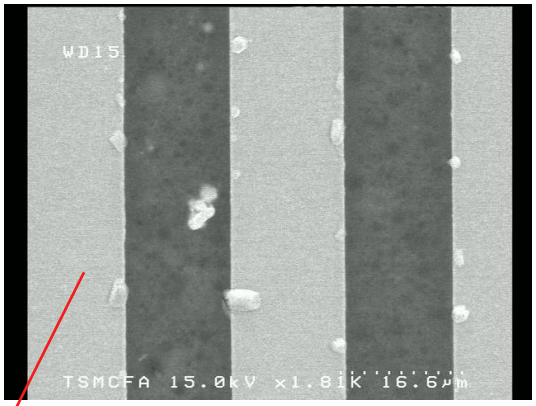


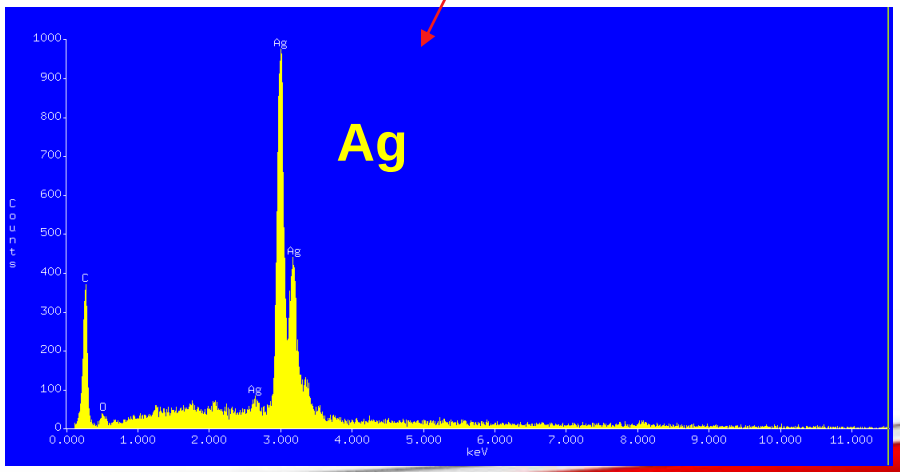
Ag particle (Assembly A, one time occurrence)

OM



SEM





"Systematic" assembly defects

- 20μm and 15μm spaced Cu lines leakage improvement
- Stainless steel particles (~10% yield killer)
  - Present in the molding compound
  - Specified by vendor to be <130μm in size
  - Limited potential for improvement
- Cu particles (~20% yield killer)
  - Originate from the Cu deposit in scribe channels
  - Can be eliminated by making sure Cu deposits are not present in scribe channels
- C cohesion particles (~70% yield killer)
  - Improvement path identified by the molding compound vendor

Carbon cohesion particles improvement

Defect size	“Current “ Carbon	“Dispersed” Carbon	“Highly dispersed C”
45um and >	22/ sample	0	0
25um-44um	40/sample	1	0
20um-24um	4/sample	3	2

Distribution of defect sizes for the current molding compound (“Current Carbon”), Dispersed Carbon and highly dispersed Carbon samples. Sumitomo formed two samples with each type of Carbon additive (10cm diameter disc, 2mm thick, weight ~31g), and inspected these for the black carbon particle number and size using the fluorescent microscope. Note that the “dispersed” and the “highly dispersed” Carbon grades result in significant reduction in the both the size and the observed density of C particles.

Package Level Reliability Tests

Qualification Item	Stress Condition	Read Out
Unbiased HAST	130C / 85% RH / 33.3psi without bias	168 hrs
T/ C Temperature Cycle	-65C ~ +150C (Condition C, air to air)	500 / 1000hrs
HTS High Temperature Storage Test	150C	500 / 1000hrs

Summary and conclusions

- ~1 mOhm/[] bond-able post passivation interconnect is developed
  - Processing does not affect device parameters
- Several assembly defects are identified
  - Assembly process/material items requiring improvement identified
  - Effect on yield estimated
- PPI successfully pre-qualified
  - Wafer level
  - Package level