Fully Integrated SC DC-DC: Bulk CMOS Oriented Design

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Outline

- Towards monolithic integration
- CMOS as technology vehicle
- Techniques for CMOS DC-DC
- Conclusions
TOWARDS MONOLITHIC INTEGRATION
Driving aspects

- Limited I/O pads
- Multiple Voltage Rails
- Power Saving Techniques
- Multicore Granularity
- High Supply Current
- Supply Impedance

Monolithic integration
CMOS AS TECHNOLOGY VEHICLE
Why CMOS?

- When there are other superior technologies such as GaN and GaAs
  - Superior parameters
  - But more expensive

- It depends on the specific requirements
- There is no single technology that can replace all others
CMOS offers compact coexistence of power supply and load

- Compatibility
- Size
- Cost
- It’s already available

CMOS also offers parasitics ...

Required for true granularisation

In this case it is not a matter of being the best in class, but to be (more than) sufficient by coping for parasitics and having the benefit of low cost.
TECHNIQUES FOR CMOS DC-DC
Bottom Plate Parasitic

- Concerns parasitic coupling of flying capacitor
  - 2 possible locations in a 2/1 step-down
Parasitic Capacitor

- Typical bottom plate parasitic in CMOS
Flying Well

- Reduces $C_{par}$ from >5% to 1.3% in this case
Intrinsic Charge Recycling

- Concerns parasitic coupling of flying capacitor
  - 2 possible locations in a 2/1 step-down
Intrinsic Charge Recycling

An output perspective

Without Recycling

\[ \Phi_a \]
\[ V_i \quad C_{fly} \quad V_o \]
\[ C_{par} \]

\[ \Phi_b \]
\[ C_{par} \quad + \quad - \quad V_o \quad C_{fly} \quad C_o \]

With Recycling

\[ \Phi_a \]
\[ + \quad - \quad C_{fly} \quad V_o \]
\[ C_{par} \]

\[ \Phi_b \]
\[ C_{par} \quad - \quad + \quad V_o \quad C_{fly} \quad C_o \]
**Intrinsic Charge Recycling**

\[
E_{O,C_{par},REG} = C_{par} (\gamma V_{o,id})^2
\]

**Output perspective**

With Recycling

\[\Phi_a\]

\[\Phi_b\]

Without Recycling

\[\Phi_a\]

\[\Phi_b\]
Intermezzo: $V_{o,id}, V_o$ and $\gamma$

Thevenin Model

$$V_{th} = \frac{1}{2} V_i = V_{o,id}$$

$$R_{th} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \quad [5]$$

Voltage drop over $R_{th}$ due to voltage divider formed by $R_{th}$ and a $R_L$. This ratio equals $\gamma$. 

$micas$

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PowerSoC 2012
Intrinsic Charge Recycling

\[ E_{O,C_{par},\text{REG}} = C_{par}(\gamma V_{o,\text{id}})^2 \]

\[ E_{O,C_{par},\text{ICR}} = C_{par} V_{o,\text{id}}^2(\gamma^2 - 2\gamma) \]
Intrinsic Charge Recycling

*An input perspective*

**Without Recycling**

\[ \frac{1}{2}V_i = V_{o, id} \]

\[ V_o = \gamma V_{o, id} \]

**With Recycling**

\[ \Phi_a \]

\[ \Phi_b \]
Intrinsic Charge Recycling

An input perspective

Without Recycling

\[ E_{I,C_{\text{par}},\text{REG}} = \frac{C_{\text{par}}(\gamma V_{o,\text{id}})^2}{\gamma} \]

With Recycling

\[ \Phi_a \]

\[ \Phi_b \]
Intrinsic Charge Recycling

An input perspective

Without Recycling

\[ E_{I,C_{par},REG} = \frac{C_{par}(\gamma V_{o,\text{id}})^2}{\gamma} \]

With Recycling

\[ E_{I,C_{par},ICR} = C_{par}V_{o,\text{id}}^2(4 - 2\gamma) \]
The combined perspective

Trade-off: $\Delta E_{out} - \Delta E_{in} \geq 0$

\[
\left( -E_{O,Cpar,ICR} + E_{O,Cpar,REG} \right) - \left( E_{I,Cpar,ICR} - E_{I,Cpar,REG} \right)
\]

= ...

= $C_{par} V_{o,id}^2 (5\gamma - 4)$

The trade-off is only function of $\gamma$!

→ Any capacitor type

→ Any $V_i$
The combined perspective
Intrinsic Charge Recycling

The combined perspective
Intrinsic Charge Recycling

- **Summary**

  ✓ $f_{sw}$ constant $\rightarrow P_o \uparrow$

  ✓ $P_o$ constant $\rightarrow f_{sw} \downarrow$
Other forms of charge recycling

- Voltage domain recycling by serial voltage domains
System Architecture

- Converter core
  - Non overlap generation
  - Level shifting
  - Buffering
  - 2 voltage domains
    - ground..V_o
    - V_o..V_i
  - 1 C_{fly}: P-moscap
  - 4 switches
System Architecture

- On-chip 21 tap VCO
- 21 converter cores spread out of phase
- $C_{\text{fly, total}}$: 12 nF
- $W_{\text{switch, total}}$: 11.5 cm
- Integrated linear regulator for start-up
Chip microphotograph + layout

1510um

Core

Switches

C1a

C1b

C1c

C1d
Measurements

- Closed loop
- $V_{in}$: 2.4V
- $V_{out}$: 1V
- $P_o$ range: 250-1050mW
- Peak efficiency: 65% at 1W
- Battery lifetime extension ($EEF$ [3]): +36%

![Graph showing efficiency vs. output power](Image)
Measurements

- Open loop
- Maximum $P_{\text{out}}$: 1.65W
- Maximum $\eta$: 69%
Measurements

- Open loop load regulation
  - -0.175 Ω
## Comparison with state of the art

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>capacitive</td>
<td>capacitive</td>
<td>inductive</td>
<td>capacitive</td>
<td>capacitive</td>
</tr>
<tr>
<td>Control</td>
<td>closed external</td>
<td>external $f_{sw}$</td>
<td>SCOOT</td>
<td>discrete step loop</td>
<td>closed external</td>
</tr>
<tr>
<td>Power density</td>
<td>0.86W/m²</td>
<td>7.4W/mm²</td>
<td>0.21W/mm²</td>
<td>1.12W/mm²</td>
<td>0.77W/mm²</td>
</tr>
<tr>
<td>$P_{out,max}$</td>
<td>0.33W</td>
<td>8.88mW</td>
<td>0.8W</td>
<td>10.6mW</td>
<td>1.65W</td>
</tr>
<tr>
<td>$\eta_{max}$</td>
<td>85%</td>
<td>90%</td>
<td>58%</td>
<td>64%</td>
<td>69%</td>
</tr>
<tr>
<td>Tech option</td>
<td>SOI</td>
<td>SOI, deep trench caps</td>
<td>Bulk CMOS</td>
<td>Bulk CMOS, metal gate</td>
<td>Bulk CMOS</td>
</tr>
<tr>
<td># interleaving</td>
<td>32</td>
<td>1</td>
<td>4</td>
<td>32</td>
<td>21</td>
</tr>
</tbody>
</table>
Comparison with state of the art

![Graph showing comparison between output power and power density for different technologies, including This Work, [1], [2], [3], and [4].]
CONCLUSIONS
Conclusions

- Cheap and power dense integrated DC-DC converters facilitate on-chip power management
- The passives are the bottleneck!
  - $\approx 90\%$ of die area
- Bulk CMOS is potential vehicle for PowerSoC
  - Flying Well
  - Intrinsic Charge Recycling
  - Multiphase Interleaving
  - Voltage Domain Stacking
- Application domain
  - High performance: solving I/O problem
  - Low performance: implementing energy saving techniques
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QUESTIONS?

- Thank you!