Many Voltage Domains using Distributed Switched Capacitor Voltage Regulators

Rinkle Jain
Circuit Research Labs
Intel Corporation
OR

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Outline

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Introduction

Recent design trends in phone/tablets

- User experience is key – in addition to battery life
- Requires bursts of high performance
- and, freeing up this power budget by minimizing idle power

What does this translate to?

- Performance autonomy of modules (e.g. cores), at low power
  - Highly granular voltage domains, voltage scaling
- Minimize idle power consumption through design
  - $V_{min}$ reduction techniques
  - Near $v_t$ (NTV) operation
  - Optimal $C_{dyn}$ through design at optimum voltage

Need: Autonomous, highly granular voltage domains
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Need: Autonomous, highly granular voltage domains
Exploit DVFS fully: energy savings with 80% efficient VR

Shared rail in black
\[ \alpha \triangleq \% \text{ time the block is in high frequency mode (HFM), } V_{cc} = V_{max} \]
\[ \beta \triangleq \% \text{ of idle time the shared rail allows } V_{cc} = V_{min} \text{ else } V_{max} \]

Dedicated rail in color
Red: \( V_{in} \approx V_{max} \), VR bypassed at HFM when \( V_{cc} = V_{max} \)
Blue: \( V_{in} \gg V_{max} \), VR incurs losses at HFM when \( V_{cc} = V_{max} \)

Dedicated voltage regulators (VR) are the key enablers
First glimpse - what does it take per domain?

Circuit Needs
Dedicated VR
Level shifters
Retention buffers
Isolation Circuits
Autonomous DVFS
First glimpse - what does it take per domain?

**Circuit Needs**
- Dedicated VR
- Level shifters
- Retention buffers
- Isolation Circuits
- Autonomous DVFS

**Rail Needs**
- Dedicated grid
- Dedicated decap
First glimpse - what does it take per domain?

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System Needs
- Big always-on rail
- Validation complexity
- Cross domain speed paths

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Circuit area/complexity versus net power savings
Can we define domain boundary for net benefits
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Voltage Domain Granularity

Figure 1. Proposed Capacitive-Coupling (CC) WWL boosting along with Self-Induced VCC Collapse (SIC) for write VMIN reduction

Rail reduction
Voltage Domain Granularity

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Rail reduction turbo & low power

Figure 1. Proposed Capacitive-Coupling (CC) WWL boosting along with Self-Induced VCC Collapse (SIC) for write VMIN reduction

Figure 1


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Voltage Domain Granularity

Per Block

SOC

Per Partition

CPU

Within custom cells

0.3 - Vmax

CPU/GPU

0.3 - Vmax

PLL

1.2V

1.2V IO

0.3 - Vmax

SRAM

0.3 - Vmax

PMU

1.8V

1.8V IO


Rail reduction	 turbo & low power	 SRAM Vmin reduction

Figure 1. Proposed Capacitive-Coupling (CC) WWL boosting along with Self-Induced VCC Collapse (SIC) for write VMIN reduction


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VR needs

[2] Courtesy: Sriram V.; data from NTV core

- CMOS compatible VR
- Digital process friendly, low area overhead
- High conversion efficiency across wide range of v,i
- Fast response to take advantage of even brief idle periods
- Low leakage/ standby power
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Switched Capacitor Power Stage

Series Parallel circuit for best capacitance utilization w.r.t \( R_{out} \)
Lower bound Hysteretic Control

- Simplest control for low power overhead (30mW prototype) [4]
- Comparator leverages latch based sense amplifier design [3]
- Completely 'digital' for low area overhead
- No start up circuit required
- No assist needed for +ve VID transition
- Ripple is a function of $V_{out}$, $I_{load}$

Clock generation for 8 phase interleaving
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Simulation Results: Efficiency

Control and switching losses dominate at lower power
Adaptive switch scaling and higher power designs approach blue
Summary

- CMOS compatible VR
- Significant power reduction in the load from multi Vcc techniques
- Low area overhead, good efficiency across 0.5V-1.05V
- Extremely fast response, scalable, suitable for DVFS
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