Digital Control Options for Embedded DC-DC Converters in CMOS SoC

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Outline

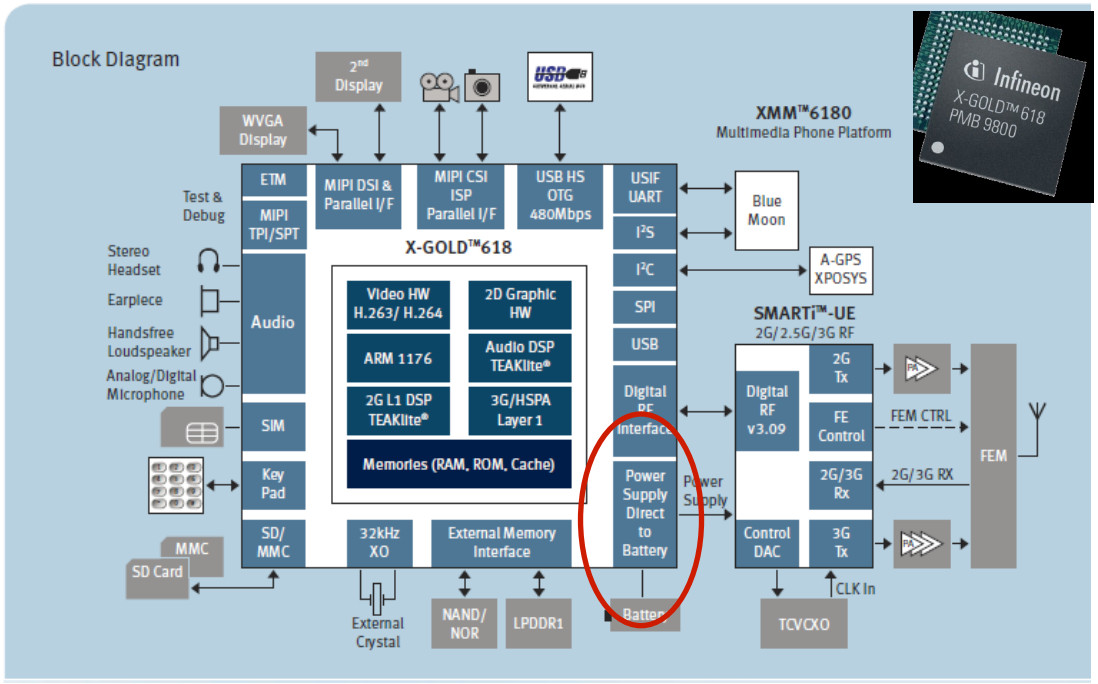
- Introduction
- Advantages of digital controllers
- Building blocks
  - DPWM
  - ADC
- Limit cycle oscillation
- Efficiency comparison
- Conclusion

Digitally Controlled Power Management in SoC

- Digital and analog baseband and power management functions are monolithically integrated in 65nm CMOS

X-GOLD™618

Cost efficient HSPA Baseband for Multimedia enabled Cellular Phones



2 x digitally controlled DCDC converter

22.2 A Digitally Controlled DC-DC Converter for SoC in 28nm CMOS

Franz Kuttner[1], Harun Habibovic[1], Thomas Hartig[1], Michael Fulde[1], Gernot Babin[1], Andreas Santner[1], Peter Bogner[1], Claus Kropf[1], Harald Riesslegger[1], Uwe Hodel[2]

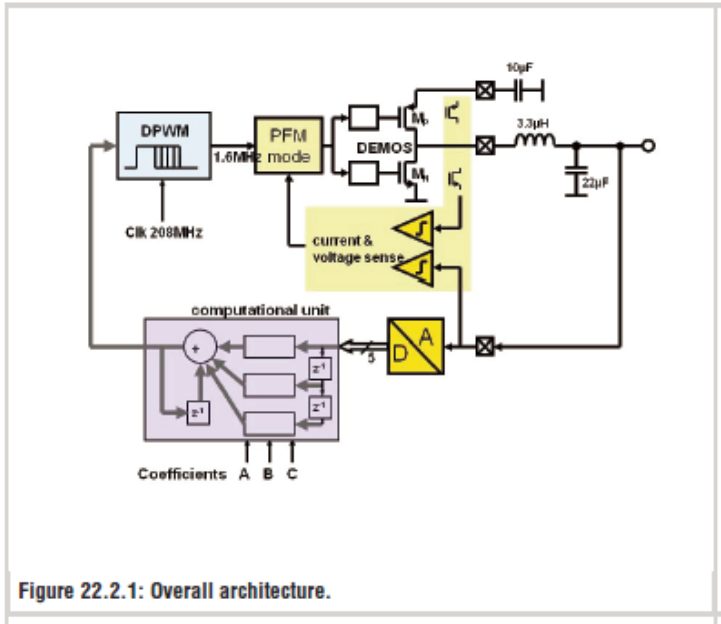
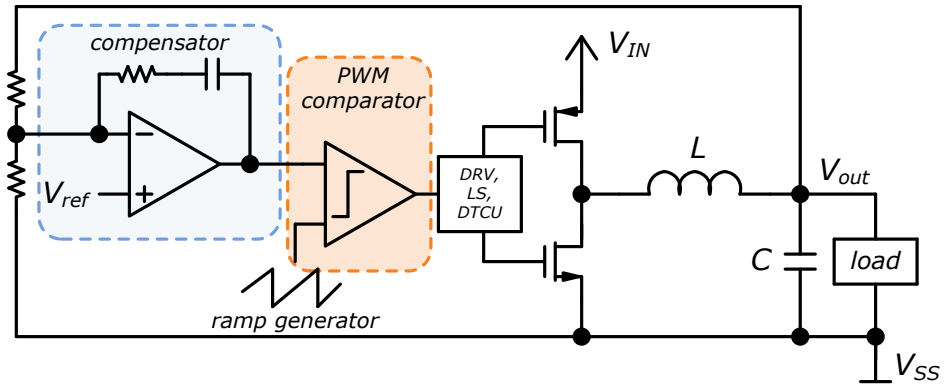


Figure 22.2.1: Overall architecture.

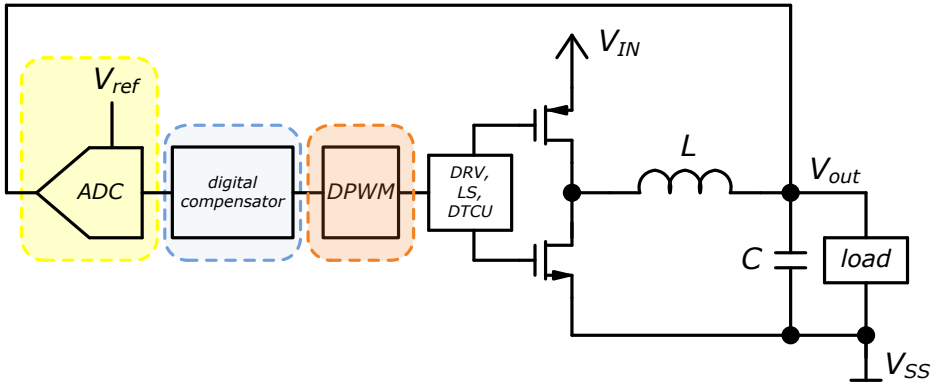
same DCDC already ported in 28nm CMOS [1]

Analog and Digitally Controlled DC-DC Buck Converters

Analog control



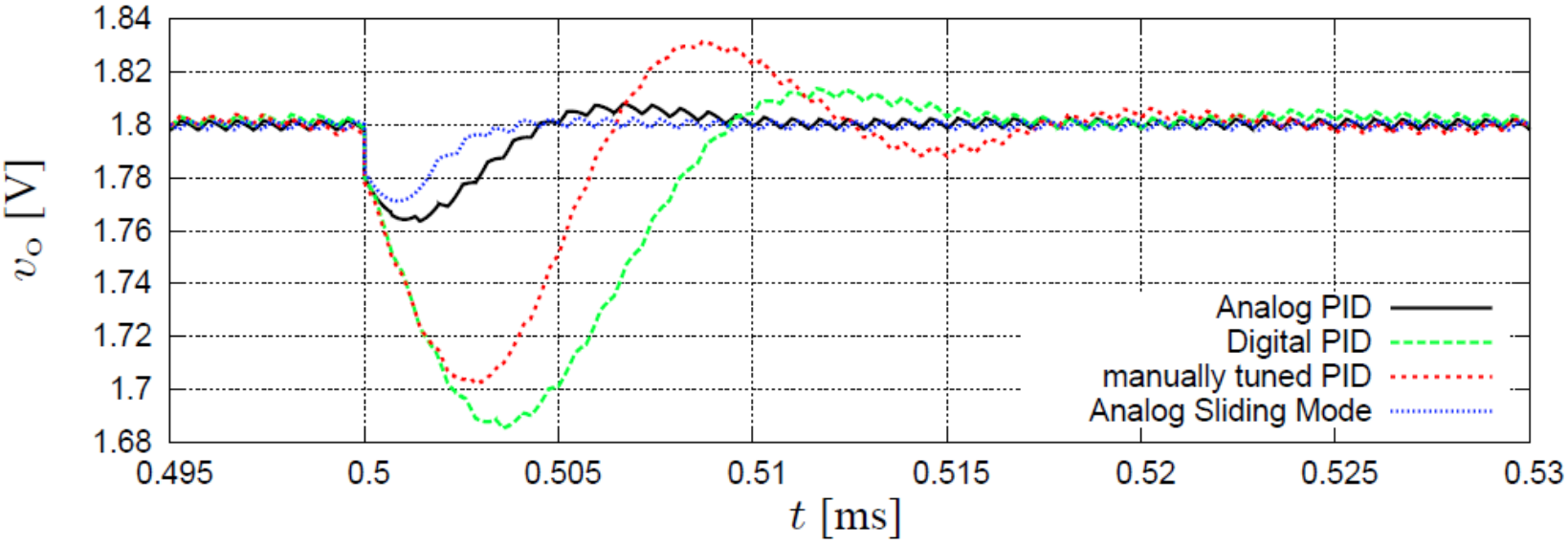
Digital control



- Analog control:
  - compensator compares a the scaled converter output voltage with a reference voltage
  - the error signal goes to a PWM which generates control pulses for the power stage
  - fine resolution of the output voltage
- Digital control
  - ADC converts output voltage into digital representation
  - digital compensator calculates actuating variable for the DPWM
  - DPWM generates control pulses for the power stage
  - only finite resolution of the output voltage

Comparison of Transient Performance for Different Controllers

- All the controllers have same bandwidths
- Analog controller structures generally are able to deliver a better transient performance than digital controllers in a certain operating point [4]

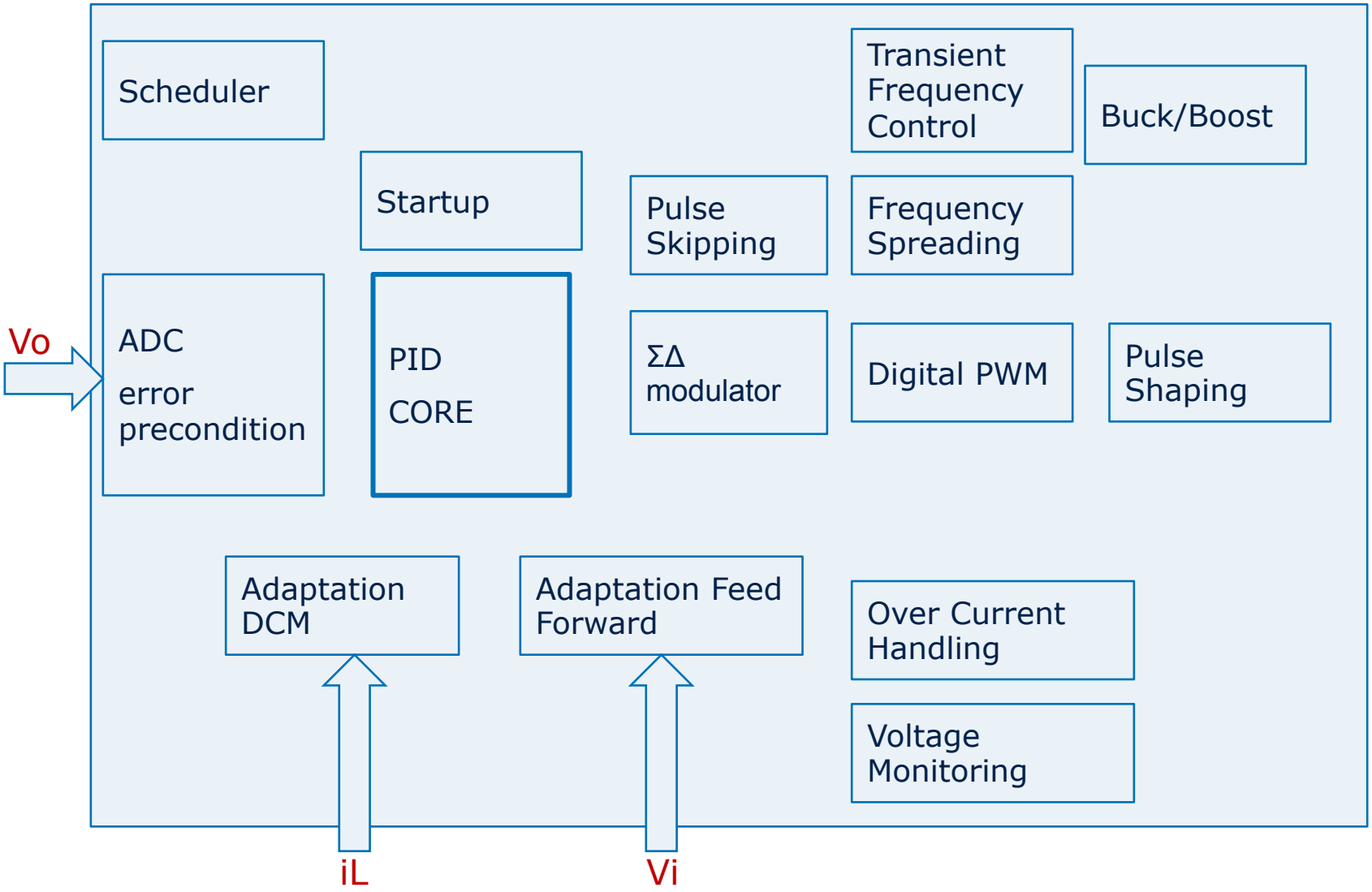


- Why do we often prefer digital implementations ?

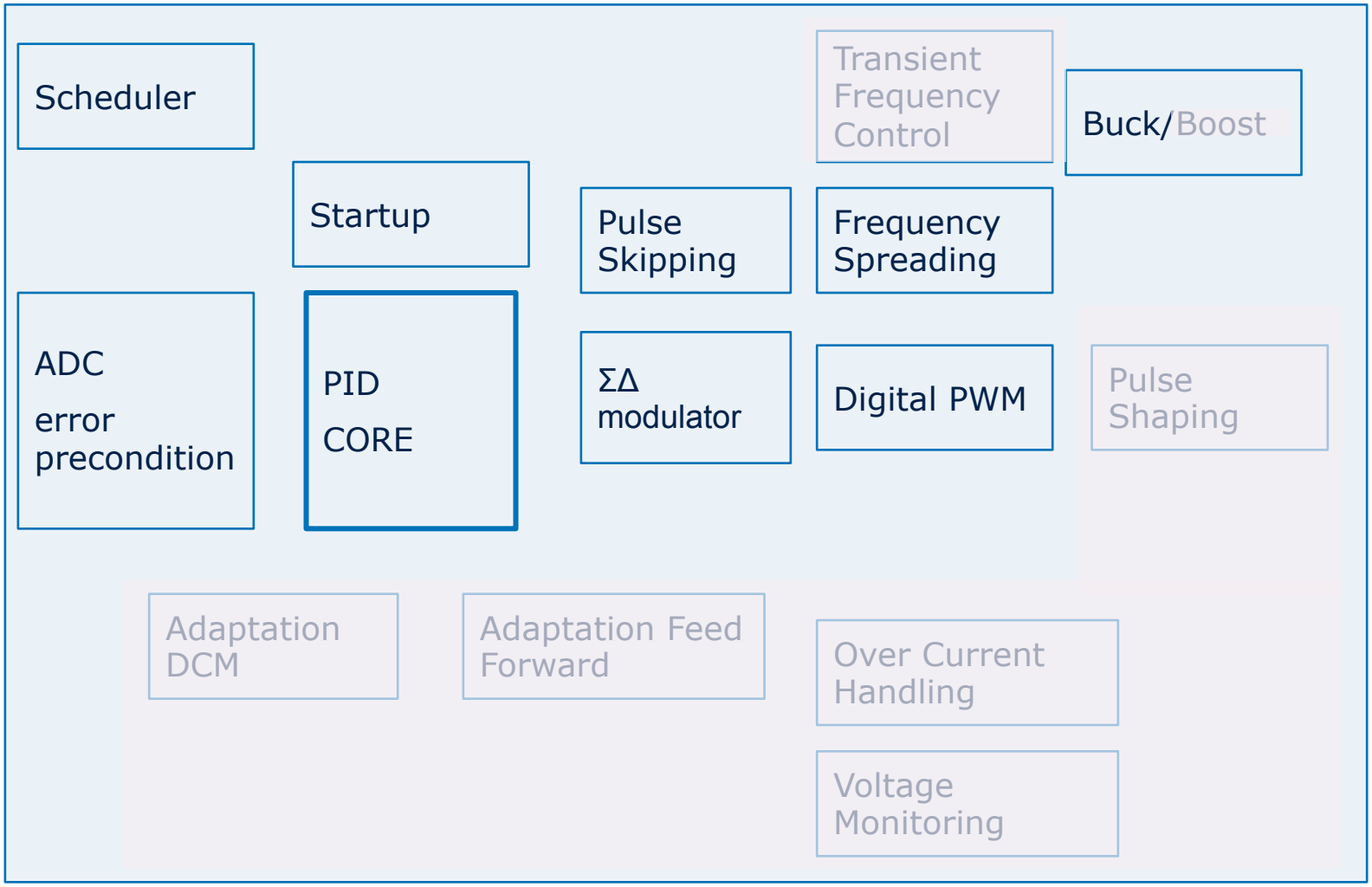
Why do we often Prefer Digital Controller?

- Can be easily ported to different technologies
- They are stable over process and temperature
- We can implement a lot of different features:
  - advanced control methods (e.g. non linear control)
  - provide different operating modes (PWM-CCM, PWM-DCM, Feed-Forward)
  - calibration algorithm
  - monitor functions
  - different controlled startup scenarios
  - frequency spreading
  - dynamic voltage scaling
  - digital dead time optimization
  - …

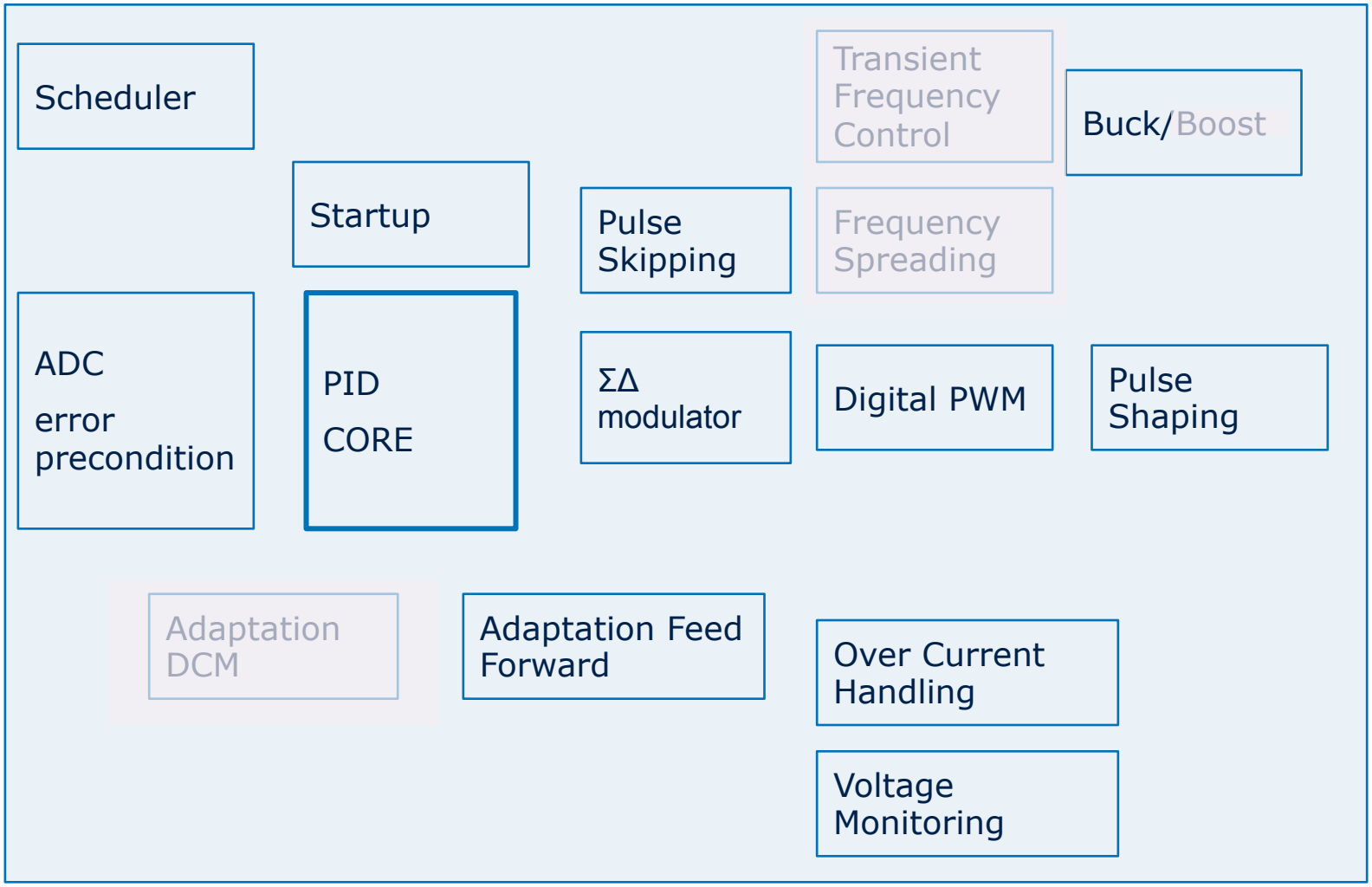
General Macro of Digitally Controlled DC-DC converter



Product A

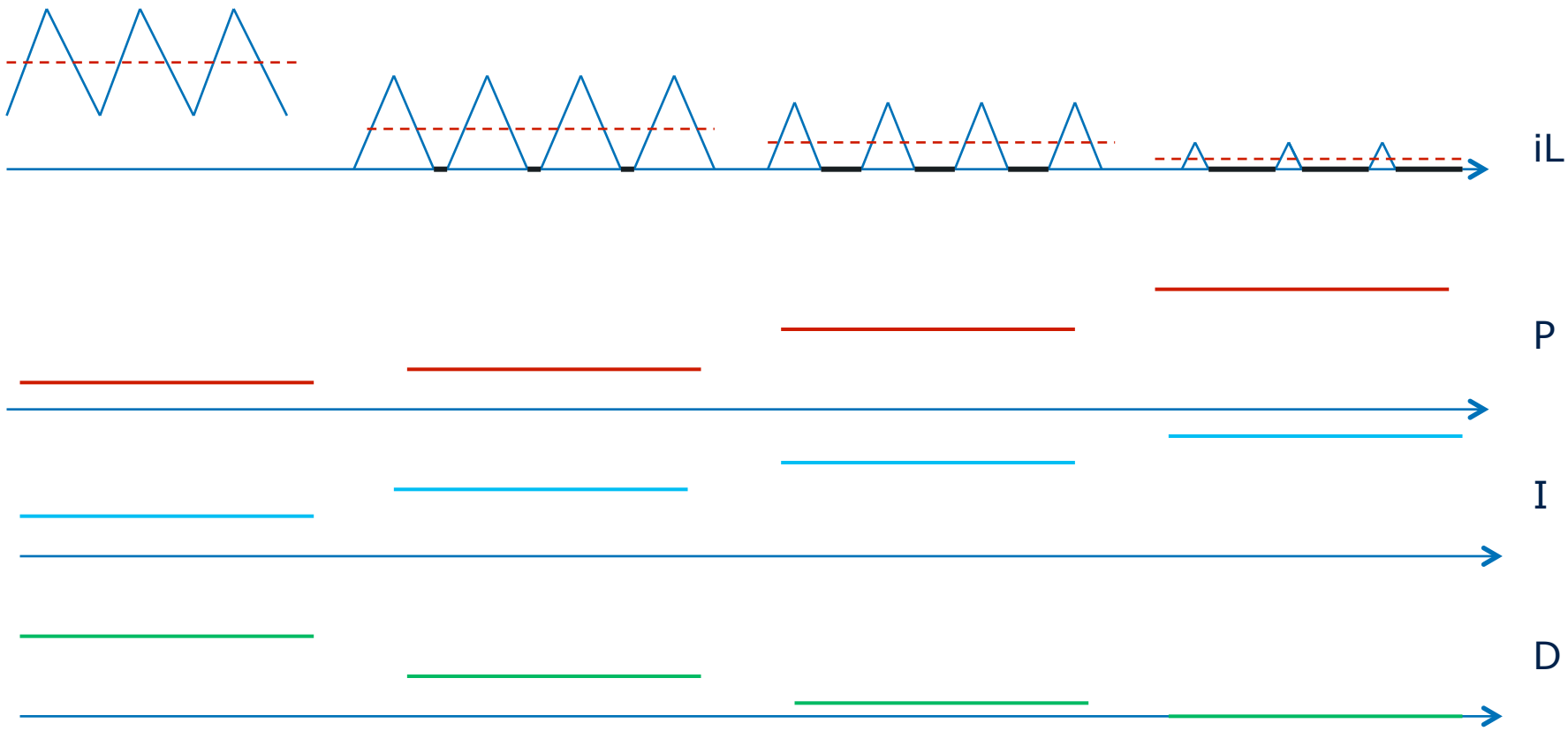


Product B

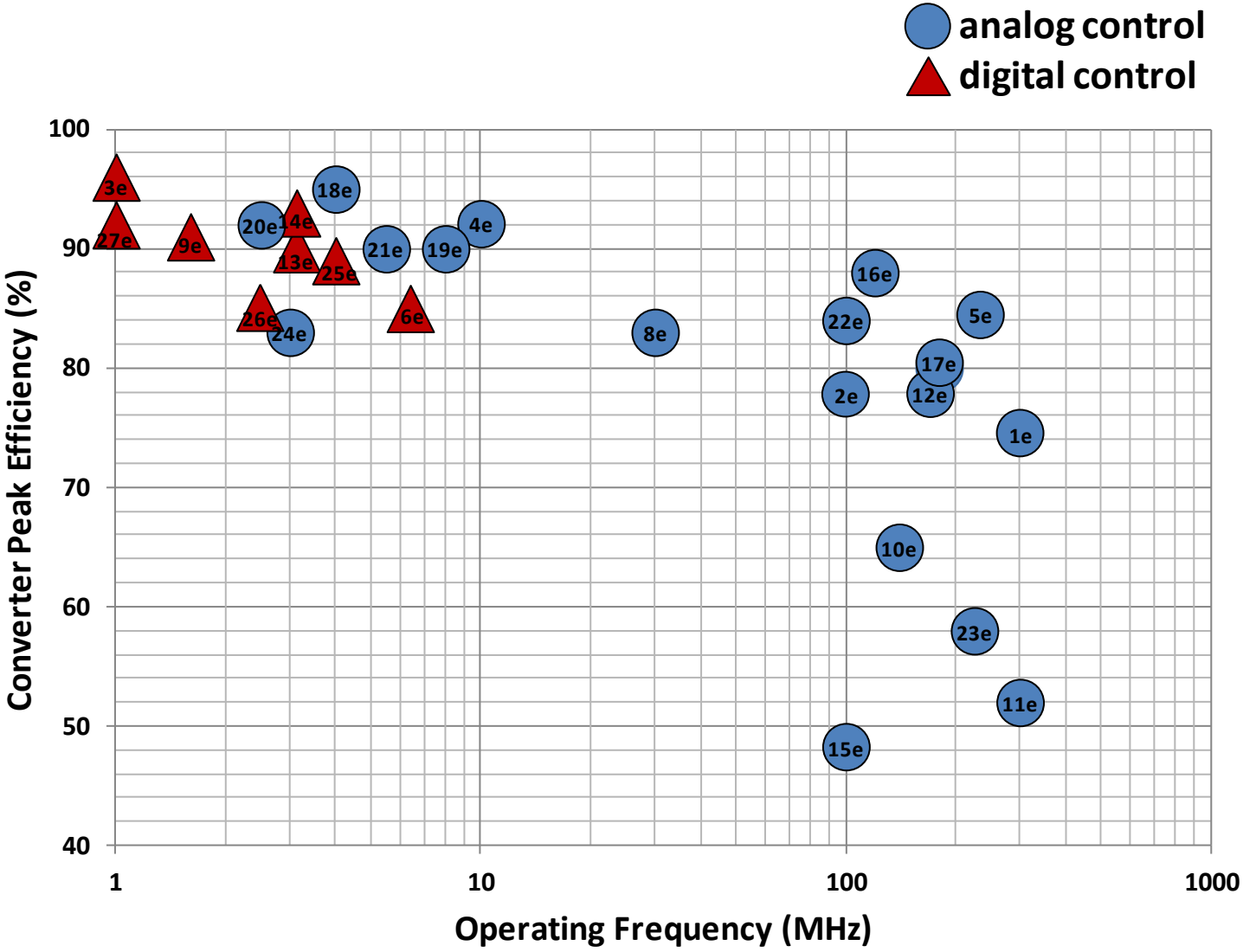


Automatic Controller Parameter Adaption for Different Operating Modes

- optimized set of controller parameters in CCM → not an optimum in DCM
- Adapt the coefficients according to the time interval where iL=0

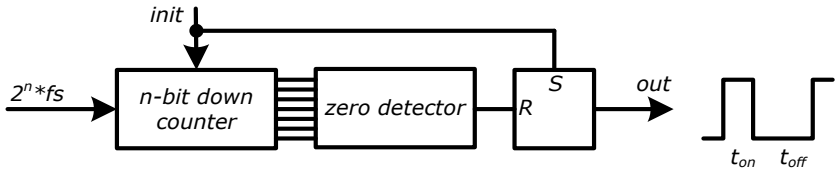


Published DC-DC Buck Converters: Analog Control vs. Digital Control

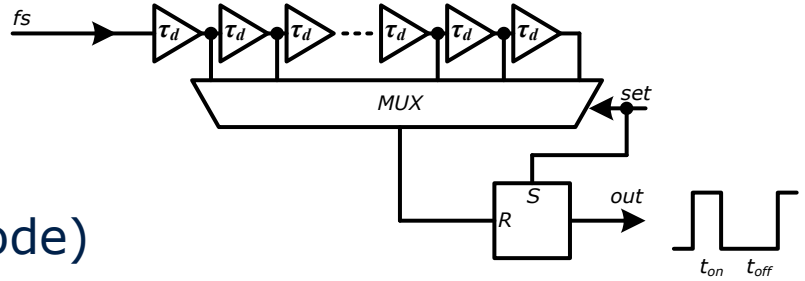


DPWM

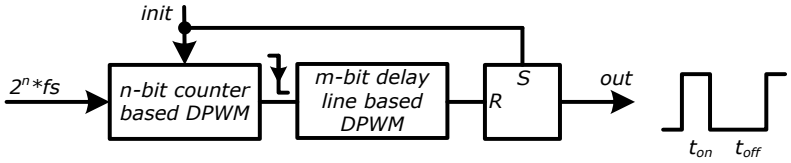
- Counter based DPWM
  - linear/monotonic
  - can be implemented in HDL
  - requires a high system clock: 2^n*fs
    (e.g. fs=5MHz, 7bit → clk ~640MHz;
    fs=80MHz, 7bit → ~10GHz!!)



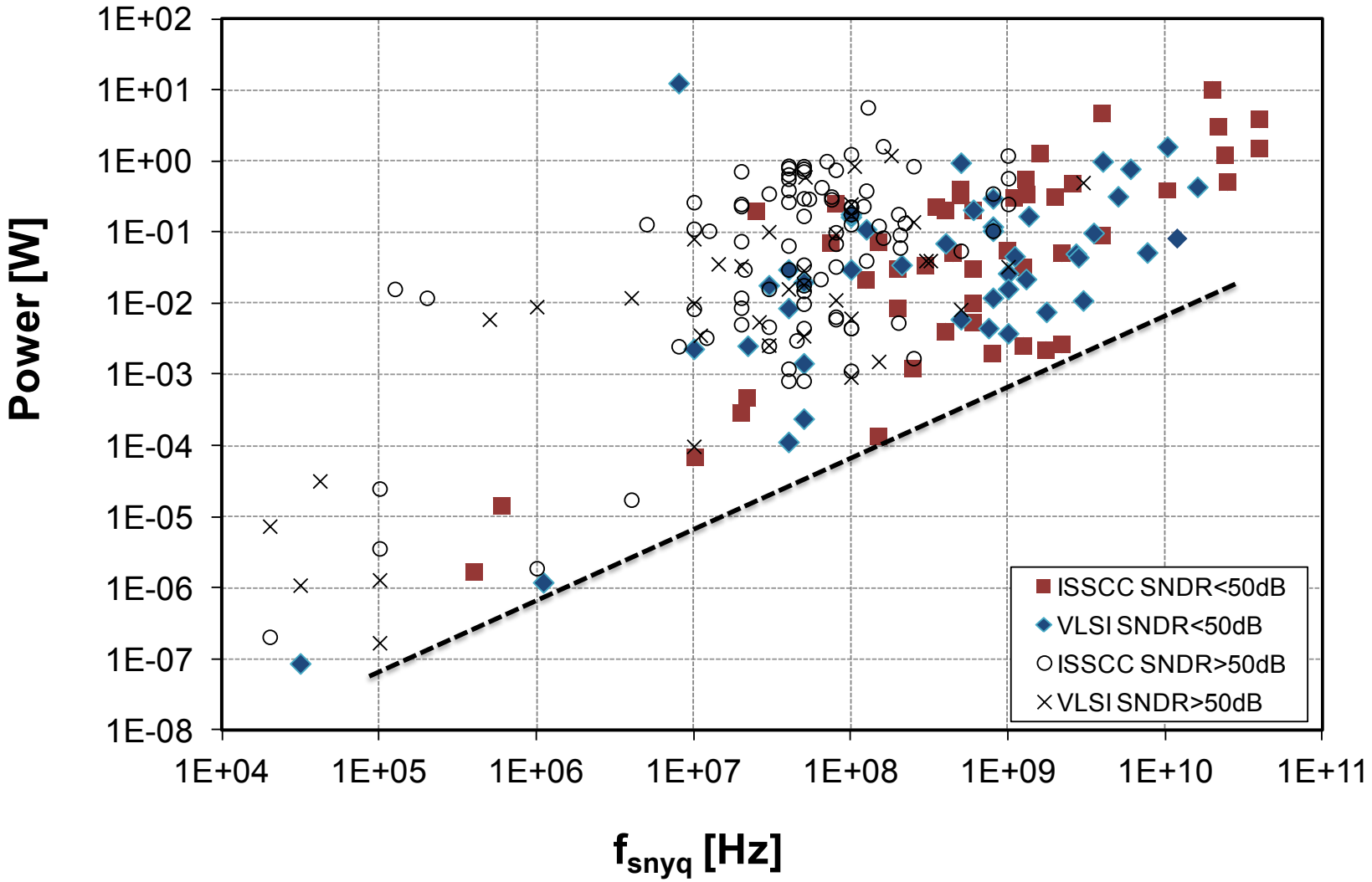
- Delay line based DPWM
  - high resolution
  - monotonic
  - large multiplexer (thermometer code)



- Hybrid DPWM
  - counter based DPWM (coarse) & delay line based DPWM (fine)
  - resolution: n+m bit
  - required system clock: 2^n*fs



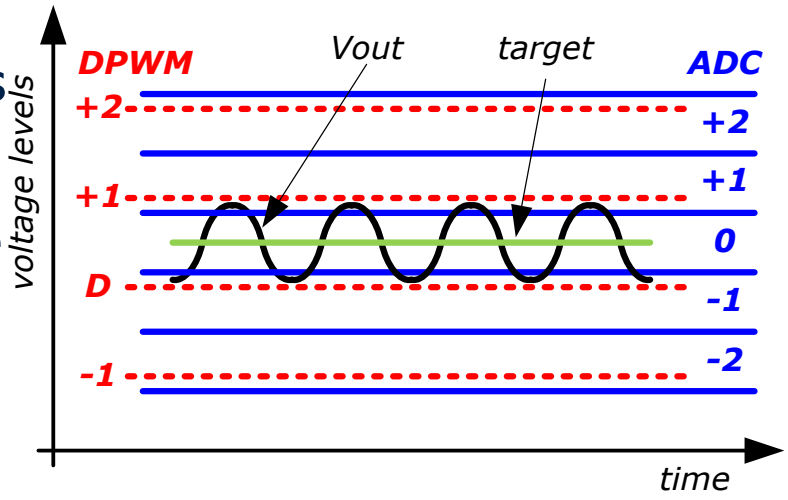
ADC Performance: Power vs. Bandwidth



[5] Data: B. Murmann, "ADC Performance Survey 1997-2012," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html.

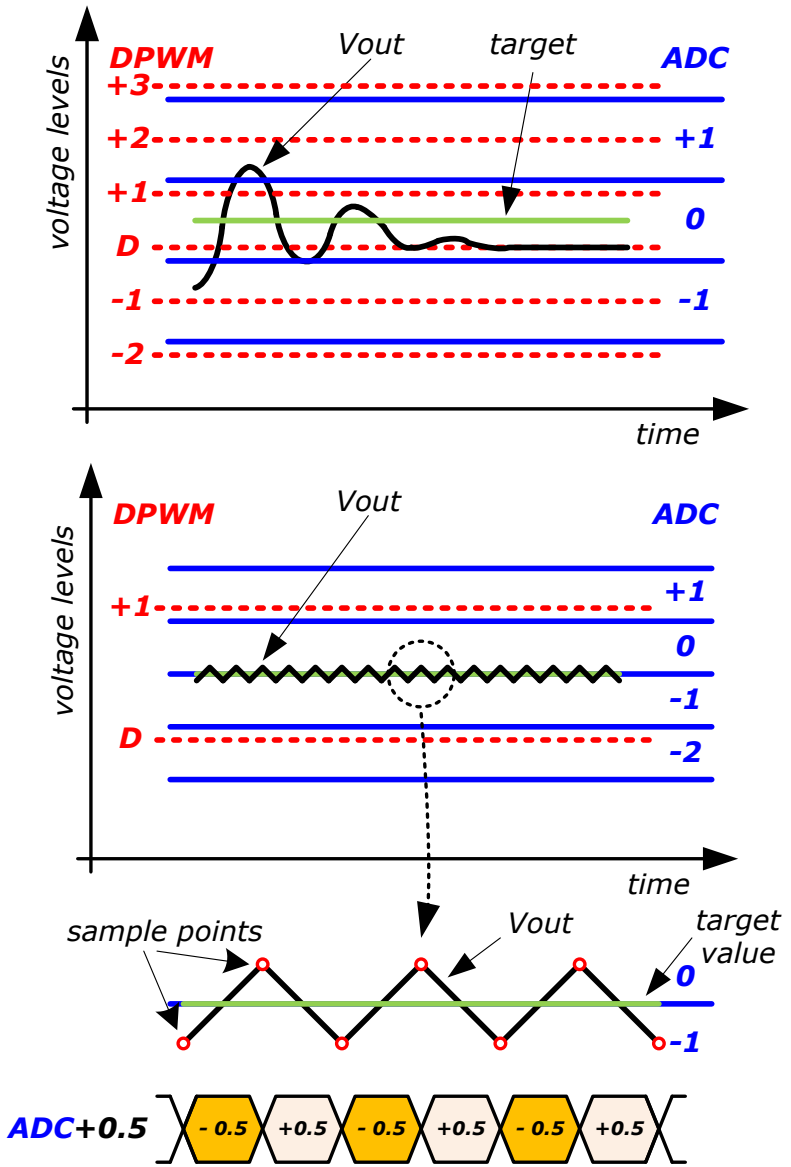
Limit Cycle Oscillation

- Limit cycle oscillation is only a problem in digitally controlled DC-DC converter
- It occurs due to quantization effects in the feedback loop
- output voltage oscillates around the nominal voltage
- It can occur if the resolution of the DPWM is lower than the resolution of the ADC



Ways to Avoid Limit Cycle Oscillations

- increase DPWM resolution [2]:
  $\Delta V_{o\_DWPM} < \Delta V_{ADC}$ with
  $\Delta V_{o\_DWPM} = V_{IN} * \Delta D$
  - can be done by:
    - increasing system clock
    - change the DPWM topology
    - dithering
    - ∑Δ-modulation
- shift the target value to a comparator threshold by adding 0.5 to the ADC output [1]:
  - high static accuracy
  - only one comparator has to be designed with low offset



Power Losses: fs=1.6MHz vs. 80MHz (50x)

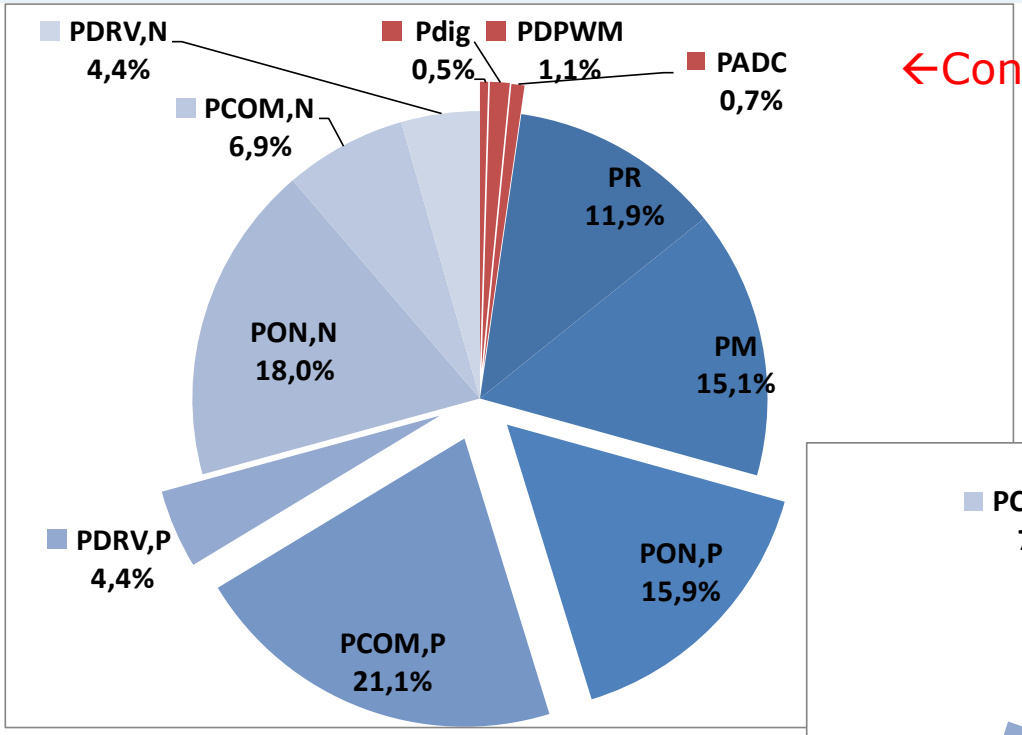
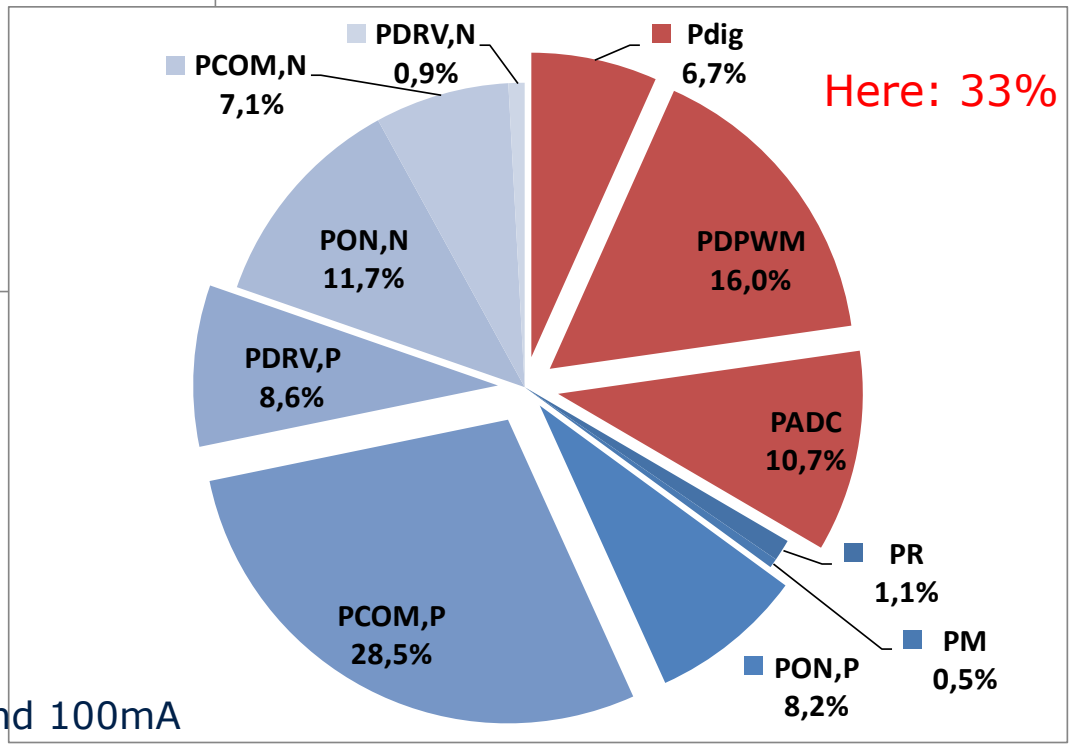


Fig.1: 1.6MHz, Efficiency=90%

←Controller+DPWM+ADC: 2,3%

Fig.2: 80MHz, Efficiency=73%



Conditions:

- 65nm CMOS, 100mA load
- 3.3uH vs. 200nH
- switches optimized for peak eff. around 100mA

Conclusion

- Digital power control allows very flexible power conversion
- Going to high switching frequency (→PowerSoC applications):
  - No blocking point in using digital power control
  - We can implement
    - high resolution DPWMs,
    - fast ADCs
  - We know techniques to avoid limit cycle oscillation
  - BUT: efficiency!!!
  - Analog control: much simpler (eg. COOT, hysteretic controller), therefore better efficiency
- Future will show more and more digital control also at higher frequencies, since technology scaling will help digital control

Bibliography

- [1] A digitally controlled DC-DC converter for SoC in 28nm CMOS-F.; Habibovic, H.; Hartig, T.; Fulde, M.; Babin, G.; Santner, A.; Bogner, P.; Kropf, C.; Riesslegger, H.; Hodel, U.; - Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International
- [2] Quantization Resolution and Limit Cycling in Digitally Controlled PWM Converters; Peterchev, A.V.; Sanders S.R., IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 18, NO.1 JANUARY 2003
- [3] A Digitally Controlled Linear Voltage Regulator in a 65nm CMOS Process; Jackum, T.; Riederer, R.; Maderbacher, G.; Pribyl, W., Proceedings of ICECS , 2010
- [4] Comparative study of linear and non-linear integrated control schemes applied to a Buck converter for mobile applications - Priewasser R., Agostinelli M., Marsili S., Straeussnig D., Huemer M. - Austrochip 2009 Tagungsband - pp. 51-56
- [5] Data: B. Murmann, "ADC Performance Survey 1997-2012," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html.