Deep Trench Capacitors for Switched Capacitor Voltage Converters

Jae-sun Seo, Albert Young, Robert Montoye, Leland Chang

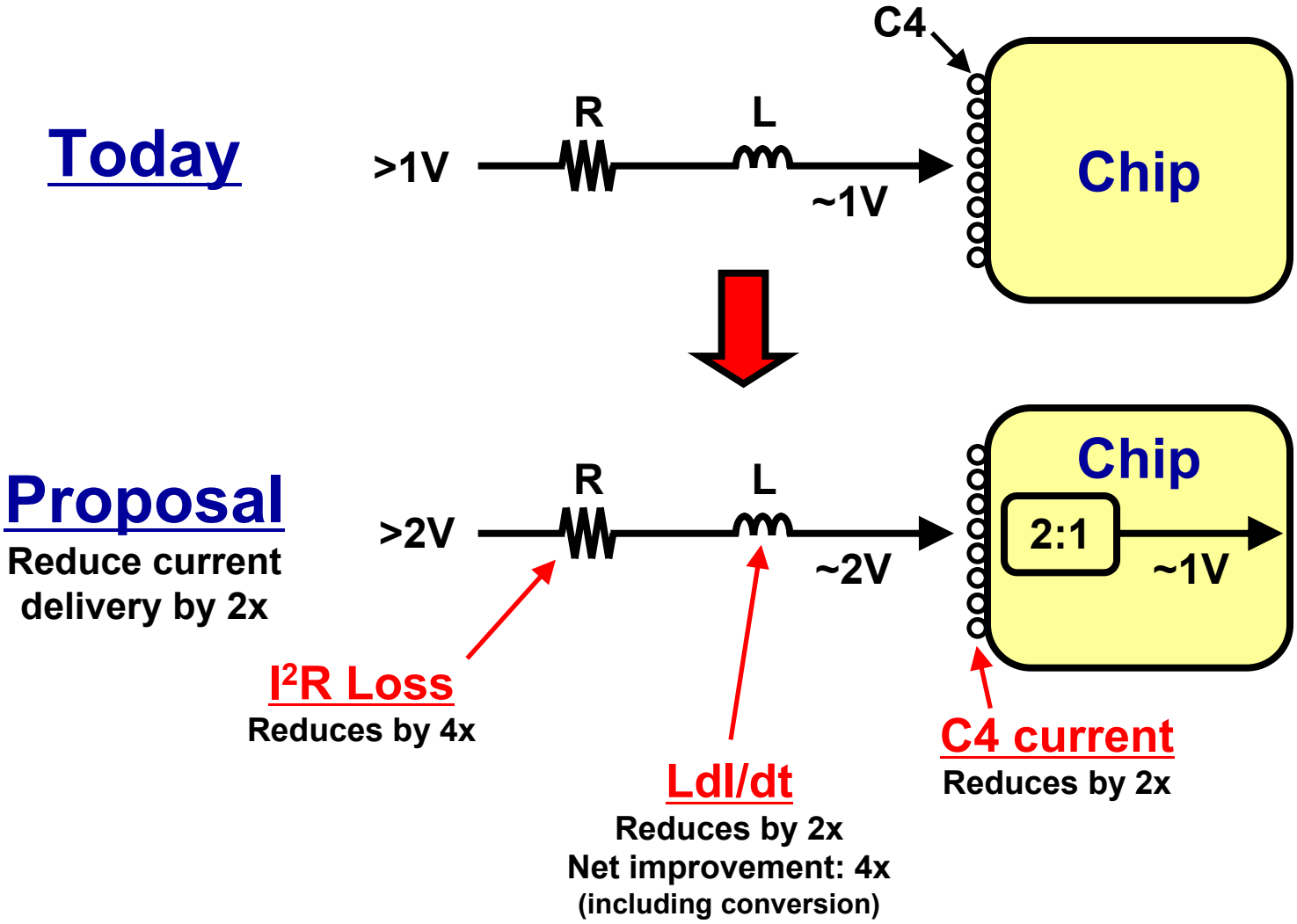
IBM T. J. Watson Research Center

3rd International Workshop for Power Supply on Chip
Nov 17th, 2012

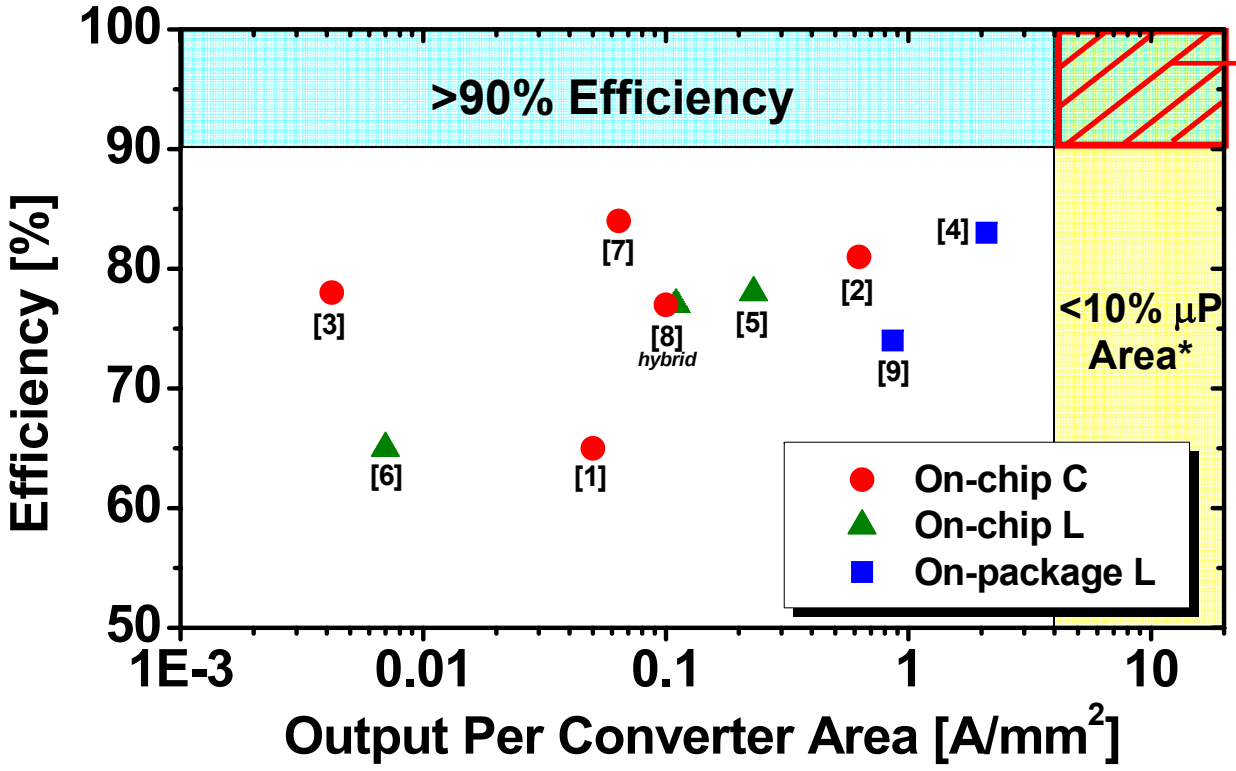
Outline

- Motivation
- Switched-capacitor voltage converter with deep trench capacitor technology
- Design Tradeoffs for Efficiency and Current Density
- Chip floorplanning / Application
- Summary

Power Delivery w/ 2:1 Step Down



Previous Work on On-Chip Voltage Conversion



[1] Le, ISSCC10, 32nm
[2] Ramadass, ISSCC10, 45nm
[3] Kwong, ISSCC08, 65nm
[4] Hazucha, JSSC05, 90nm
[5] Wibben, JSSC08, 130nm
[6] Abedinpour, ISSCC06, 180nm
[7] Patounakis, JSSC04, 250nm
[8] Kim, JSSC12, 130nm
[9] Sturken, ISSCC12, 45nm

*Assumption: 1V, 200W, 500mm^2

- **Typically 3 approaches : (1) linear (2) switched-capacitor (3) buck**
  - **Linear regulator not suitable for high-voltage power delivery**
- **Difficult to achieve high efficiency & current density simultaneously**

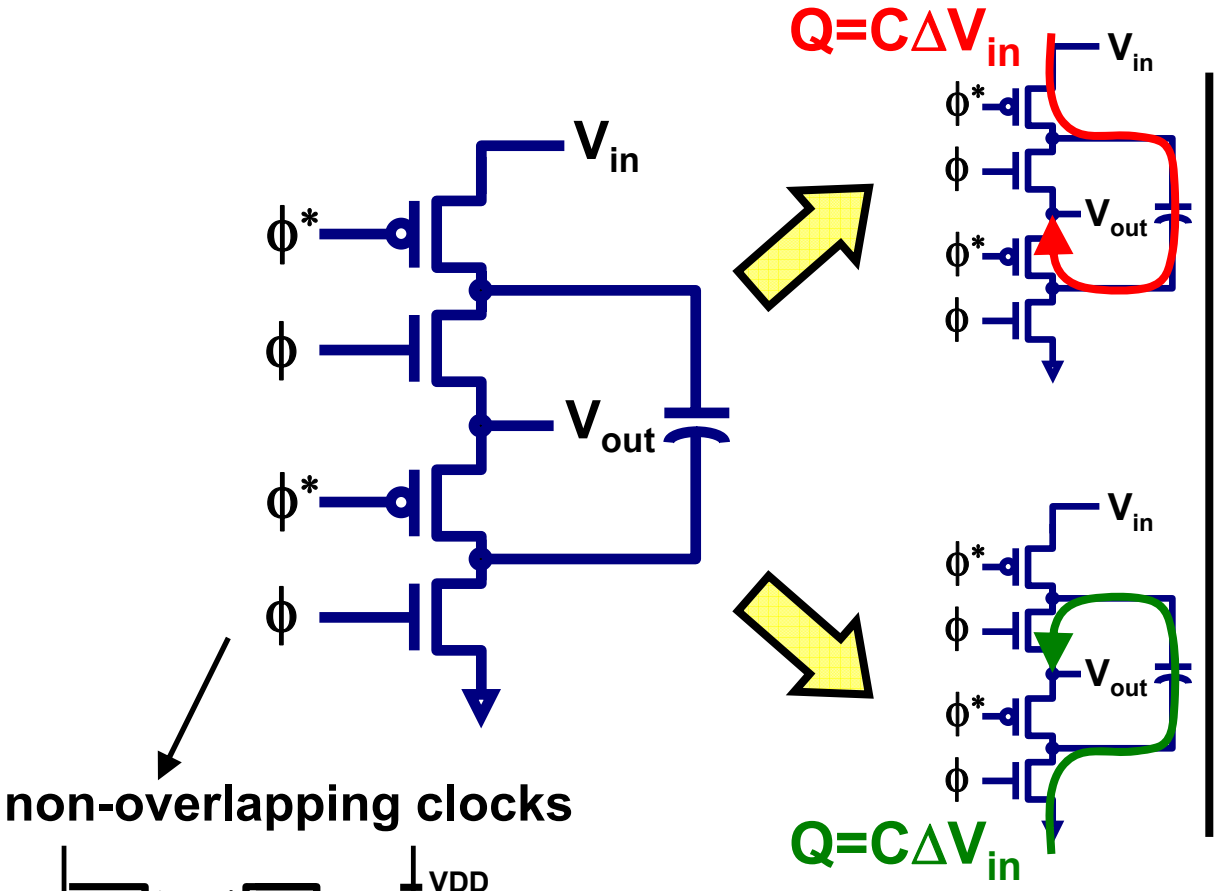
Why Switched-Capacitor Converters?

- **High-voltage power delivery**
  - **Offers strong benefits especially for high-current applications or when significant package loss exists**
  - **Achievable by switched-capacitor voltage converters with fixed ratio step-down**
  - **Linear regulator : no high-voltage delivery benefit**
- **Low-cost on-chip integration with existing technology**
  - **Buck converter : on-chip inductor material with high-enough Q not quite there, external inductors not good for integration**
- **With dense deep trench capacitors, switched-capacitor converter can achieve high-efficiency and high current density**

Outline

- Motivation
- **Switched-capacitor voltage converter with deep trench capacitor technology**
- Design Tradeoffs for Efficiency and Current Density
- Chip floorplanning / Application
- Summary

2:1 Switched-Capacitor Converter

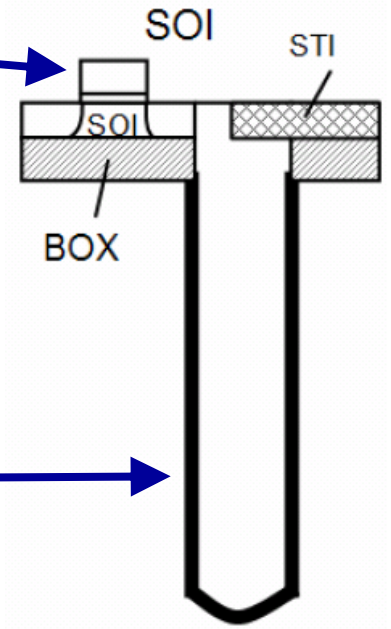


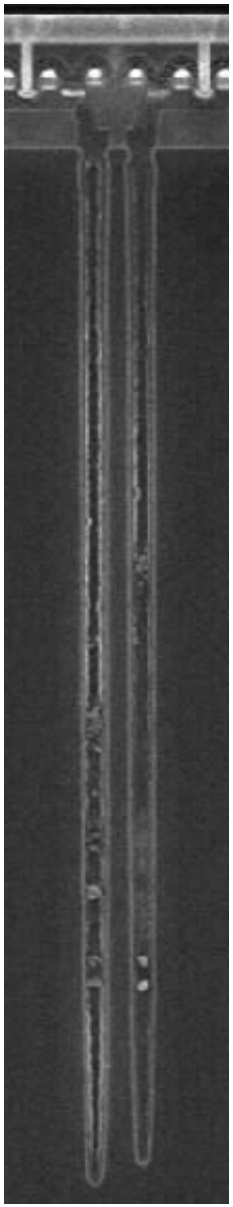
- $V_{out} = ½\ V_{in}(1–\Delta)$
- $I_{out} = 2\Delta C V_{in} f$
- Intrinsic efficiency $= (1–\Delta)$

- Small Δ offset in V_{out} generates current
- With traditional capacitor, cannot really achieve intrinsic efficiency or sufficient output current

Deep Trench Capacitor Technology

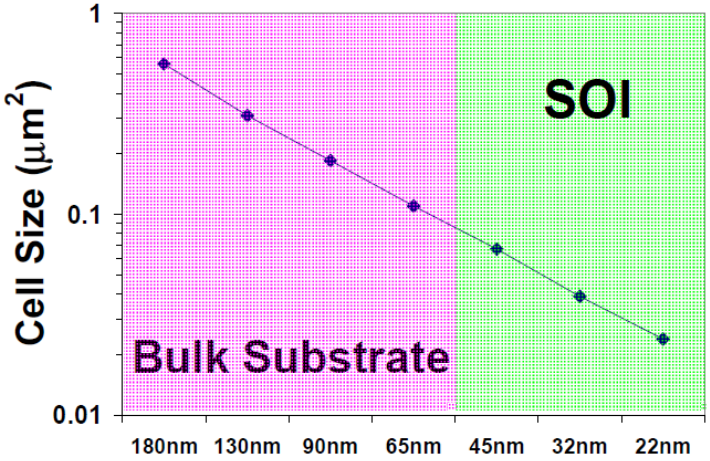
- **High performance SOI CMOS**
  - Yields low loss switch
  - Floating body FET with buried oxide isolation
    - Facilitates stacking of thin-oxide devices for high voltage conversion
- **Deep trench capacitor**
  - High density, low loss vs. MOS capacitor:
    - Area efficiency: >25× better density
    - Conversion efficiency: >10× better parasitics
  - High-κ storage node dielectric introduced in 32nm, metal liner mitigates poly depletion





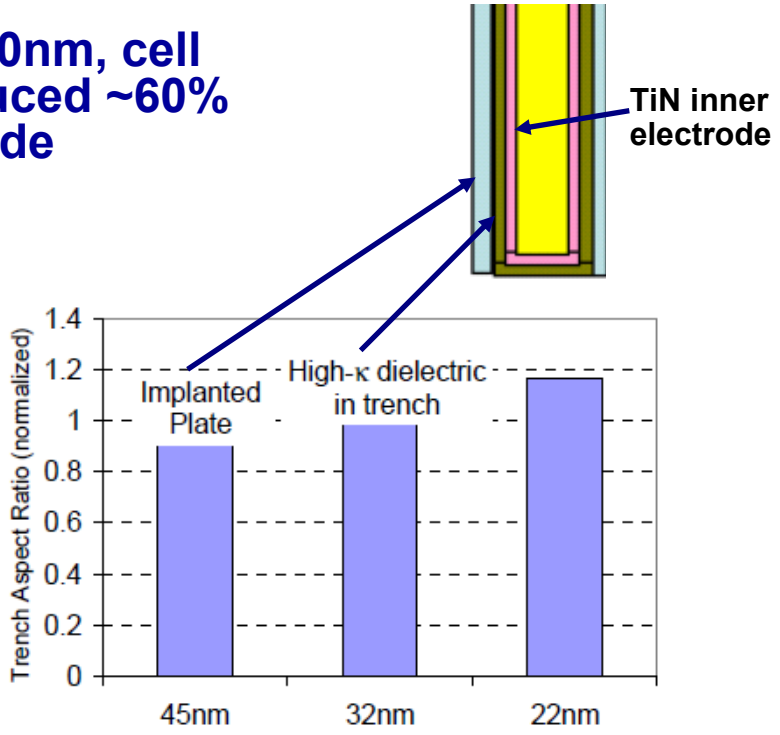
32nm SOI eDRAM
(Wang, IEDM 2009)

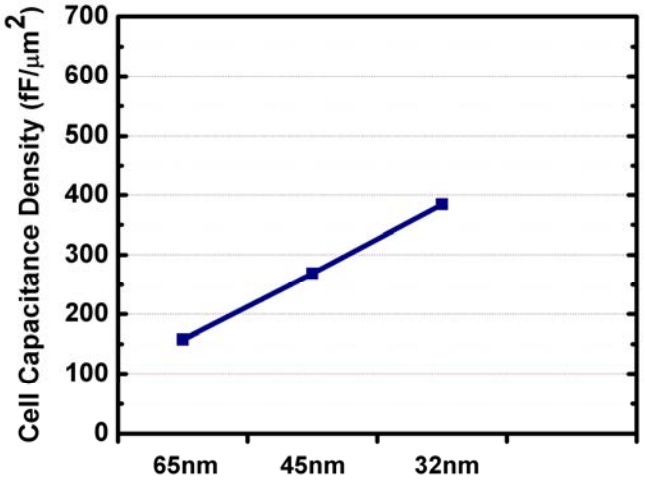
Scaling Trend of Deep Trench Capacitor



- IBM's embedded DRAM implemented with deep trench capacitor
- Since 180nm, cell size reduced ~60% every node

Wang, IEDM 2009



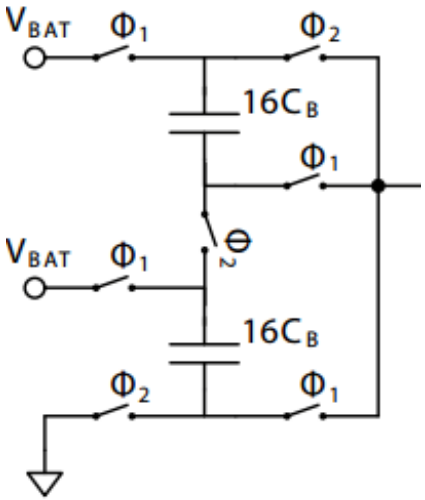


- eDRAM cell capacitance density scales well, path shown for 22nm

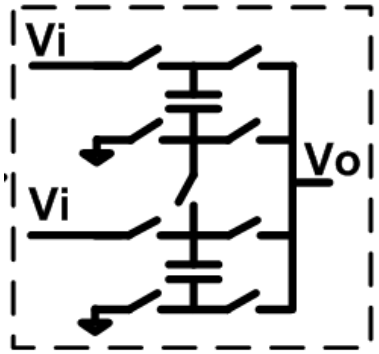
- New technology elements + modest increase in trench AR → optimal storage capacitance

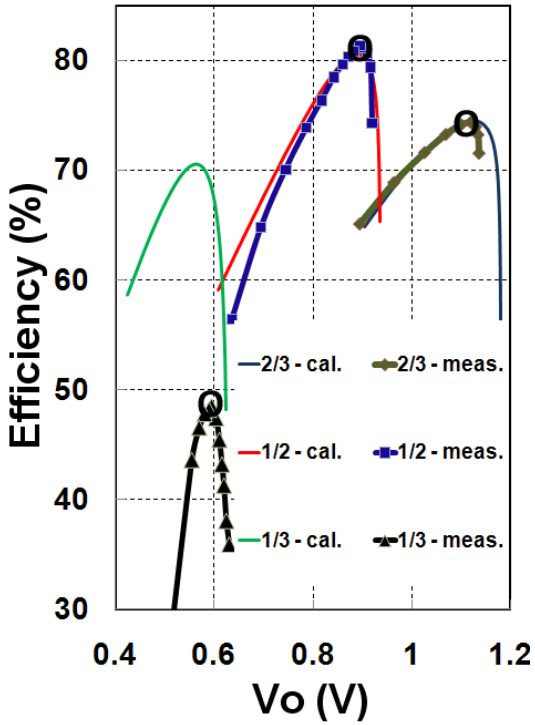
Multiple Conversion Ratios (3:1, 3:2, …)

Ramadass, ISSSCC 2010



Le, ISSSCC 2010



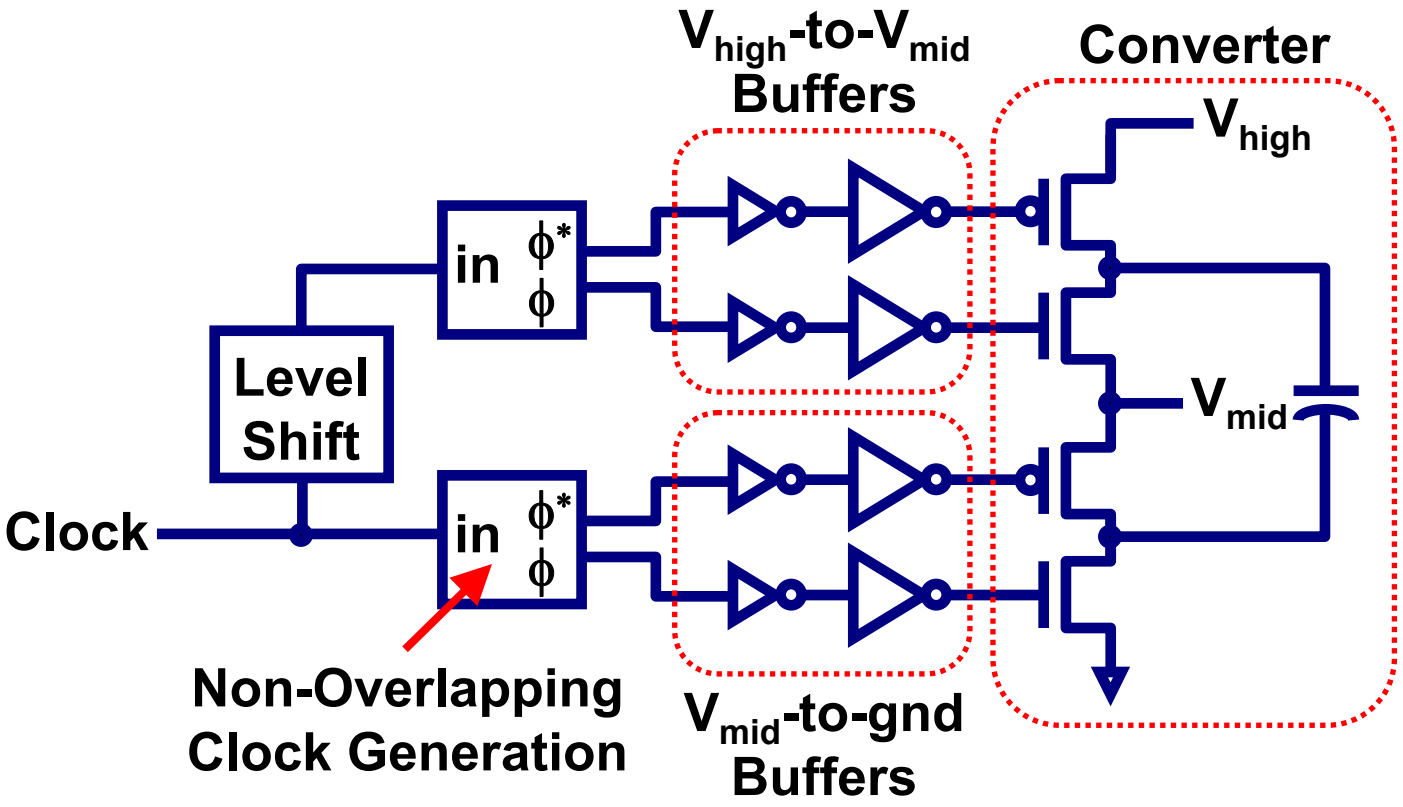


- **Different conversion ratios, reconfigurable converters, hybrid conversion schemes are possible**
- **However, they require more area (than 2:1), not necessarily favorable in terms of current density for high-current microprocessors**
  - **Depends on whether the application requires a continuously wide range of output voltages**

Outline

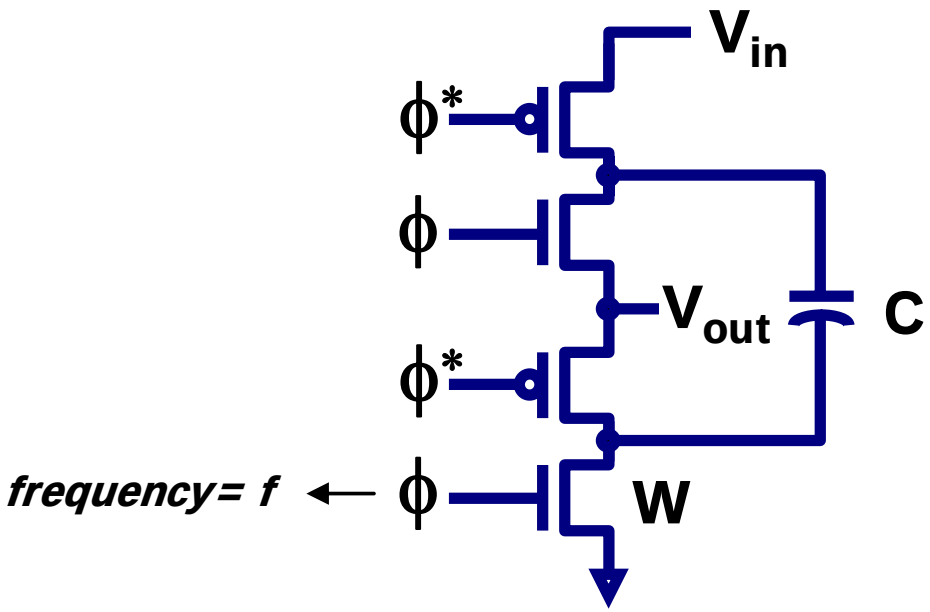
- Motivation
- Switched-capacitor voltage converter with deep trench capacitor technology
- **Design Tradeoffs for Efficiency and Current Density**
- Chip floorplanning / Application
- Summary

2:1 Switched-Capacitor Converter Circuits



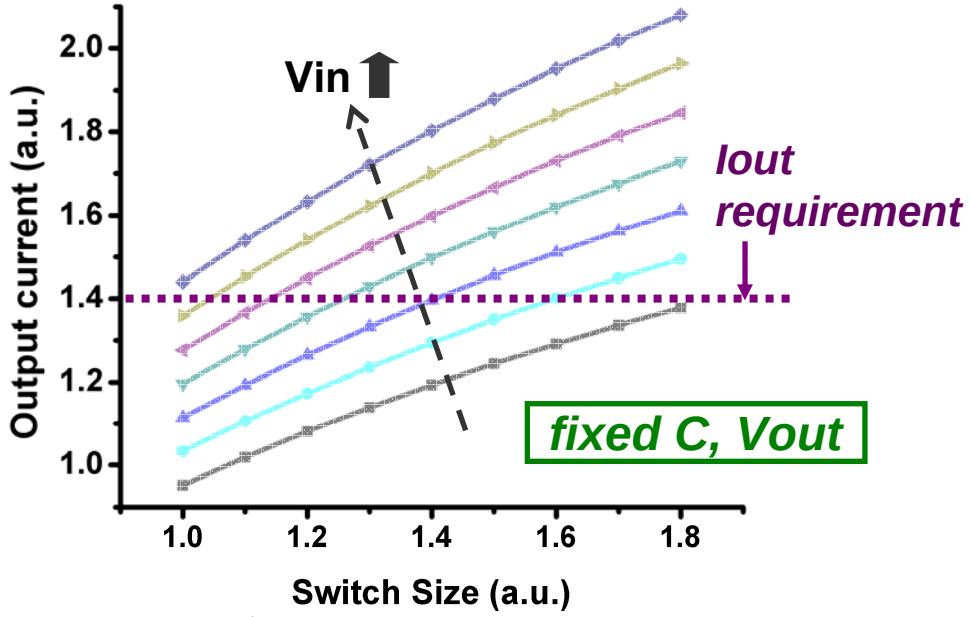
- Using level shifters / stacked buffers, no thick-oxide devices required
- External supplies of negligible current for ϕ/ϕ^* generation

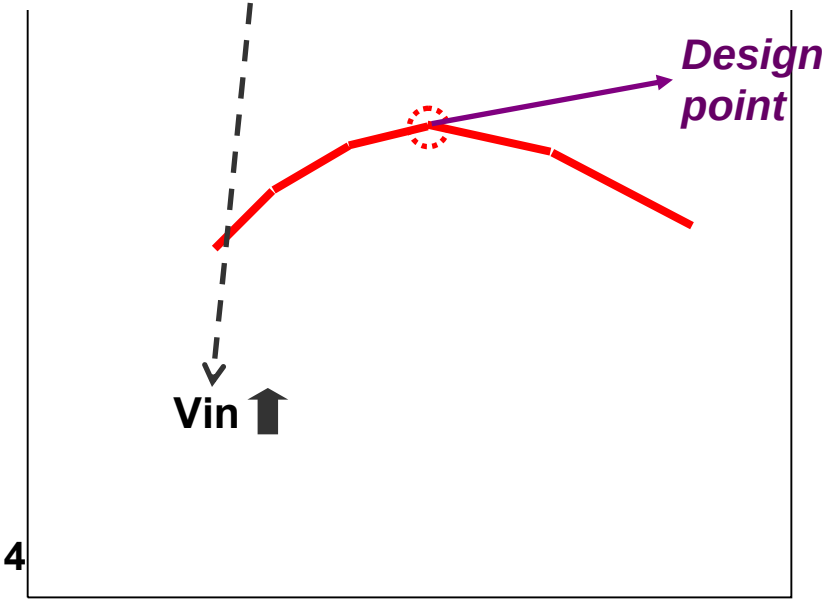
2:1 Switched-Cap Single-Phase Design Point



- $V_{out} = ½*Vin*(1-\Delta)$
- $I_{out} = 2*C*Vin*\Delta*f$
- Efficiency = $1-\Delta-k*W*f$
- Trade-off in efficiency, area, output current by selecting Vin, C, W, frequency, etc.
- Objective: high efficiency with that satisfies required output current for an application

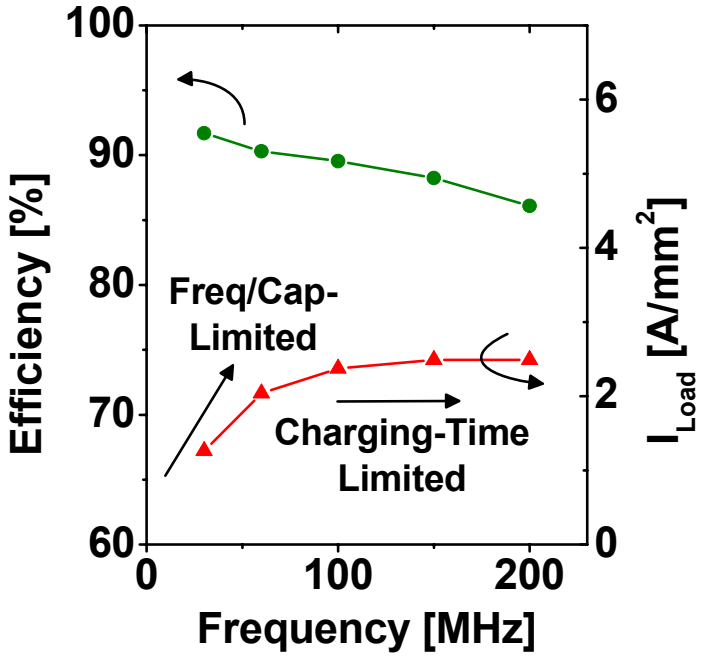
Efficiency / Output Current Optimization

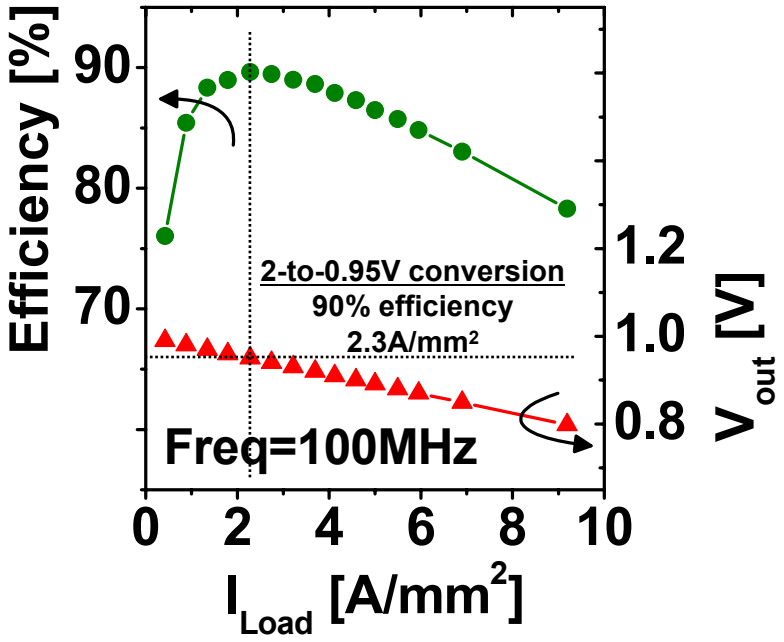




- For a certain application, following specs will be fixed
  - Target supply voltage
  - Required output current
  - Allowable area for SC converters → fixed flying cap
- Still, designers have freedom on the following to optimize efficiency
  - Vin (Δ)
  - Switch sizes
  - Frequency
  - Need to keep balance between Δ losses and switching (W, freq.) losses

Measurements of 45nm 2:1 SC Converter

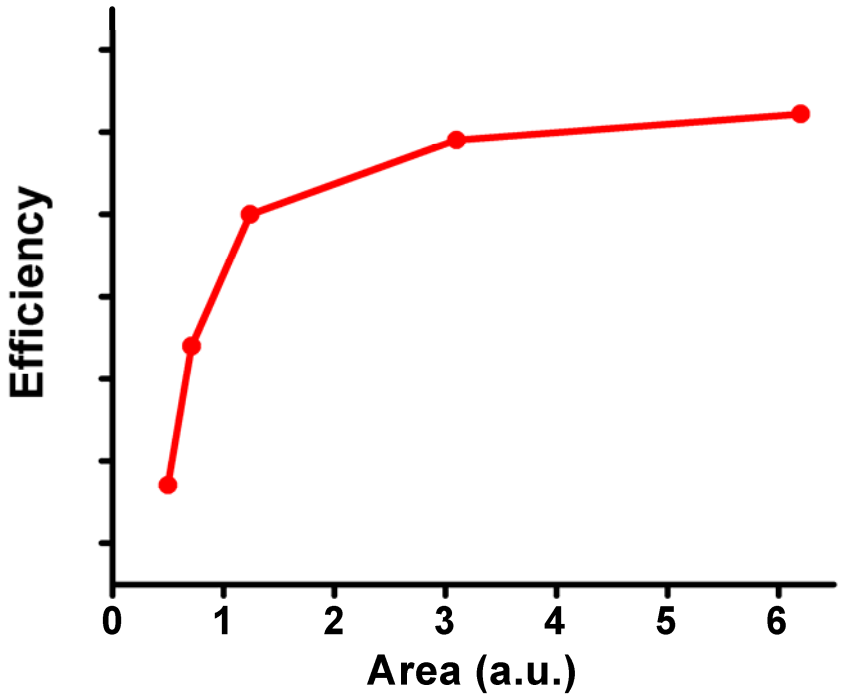




Chang, VLSI Symp. 2010

- **Output current is bounded by flying cap charge (when freq. is low), and RC of switch (when freq. is high)**
- **Achieved 90% efficiency (Δ~5%, clock losses ~5%) with 2.3A/mm^2**
  - **Higher current density achievable by trading off efficiency**

Tradeoff: Efficiency vs. SC Area

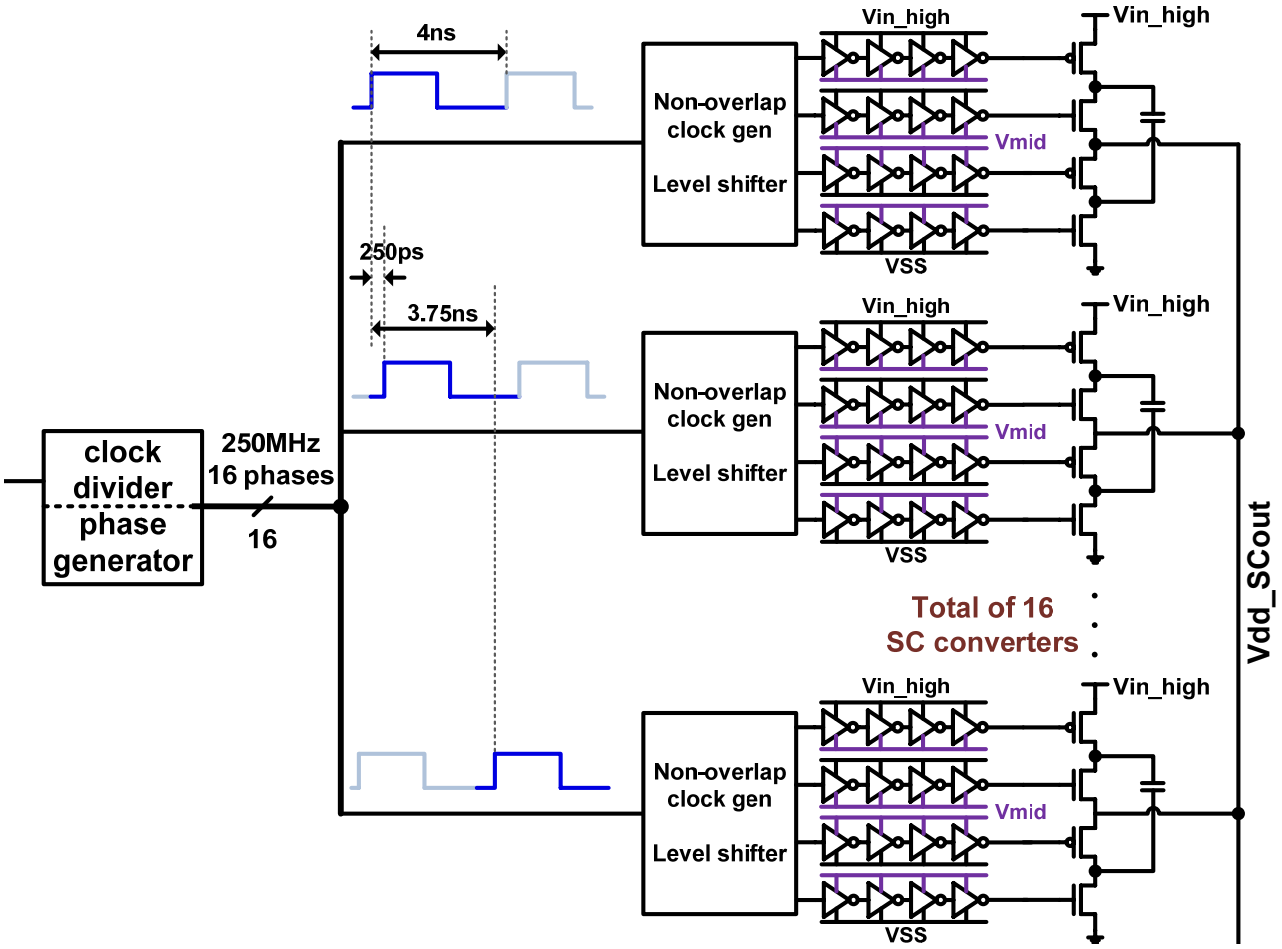


- Once the output current requirement is set, spending more area for SC converters (flying capacitors) increases power efficiency
- But eventually saturates due to minimum switching loss and ∆-related loss

Outline

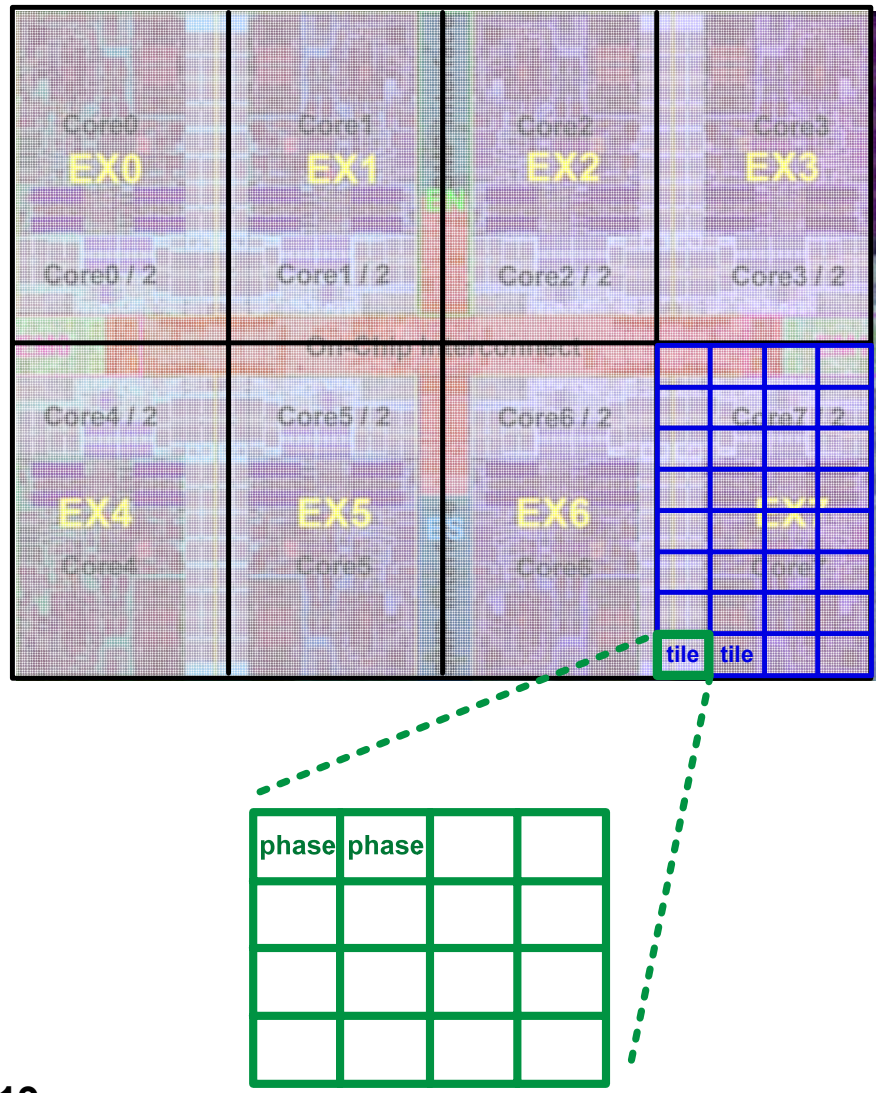
- Motivation
- Switched-capacitor voltage converter with deep trench capacitor technology
- Design Tradeoffs for Efficiency and Current Density
- **Chip floorplanning / Application**
- Summary

Interleaved Switched-Cap Converters



- Reduce output ripple
- Main processor clock could be tapped and divided for multiple phases

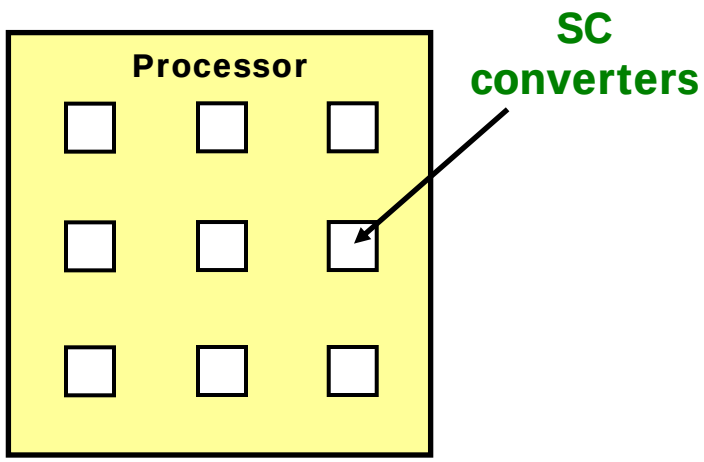
Chip Floorplanning



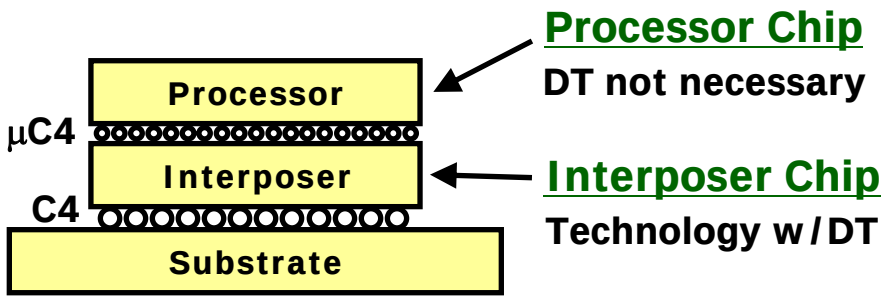
- One switched-capacitor tile consists of multiple interleaved SC converters
- Multiple switched-capacitor tiles could be placed across a processor
- Each tile has its own SC control, enable, duty cycle
  - Output could be all tied together
  - SC converters near hot spots would be turned on more frequently than idle spots

2-D / 3-D Implementation Options

2-D implementation:
Allocate certain area for SC



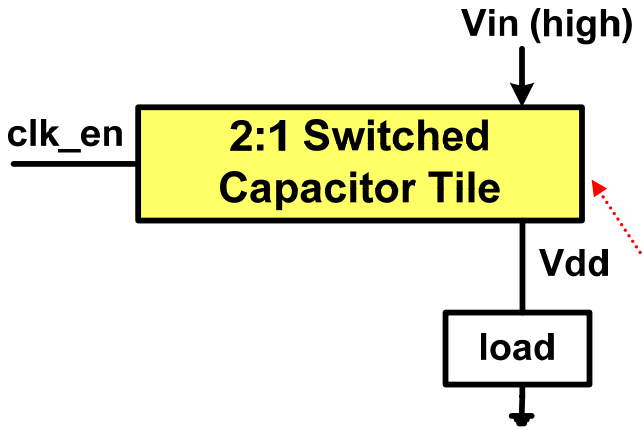
3-D implementation:
Interpose chip for voltage conversion/regulation



- **Implementation depends on system requirements, area availability**

Fast Switched-Cap Strategy for Processors

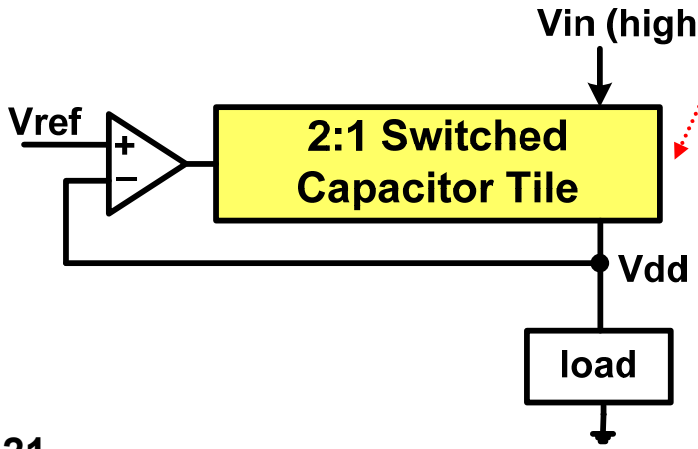
- **Open-loop operation**



- If SC is fully ON, Vdd varies linearly with load current
- SC could be turned on with a certain duty cycle depending on output load current

DT flying capacitors also act as decoupling caps for Vin and Vdd

- **Closed-loop regulation**

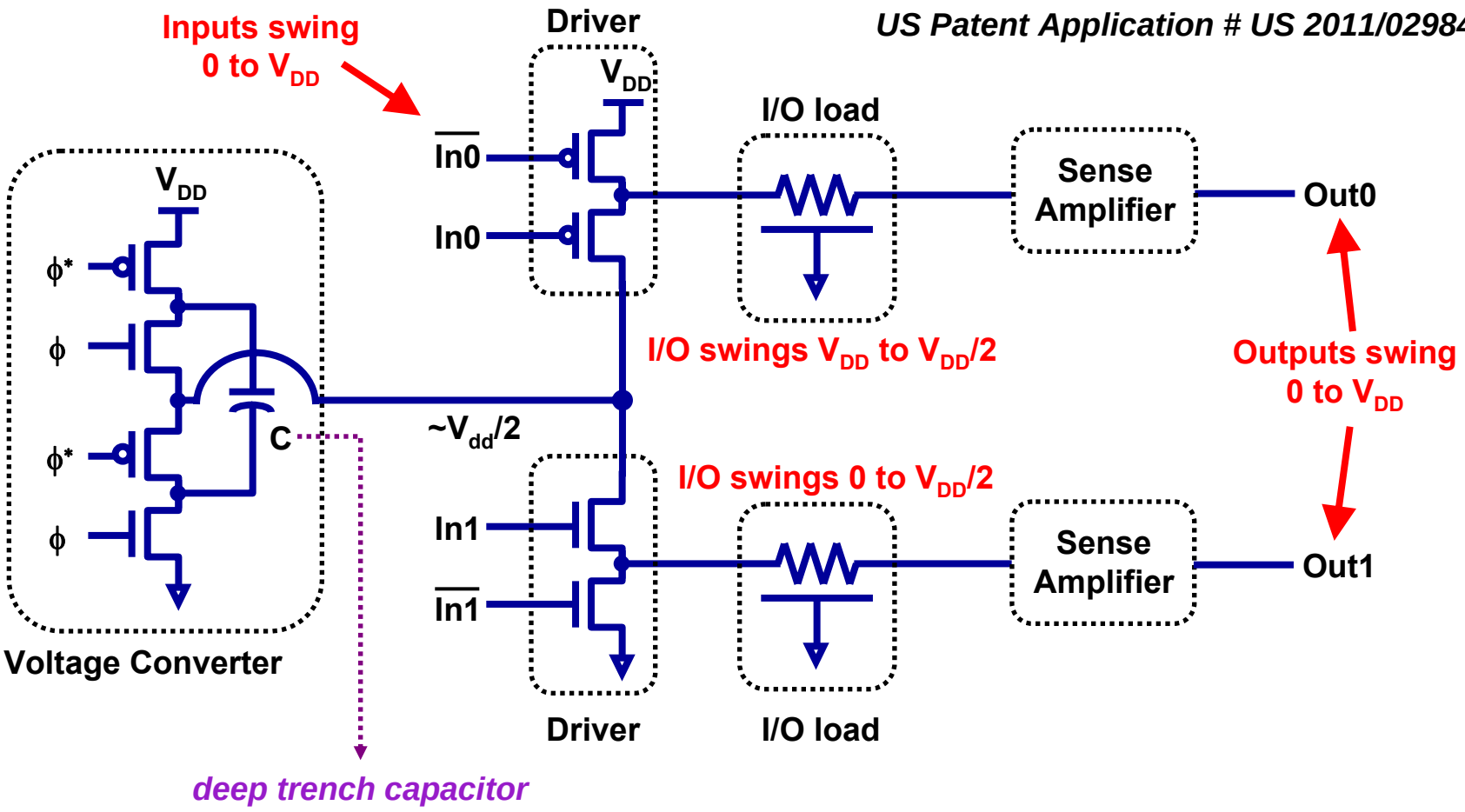


- Needs accurate reference voltage
- Overall closed-loop latency is critical for noise reduction
- Input voltage noise largely handled against load fluctuations

Ramadass JSSC10, Kim JSSC12

Another Application – Stacked I/O

- **Stacked I/O for low voltage signaling**



Summary

- High-voltage power delivery is beneficial to reduce power distribution losses, which could be achieved with switched-capacitor down-conversion
- Deep trench capacitors enable switched-capacitor converter to achieve high efficiency and high output current
- Clear scaling path is shown for deep trench capacitors towards 22nm and beyond
- Design tradeoff exists between efficiency, area, output current
- DT-based switched-capacitor circuits offer solutions for highly-efficient voltage regulation modules for various applications

Thank you!